

Challenges and Responses for Virtual Silicon

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Abstract—The dimensional evolution of device has increased the importance of TCAD simulation and its multilateral expansion to process and design domains. Challenges for achieving virtual silicon as a holistic simulation analysis and recent progresses are discussed.

Keywords—TCAD; semiconductor simulation; virtual silicon; device modeling; process modeling

I. INTRODUCTION

Aggressive device engineering such as non-planar and multi-gate structures, strain engineering, and HK/MG process have exposed both challenges and opportunities for TCAD [1]. Especially, the introduction of a 3rd dimension into device and process integration has triggered huge demands for TCAD simulation. Although relatively simple electrostatics and stress calculations have composed the majority of contributions to 3D device design, novel quantum mechanical transport simulation are now required for analyzing new channels and architectures for the sub 5nm node. Moreover, device engineers and designers have started to discuss exploiting the concept of virtual silicon in order to hedge the risk arising from difficulties in optimizing many new knobs simultaneously. Concurrent optimization of design and technology based on prediction of Si characteristics has now become an integral component of technology development.

On the other hand, recent innovation in 3D process integration has cast serious challenges on process modeling and simulation, resulting in amplified concerns on the lack of the modeling capability for high aspect ratio etch and macro-scale deposition processes and significant limitations of TCAD contribution. Taking into account that such critical processes may limit technology development and the recent increase in process integration failures, simulation-based process design is foreseen to become the most critical issue in the next decade.

The paper consists of three major parts – advanced atomistic simulation for device path-finding, simulation-based concurrent optimization of technology and design, and critical process modeling and 3D integration analysis. Recent progresses in each modeling area will be highlighted.

II. ATOMISTIC MODELING FOR DEVICE PATH-FINDING

Many efforts have been made to continue on the path of scaling device dimensions with TCAD simulation. Simulation has helped to successfully navigate through complex issues of scaling nano-scaled devices. However, as the traditional scaling of dimensions no longer enhance performance, further advances require solid understanding of quantum transport, new materials, defects, and microscopic nature of processes.

The challenge is inserting more physically rigorous (but time-consuming) approach in efficient daily simulation flow. The remainder of this section will discuss some examples of atomistic/microscopic approach in device and process modeling.

Exploring new material for high channel mobility is done with a physics based atomistic or microscopic model because the experimental data are insufficient and its validity under very thin and highly-strained condition is often debated. For SiGe channel, atomistic approach was used to augment a conventional Drift-Diffusion (DD) model [2]. The SiGe alloy channel is described in the atomistic level and the alloy scattering mobility for various channel thicknesses and strains is computed without fitting parameters as shown in Fig. 1.

A coupled DD and multi-subband Boltzmann transport equation (MSBTE) solver can be a practical TCAD tool to

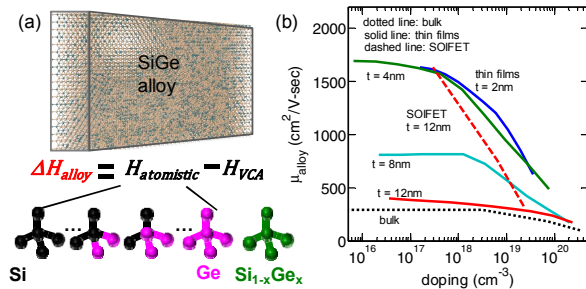


Fig. 1. (a) Alloy scattering potential is extracted with atomistic description of alloy and virtual crystal approximation (VCA). (b) Alloy mobility in confined structure compared to bulk.

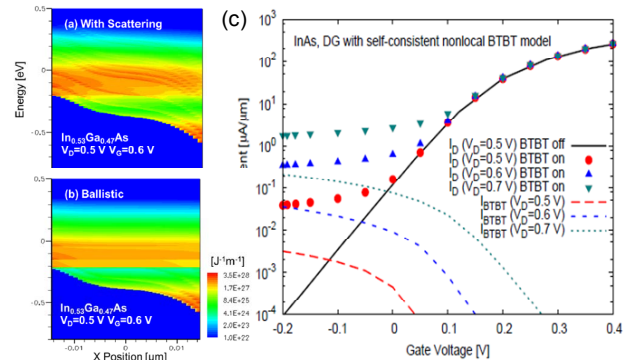


Fig. 2. (a) Energy resolved electron density: MSBTE solver well describes quasi-ballistic transport (b) Improved BTBT model for stress/orientation/non-parabolic bandstructure.

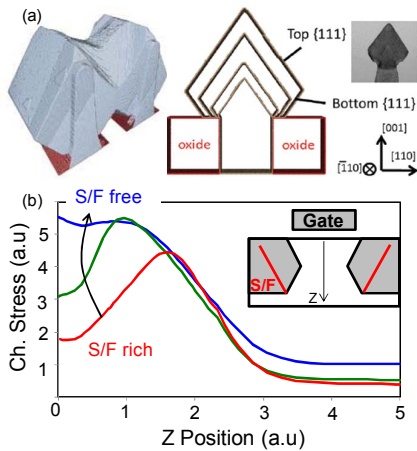


Fig. 3. (a) Profile evolution in Epi process can be simulated with KLMC. (b) pFET SD stress analysis to minimize Stacking Fault (S/F) induced relaxation.

assess the performance of device with III-V gate-all-around channel [3]. Taking into account the stress and orientation dependent bandstructure (beyond effective mass approximation) and quantum-confinement effect, surface roughness (SR) scattering and band-to-band tunneling (BTBT) rate are correctly computed. It is shown that expected ballistic performance for InGaAs could not be obtained due to strong SR scattering and the BTBT induced off-current is marginal as shown in Fig. 2.

Strain engineering (e.g. Source/Drain (SD) embedded stressor) has become another enabler of improved device performance. Atomistic modeling approach of epitaxial growth such as Kinetic Lattice Monte Carlo (KLMC) is crucial to control realistic epi-grown shape in SD [4] because the improved DC performance by stress often translated to unwanted increase of gate-to-SD capacitance. In addition,

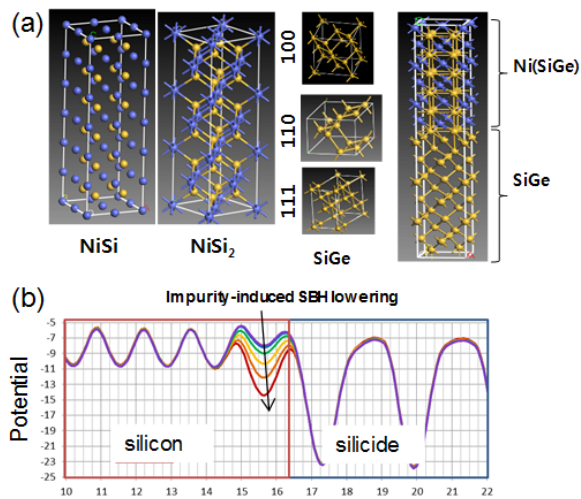


Fig. 4. (a) Atomistic modeling compute SBH for various choice of silicide and SD material. (b) This example shows that impurity engineering can reduce SBH by dipole formation.

judicious engineering of SD epi-growth is required to avoid stress relaxation by stress-induced defects (Fig. 3). Since validity of finite element method (FEM) is questionable in highly strained nanostructure, the valence force field (VFF) method is coupled with the FEM to include nonlinearity with an atomic level description of system [5].

As channel resistance becomes close to ballistic limit due to high mobility channel by either new material or strain engineering, portion of contact resistance (R_c) to total resistance keeps increasing. Ab-initio calculation can provide a good guideline of lowering Schottky barrier height (SBH) as there are many choices of silicide material as well as impurity/defect engineering (Fig. 4).

III. DESIGN-TECH CO-OPTIMIZATION WITH VIRTUAL SI

Traditional design and technology co-optimization (DTCO) has focused on the interplay between technology (device architecture and integration) and design (design rule and layout scheme) in terms of design for manufacturability [6]. As silicon scaling approaches to fundamental limit, however, the transistor performance is highly susceptible to design rule scaling and the parasitic RC portion of MOL and BEOL has increased. In addition, design impacts of new process knobs should be addressed in systematic manner. Thereby, the interplay between design and device performance has become increasingly important.

A. Augmentation with Virtual Silicon

The performance-power-yield (PPY) trade-off of circuits is assessed with virtual silicon, which is obtained by exhaustive TCAD analysis on DC/AC performance and secondary effects such as local layout effect (LLE) and self-heating. Recent introductions of aggressive performance knobs significantly increase risks in having timely reliable HW data to transfer device characteristics into design domain. Especially, augmentation with virtual silicon including early-stage variability assessment [7] is imperative for the novel transistor and BEOL schemes (e.g. nanowire, nanosheet, air gap etc) beyond 5nm technology nodes. In the next section, the LLE is discussed in terms of the evolution of physical mechanisms with new technology options.

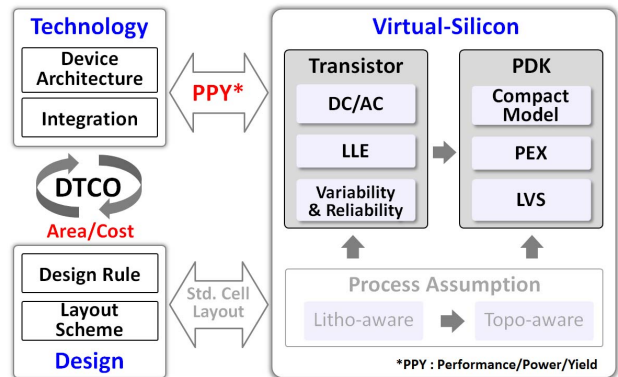


Fig. 5. Augmented DTCO platform with virtual Si.

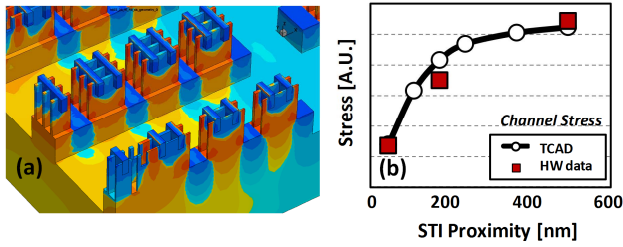


Fig. 6. (a) 3D process simulation with stress effects. (b) Comparison between TCAD results and HW data.

B. Local Layout Effects

Traditionally, LLE have occurred mostly due to shallow trench isolation (STI) induced stress and well proximity effect (WPE) [8]. However, in recent technologies, LLE comes from various other sources such as active-to-active space, types of trench isolation, gate patterning, and so on. Moreover, the advent of multi-Vt HK/MG process to meet the designers' needs for multi-Vt flavors has aggravated the variability of gate-related LLE. To assess these stress- and WF- induced LLE, full 3D process and device simulation in standard cell level is necessary. Since it is still not clear how to change the stress profile of the materials during the process, the stress models should be extensively validated with hardware data. Fig. 6 shows the full 3D process simulation with stress effect, and the simulated stress results are well matched with measured stress level. To take into account of LLE in circuit analysis, LLE model is accurately implemented into compact model as well as LVS.

IV. 3D INTEGRATION MODELING

Challenges imposed to 3D integration are discussed in terms of the critical fabrication processes (etching and deposition) as well as mechanical failure analysis based on multi-physics simulation.

A. High Aspect Ratio etching

Achievement of 3D vertical integration is inevitable for high density integration which could be feasible only with high aspect ratio (HAR) patterning typically bringing about shape related failures such as bowing, necking, distortion, and so on. There has been increasing need for rigorous simulation of plasma generation, particle trajectory and surface reaction in order to control those defects quantitatively as shown in Fig. 7.

As for surface reaction out of three simulation tasks above, many researches are conducted to reveal detailed mechanism of chemical reactions between $C_xH_yF_z$ on dielectric surfaces with molecular dynamics (MD) and density functional theory (DFT) calculations [9,10]. Major reactions are passivation of polymer layer and sputtering due to highly energetic ions. These reactions are governed by radicals' sticking coefficient (SC) on the surface and high energy ions' sputtering yield (SY). Recent advance in atomistic simulation enables direct determination of reaction coefficients (SC, SY) and integration with proper reaction models makes more accurate topography simulation feasible for the HAR etching [11].

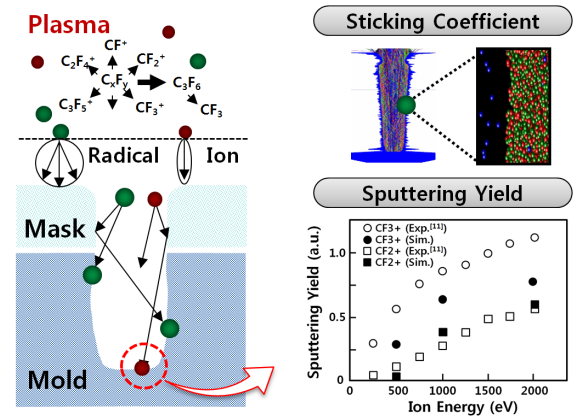


Fig. 7. Plasma coupled feature scale topographic simulation based on physical surface reactions.

B. Deposition

Fluid analysis was playing a major role for process optimization of ALD/CVD/Etch process since uniform gas distribution was a key factor for the process yield enhancement. However, fine 3D structures on the wafer surface cause drastic variations in correlation between gas distribution and process yield. Arrangement/structure of profile/chip on the wafer modifies effective surface area and even surface reactions which in turn affect gas flow significantly. Hence, classical fluid analysis has limitations for quantitative optimization of process conditions [12]. Accordingly, key challenges are to find out proper relations between modification of surface reaction and fine structures in wafer including consequent effects on the gas flow. These enable multi-scale simulation which relate feature scale geometry to equipment scale fluid simulation and yield prediction capability for profile shape and distribution as shown in Fig 8.

C. Mechanical Failure Analysis with Multi-Physics

Structures with ever increasing HAR, owing to continuous scaling down of the device, face mechanical failures such as bending, leaning, and cracking, during the processes in addition to above-mentioned topographical issues of deposition

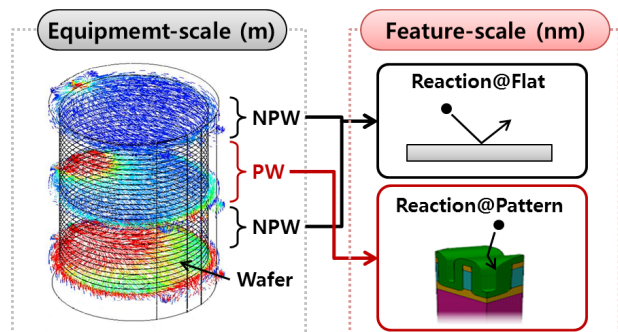


Fig. 8. Schematic illustration of feature to equipment bridging simulation.

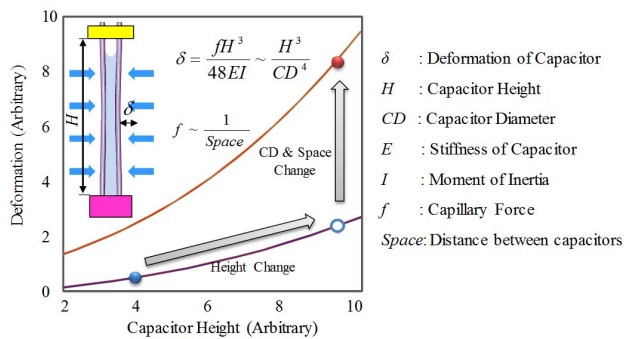


Fig. 9. Deformation of DRAM capacitor depending on height, CD and space (Equation of cylinder deformation by surface tension load).

and etch processes. In the case of DRAM-capacitor being affected by surface tension during wet cleaning process, structural strength is inversely proportional to the cubic height. Further, surface tension is also inversely proportion to space [13]. Hence, deformation of the capacitor increases by about 20 times, when height of the capacitor is doubled (Fig.9).

There are various types of external forces causing the mechanical failures such as surface tension, film intrinsic stress and CTE (coefficient thermal expansion) mismatch. Identifying the dominant forces among them and predicting precise deformation during the cleaning process is a huge challenge because of complex liquid-vapor-thermal-structural interactions governing the phenomena of so called FSI (Fluid-Structure Interactions). Liquid flow is significantly affected by molecular adhesive forces from solid structure, whereas adhesive forces from the gas/vapors above the fluid's free surface are weaker. Hence, the liquid surface tension behavior is the most influential factor and should be predicted with due accuracy for the residual liquid shape and contact angle. Also, phase transformation of the cleaning liquid through evaporation drives heat transfer through the surface of the fluid. Hence, simultaneous modeling of such coupled effects in a computationally efficient framework is needed.

V. CONCLUSION

Relentless technology scaling has opened abundant opportunities to TCAD. Traditional device centric simulation needs to be expanded to process and material modeling and design co-optimization domains. Exploiting virtual silicon as a

strategic decision solution will serve as an integral competence in semiconductor manufacturing. Recent successful technical progresses demonstrate that the virtual silicon is more than virtual.

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