Investigation of leakage current in pinned photodiode CMOS imager pixel with negative transfer-gate bias operation

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***Abstract*—The characteristics of leakage current observed in the pixels of pinned photodiode CMOS image sensor with negative transfer-gate bias operation are investigated, taking metal contamination into account. Simulation results show that interface states between insulator and the pinned layer in the vicinity of transfer gate, acting as hole traps, are responsible for negative transfer-gate bias dependence of the dark current.**

Keywords—CMOS image sensor, bright/hot pixels, dark current, hole trap

I. INTRODUCTION

Four-transistor pixels with pinned photodiode in a CMOS image sensor, utilizing a negative offset voltage to the gate of the transfer transistor, particularly only when the transfer transistor is off, have been studied [1], [2]. The advantage of utilizing the negative offset voltage is two folds: the reduction of voltage drop due to dark current of the pinned photodiode and the enhancement of the well capacity [1], which are attributed to the accumulated holes and the increased potential barrier near the pinned photodiode, respectively.

Bright/hot pixels in the state-of-the-art CMOS image sensors are one of the main limiting factors for their performance. They can be caused by a number of defects, including bulk Si dislocations or metal contamination, or interface states at the surface or at the isolation, or interface states or traps in the gate dielectrics.

In this study, pinned photodiode CMOS image sensors were fabricated using four-transistor-shared pixel architecture. Fig. 1 and 2 show dependence on negative transfer-gate bias of measured dark current and number of bright/hot pixels, respectively. Previous work [3] suggests that accumulation of holes at the interface between gate insulator and silicon reduces the generation rate of dark current. It is also reported that further lowering of negative gate bias beyond -0.9V in turn increases dark current [1], which is attributed to the trap-assisted tunneling leakage current induced by negative gate bias [2]. As shown in Fig. 1, the reported characteristics [1], [2] were not observed, indicating that there is another mechanism of dark current. We supposed a bright/hot pixel have extremely large dark current, so we assumed a highly and locally contaminated pixel with metallic impurity. The aim of this study is to examine the dark current in the pixels with the transfer-gate bias of -0.8V and -1.4V, considering metal contamination.

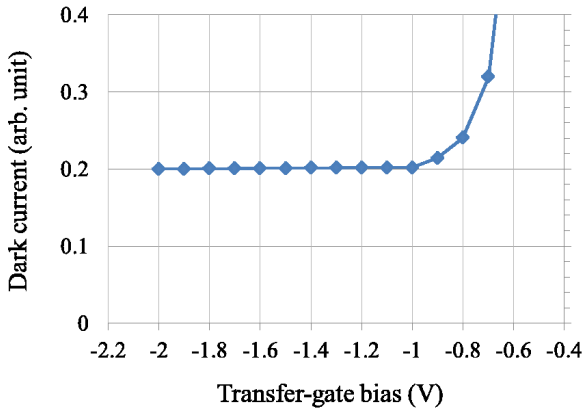

Fig. 1. Dark current characteristics as a function of negative transfer-gate bias. (measured data)

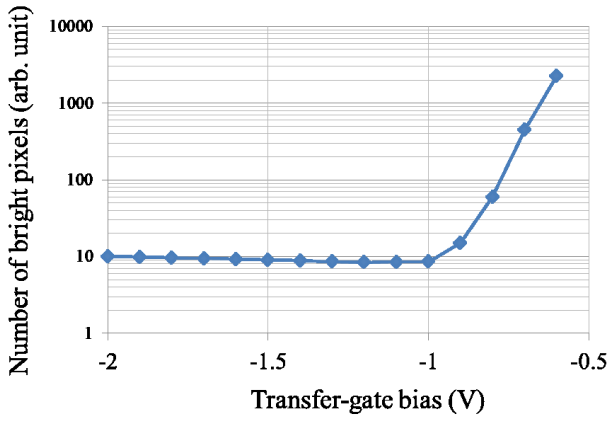

Fig. 2. Number of bright/hot pixels as a function of negative transfer-gate bias. (measured data)

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II. DARK CURRENT MODEL

Metallic impurities, for example, Fe, Cr, Cu, Mo and Co, are common in photovoltaic grade crystalline silicon. Fe can exist in p-type silicon as either interstitial iron, Fe*i* [4], or paired with boron atoms, Fe-B [5]. In this study, we focus on Fe*i* because it is an especially common contaminant [4]. In order to investigate the effect of negative transfer-gate bias on dark current in the pixels, we assume Fe*i* as a contaminant, which generates interface states acting as a hole trap: it produces a deep level in the band gap, as shown in Fig. 3, and its capture cross section is 7e-17cm^2 [4].

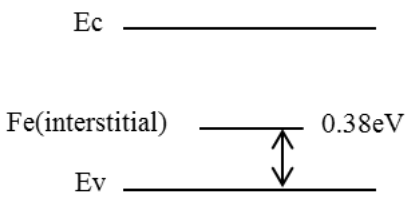

Fig. 3. Energy level of trap due to interstitial Fe

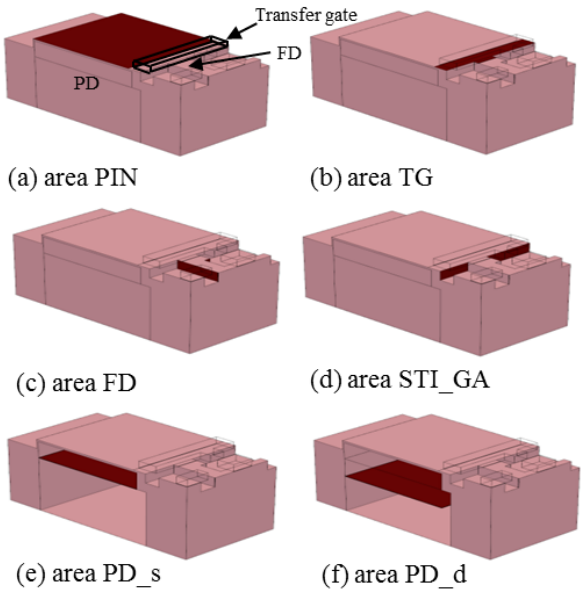

Fig. 4. Areas in which interstitial Fe is distributed evenly. Brown region indicates the areas. (Silicon is shown only)

To get a good insight into the location in the pixel where the leakage current is generated, Fe*i* is assumed to be evenly distributed at the interface of the following areas; (a) insulator/the pinned layer (area PIN), (b) gate insulator/channel region of the transfer-gate (area TG), (c) STI sidewall/floating diffusion (area FD), (d) STI sidewall/silicon substrate underneath the transfer-gate (area STI_GA), (e) shallow position of the depth of 0.5um from the silicon surface (area PD_s), and (f) deep position of the depth of 1um from the silicon surface (area PD_d), respectively, as shown in Fig. 4. The interface states are filled by means of holes in the p-type impurity layer. Area PD_s and PD_d are the virtual interface in order to set the same trap area density for convenience. Contribution of each area to dark current is investigated by three-dimensional device simulation in a TCAD tool [6]. Dark current is calculated by integrating the electrons accumulated in the pinned photodiode after the reset operation.

III. RESULTS AND DISCUSSION

Fig. 5 shows hole density distribution during dark current integration period (a) without and (b) with hole traps located in area PIN, respectively. The trapped hole induces localized modulation of the electrostatic potential at the surface of silicon in the vicinity of transfer gate and increases the depletion width at the surface, leading to increase in the Shockley-Read-Hall (SRH) generation current which flows into the photodiode.

Fig. 6 shows comparison of dark current generated in each region with hole trap area density of (a) 1 (arb. unit) and (b) 100, respectively. Although a concentration of a metallic impurity is close to 1 on average (indicating no contamination) by use of contamination monitoring of silicon samples, there exists the locally contaminated area in bright/hot pixels. In this study, we assume the hole trap area density in a bright/hot pixel is 100 times as large as that in a normal pixel. Each dark current is normalized by the value in area PD_s with trap area density of 100. There is no difference among the dark current in six areas with no contamination. By changing the gate bias from -0.8 to -1.4V, the dark current especially generated in area PIN is reduced, as shown in Fig. 6(b). It might be attributed to iron pileup at the Si-SiO_2 interface [7].

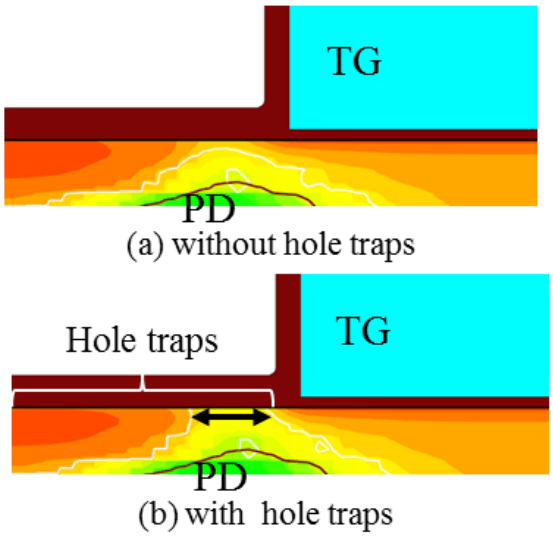

Fig. 5. Hole density distribution during dark current integration period; (a) without hole traps, and (b) with hole traps located in area PIN, respectively. An arrow indicates the depletion width at the insulator/pinned layer interface. White line indicates the boundary of the depletion region. Bias of -1.4V is applied to the transfer gate TG.

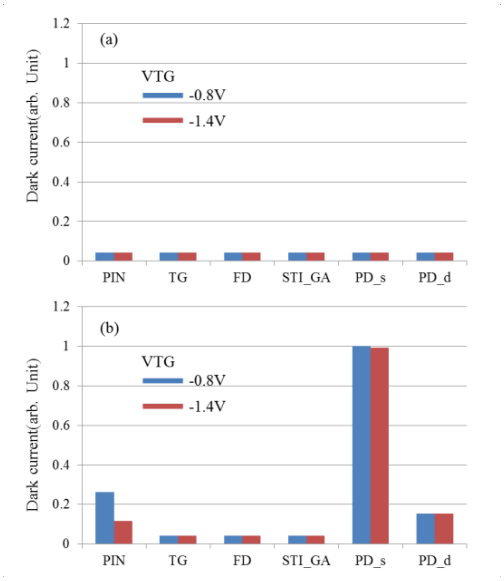

Fig. 6. Comparison of dark current generated in each region with hole trap area density of (a) 1 (arb. unit) and (b) 100, respectively.

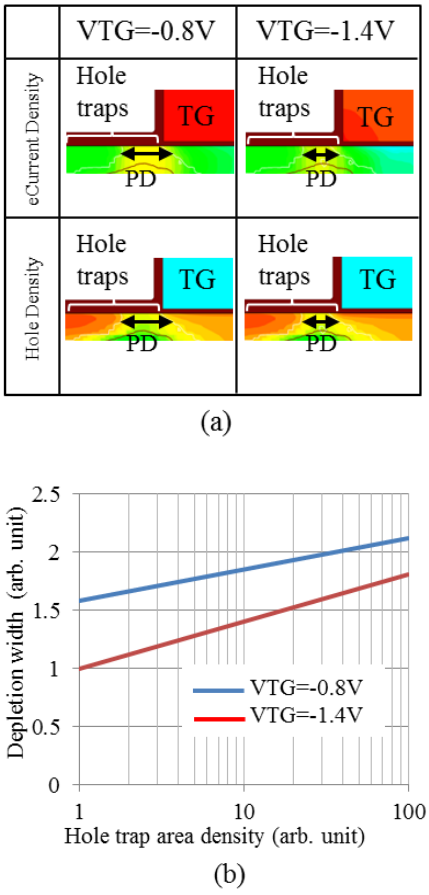

Fig. 7. Electron current density and hole density distribution during dark current integration period with hole trap density of 100 (arb. unit) in area PIN. Arrows indicate the depletion width at the insulator/pinned layer interface. (b) Depletion width at the interface as a function of hole trap density.

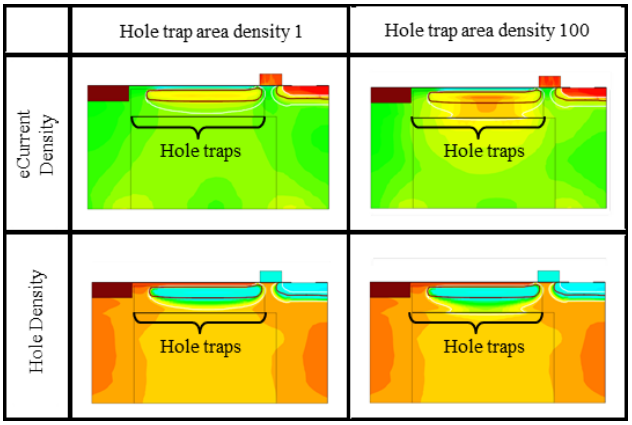

Fig. 8. Electron current density and hole density distribution during dark current integration period with hole trap density of 1 (arb. unit) and 100, respectively, in area PD_s. Bias of -1.4V is applied to the transfer gate.

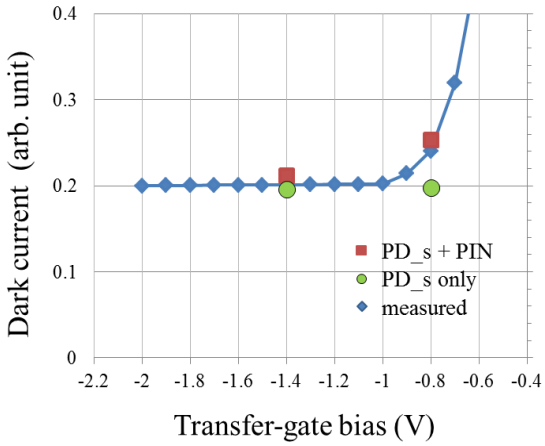

Fig. 9. Dark current characteristics as a function of negative transfer-gate bias. Hole trap area density of 100 (arb. unit) is assumed.

Note that there is no reduction in dark current by changing the gate bias in the case of area TG. We suppose the area under the transfer gate is filled enough with holes which are accumulated even if the transfer-gate bias is equal to -0.8V. In the case of area PIN, as shown in Fig. 7, changing the bias from -0.8 to -1.4V decreases the depletion width at the interface of insulator and pinned layer due to the hole accumulation at the silicon surface under negative transfer-gate bias.

Fig. 8 shows electron current and hole density distribution during dark current integration period in the case of area PD_s. The area of the depletion region underneath the photodiode increases with the hole trap area density of 100, leading to increase in the dark current. As this area is far from the transfer gate, the negative bias does not affect the dark current as shown in Fig. 6 (b).

Fig. 9 shows the calculated leakage current compared with the measured data. The calculated leakage current, considering both area PIN and PD_s, matches very well with measured data, which validates the present model.

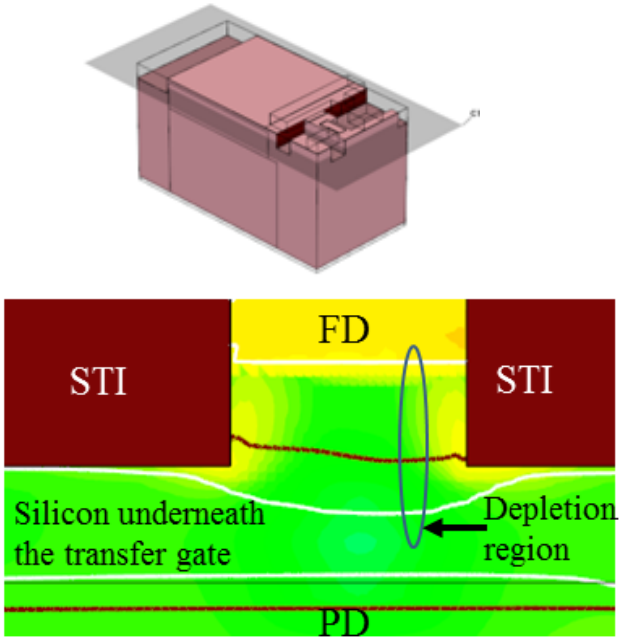

Fig. 10. Partial cross section of electron current density distribution during dark current integration period. (hole traps located in area STI_GA, VTG=-1.4V) White line indicates the boundary of the depletion region.

Fig. 10 shows cross-sectional view of electron current density distribution with hole traps located in area STI_GA. Electron current generated in the depletion layer at STI sidewall flows into the floating diffusion. Although these electrons do not contribute to the dark current in our evaluation as they pass through silicon underneath the transfer gate without being accumulated in the pinned photodiode, they can be responsible for the actually measured dark current. Note that this dark current is different from the dark current in area STI_GA.

Finally, we investigate the dark current in the case of Fe*i* acting as an electron trap whose energy level is same as that of a hole trap, as shown in Fig. 3. We assume that a capture cross section of electron traps is 5e-14cm^2 [4] which is larger than that of hole traps. Fig. 11 shows the comparison of dark current due to hole traps and electron traps in the area of PIN, respectively. Each dark current is normalized by the value in area PD_s with trap area density of 100, as shown in Fig. 6(b). Even in the trap density of 100, the dark current due to electron traps is smaller than that due to hole traps. It is found that the expanding the width of the depletion region due to hole traps is a significant factor of the dark current under the negative transfer-gate bias operation.

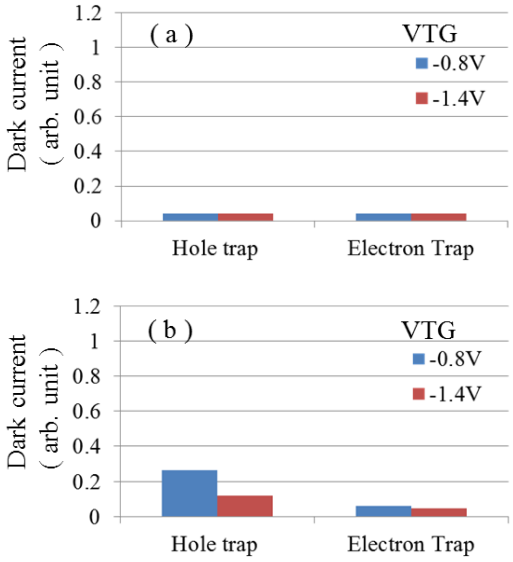

Fig. 11. Comparison of dark current in the area PIN with hole and electron area trap density of (a) 1 (arb. unit) and (b) 100, respectively.

IV. CONCLUSION

The characteristics of leakage current observed in the pixels of pinned photodiode CMOS image sensor with negative transfer-gate bias operation are investigated, taking metal contamination into account. We focus on interstitial iron (Fe*i*) which is an especially common contaminant. Simulation results show that interface states between insulator and the pinned layer in the vicinity of transfer-gate, acting as hole traps, are responsible for negative transfer-gate bias dependence of the dark current. The trapped hole induces localized modulation of the electrostatic potential at the surface of silicon in the vicinity of transfer gate and increase in the Shockley-Read-Hall generation current.

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