Automated Vertical Design Optimization of a 1200V IGBT

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Abstract—Many important performance parameters in an IGBT power semiconductor are heavily affected by its field-stop profile, its device thickness and its collector-side p-doping concentration. To find the optimum combination of these design parameters is of high importance for an optimal IGBT design. The optimization criteria include low switching and on-state losses as well as limited maximum overshoot voltage and modest current and voltage rise and fall times. This work focusses on an automated global optimization scheme to solve this issue. The method and definition of a proper target function are briefly explained. Finally, design optimizations found under different constraints are discussed.

I. INTRODUCTION

The desired switching profile of an IGBT is crucial for design optimization (e.g. [1], [2]). It has to be optimized for lowest switching losses, but at the same time exhibit only modest maximum overshoot voltage \(V_{ce,max}\), combined with a low \(\frac{dV}{dt}_{10,90}\). For example a maximum \(\frac{dV}{dt}_{10,90}\) of 5 \(\mu V\) is required for drive applications. The term \(\frac{dV}{dt}_{10,90}\) denotes a voltage gradient calculated from points taken at 10% and 90% DC Link voltage \(V_{DC}\) on the rising edge. These requirements arise from electromagnetic compatibility (EMC) and interference (EMI) issues [3] as well as electric motor lifetime considerations [4]. While turn-off losses in general decrease with a reduced collector-side p-doping, \(\frac{dV}{dt}_{10,90}\) is required. The current gain of the IGBT cell was fixed to the backside, as a final peak in front of the collector-side p-doped layer is necessary for a field-stop IGBT to prevent that the space-charge region expands into the p-doped layer during reverse blocking. Further optimization parameters include the collector-side p-doping dose \(d_p\), as well as the device thickness \(x_w\) which was adjusted to fulfill the breakdown voltage requirements of a 1200V IGBT. The optimization parameters are shown in Tab. I.

<table>
<thead>
<tr>
<th>(\sigma_1)</th>
<th>(N_1)</th>
<th>(\sigma_2)</th>
<th>(x_2)</th>
<th>(N_2)</th>
<th>(d_p)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>(\mu m)</td>
<td>(cm^{-3})</td>
<td>(\mu m)</td>
<td>(cm^{-3})</td>
<td>(cm^2)</td>
</tr>
<tr>
<td>Min:</td>
<td>1.0</td>
<td>(N_{min})</td>
<td>1.0</td>
<td>(N_{min})</td>
<td>0.2 (\times 10^{13})</td>
</tr>
<tr>
<td>Max:</td>
<td>20.0</td>
<td>60 (\times N_{min})</td>
<td>20.0</td>
<td>30 (\times N_{min})</td>
<td>2.4 (\times 10^{13})</td>
</tr>
</tbody>
</table>

In the annealing scheme, a complete turn-off simulation of the respective IGBT cell was performed utilizing the device simulator Sentaurus Device. In each isothermal simulation at 25 °C, the two-dimensional IGBT cell was switched off from \(I_{nom} = 140\) A, at a DC link voltage of \(V_{DC} = 800\) V. The chopper circuit used in the simulations is illustrated in Fig. 1 together with a sketch of the IGBT cell.

In order to optimize the design parameters of the IGBT for a low-power application and a high-power application, different stray inductance \(L_s\) have been used in the chopper circuit: 60 nH for the low-power application and 300 nH for the high-power application. The field-stop profile was parameterized via two Gaussian functions \(G_1(\sigma_1, x_1 = 0, N_1)\) and \(G_2(\sigma_2, x_2, N_2)\) where \(\sigma\) denotes the standard deviation, \(x\) the central position of the Gaussian function in \(\mu m\) from the backside, and \(N\) the peak concentration of the respective Gaussian function. The position of \(G_1\) was fixed to the backside, as a final peak in front of the collector-side p-doped layer is necessary for a field-stop IGBT to prevent that the space-charge region expands into the p-doped layer during reverse blocking. Further optimization parameters include the collector-side p-doping dose \(d_p\), as well as the device thickness \(x_w\) which was adjusted to fulfill the breakdown voltage requirements of a 1200V IGBT. The optimization parameters are shown in Tab. II.

<table>
<thead>
<tr>
<th>(\frac{dV}{dt}_{10,90})</th>
<th>(V_{ce,max})</th>
<th>(V_c)</th>
<th>(V_{ce,off})</th>
<th>(E_{off})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>(\mu V)</td>
<td>V</td>
<td>V</td>
<td>mJ</td>
</tr>
<tr>
<td>Constraint</td>
<td>&lt; 6.0</td>
<td>&lt; 1150.0</td>
<td>&lt; 20.0</td>
<td>1.4</td>
</tr>
</tbody>
</table>

During each run the resulting switching profile was evaluated and several parameters were extracted. These evaluation parameters are shown in Tab. II. In order to assess the strength of ringing - i.e. the excitation of an oscillation in the \(V_{ce}\)-transient that is induced by a large current-decrease rate in the resonant circuit formed by the stray inductance and the device capacitance - we used the quantity \(V_{r}\). It is defined as the amplitude of the first half cycle of the excited \(V_{ce}\) oscillation.
appearing after the voltage overshoot (cf. Fig. 2). The target values of the turn-off losses $E_{\text{off}}$ were set to relatively low values, namely 5.0 mJ and 10.0 mJ for the low-power and the high-power case, respectively. All other bounds remained the same for both optimizations.

The evaluation parameters entered into a target function $f$ based on a sum over relative errors

$$f = \sum_i \gamma_i \left( \frac{x_i - x'_i}{x'_i} \right)^2 + P(x_i, x'_i)$$

where $x_i$ denotes the i-th evaluation parameter, $x'_i$ its target value, and $\gamma_i$ an additional weighting factor for each parameter. Here $P(x_i, x'_i)$ defines a penalty function

$$P(x_i, x'_i) = \kappa_i \left| \text{erfc} \left( \frac{x_i}{x'_i} \right) \right|$$

where $x'_i(x'_i)$ is the corresponding violated bound of the i-th parameter, $\kappa_i$ its corresponding penalty weight, and erfc is the complimentary error function. After the target function was computed, a new parameter set was chosen according to the simulated annealing scheme and the annealing temperature was lowered by a cooldown factor $\alpha \in (0, 1)$, usually close to 1. The simulated annealing scheme for a single iteration $j$ at a given value of the target function $f_j(\vec{x}_j)$ for a parameter set $\vec{x}_j$ and annealing temperature $T_j$ can therefore be summarized as:

- Randomly determine new trial parameter set $\vec{x}_{tr}$.
- Compute trial value $f_{tr}(\vec{x}_{tr})$.
- If $f_{tr} \leq f_j$:
  - $\vec{x}_j \leftarrow \vec{x}_{tr}$
  - $T_j \leftarrow \alpha T_j$
- Else: Draw uniform random number $r \in [0, 1]$.
  - If $r < e^{-(f_{tr} - f_j)/T_j}$, $\vec{x}_j \leftarrow \vec{x}_{tr}$, $T_j \leftarrow \alpha T_j$
  - Else: $T_j \leftarrow \alpha T_j$ (reject trial parameters)
- $j \leftarrow j + 1$

A flow of the whole optimization procedure is displayed in Fig. 3. Optimization runs with 250 iterations each have been performed. The computational speed of the optimization strongly depends on the capability of the device simulator to solve the turn-off transient of the IGBT quickly. In our case a single optimization iteration took around 10 minutes.

### III. High-Power IGBT Variant

The resulting decrease of the target function for the high-power case is shown in Fig. 4 and plotted together with the applied simulated annealing temperature. An almost global minima was already found after 50 iterations, but due to the still high simulated annealing temperature further configurations were evaluated. At the end, the solution fluctuated around the previously found configuration, thus reaching the global minima in iteration 246. The run continued until iteration 250. At the end, the global minima from iteration 246 was written out. For selected iterations of this optimization run, transient switching profiles were extracted (Fig. 5). While the profiles at iteration 21 and iteration 109 exhibited a fast switching with lower turn-off losses, they violated several constraints, such as the $V_{\text{ce, max}}$ limit.

A more detailed analysis of the contribution of each term to the target functions at the three selected iterations is presented.
in Fig. 6. The profile at iteration 21 violated especially the 
\( \frac{dV}{dt} \) constraint, resulting in large penalties. As 
the optimization continued, these penalties could be reduced, 
while keeping an almost constant \( E_{\text{off}} \) with a reduction of 
\( V_{\text{ce sat}} \) from 1.5V to 1.3V (iteration 109). However, only for 
the final profile, the \( \frac{dV}{dt} \) constraint could be met, in this case at the cost of an increased \( E_{\text{off}} \). The 
final switching curve is shown in more detail in Fig. 7. The 
\( \frac{dV}{dt} \) value was below 5 kV/\( \mu \)s, but for example the 
maximum value, defined as the maximum occurring \( \frac{dV}{dt} \), is higher. If it 
is necessary to reduce this value, it must be included into 
the target function. This also demonstrates a crucial aspect 
of the whole optimization scheme: A careful definition of the 
contribution of each term of the target function and the penalty 
function is very important, because they define the final device 
performance.

IV. LOW-POWER IGBT VARIANT

For the low-power case, a different optimum was found. 
While a similar decrease of the target function throughout 
the optimization as in the high-power case could be ob-
served, the resulting device parameters after 250 iterations 
were substantially different from those obtained in the high-
power case. As \( L_s \) for the low-power IGBT variant was 
considerably lower than in the high-power case, penalties in 
\( V_{\text{ce, max}} \) where less pronounced, allowing the optimization 
algorithm to decrease the device thickness and allow for a 
farther switching. The resulting optimized field-stop profile is 
shown in Fig. 8 together with that of the optimized high-power 
IGBT variant. While the high-power field stop reaches deeper 
into the device to allow for a slower build up of the electric 
field during turn-off, the low-power field stop is much more 
confined to the backside and more strongly doped to stop the 
field more aggressively and prevent a punch through as a result 
of the reduced device thickness. The final transient switching 
curves for the low-power IGBT variant are shown in Fig. 9 
together with its extracted evaluation parameters which entered 
the target function.
V. CONCLUSION

An automated scheme based on a simulated annealing algorithm was developed and applied to optimize the vertical design of a 1200V IGBT with respect to numerous constraints. Specific design solutions for high-power and low-power applications were derived. The optimization is based on the assessment of the IGBTs turn-off characteristics. The computational speed for a single transient switching calculation based on two-dimensional device simulation is crucial for the practicability of the presented method. The optimization algorithm can easily be extended to include also the assessment of the turn-on behavior or other criteria, for example the switching behavior at different DC link voltages or currents. The definition of the target function to be minimized during the optimization process is of great importance, as the contributions and the penalties associated with each term of the target function determine the final design performance.

REFERENCES