Impacts of the 4H-SiC/SiO_2 Interface States on the Switching Operation of Power MOSFETs

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***Abstract*—Impacts of the 4H-SiC/SiO_2 interface states on the switching operation of power MOSFETs are evaluated. The energy distributions of the interface states are characterized using measured C-V curves of the MOS capacitors with the aid of TCAD simulation. The effect of nitrogen incorporation into the SiC/SiO_2 interface via post-oxidation anneal (POA) on reducing the interface states is confirmed by the extracted energy distributions. The effect of POA on turn-on/off energy losses of the switching circuit is quantitatively evaluated using mixed-mode TCAD simulation with the extracted interface state parameters.**

I. Introduction

Silicon carbide (SiC) is very attractive for power devices because of its superior material properties such as high breakdown field and high thermal conductivity as compared with silicon. However, it also has the problem that a SiC MOSFET has more interface states than Si one, which constricts the commercial use. Many efforts have been dedicated to reduce the SiC/SiO_2 interface states. The most widely-used technique is to introduce nitrogen into the SiC/SiO_2 interface via post-oxidation anneal (POA)[1], [2], [3]. In this work, the effect of POA is analyzed through the comparison among measured C-V curves, and the types and energy distributions of the interface states are modeled using TCAD. In addition, we performed the switching calculation of SiC power MOSFETs and evaluated the impacts of the SiC/SiO_2 interface states on the device operation.

II. Experiments and Modeling

We fabricated three types of SiC-MOS capacitors. The process flow is shown in Fig. 1. A 4H-SiC(0001) substrate with an n-type epilayer (N_D = 1×10^{16} cm^{-3}) is used. After thermal oxidation in dry O_2 ambient at 1150 °C for 6 hours, following N_2O anneal (1050 °C for 6 hours) are implemented to passivate the Si dangling bonds at the SiC/SiO_2 interface. In order to investigate the effect of the passivation by nitrogen, we split the additional N_2 POA anneal time as follows: (a)w/o N_2 POA, (b)w/ 1000 °C for 1 minute (POA1) and (c)w/ 10 minutes (POA2).

We analyzed the effect of POA on the SiC/SiO_2 interface states by comparing the measured C-V curves of these MOS capacitors. Figure 2 shows the results of sequential forward (from -10 V to +10 V) and reverse (from +10 V to -10 V) gate biasing C-V measurements ((a)w/o N_2 POA, (b)w/ N_2 POA1 and (c)w/ N_2 POA2, respectively). The measurement frequency was 100 kHz. The dashed line indicates the calculated C-V curve of the ideal MOS capacitor which has no interface state. In Fig. 2(a), the gradual slope of the C-V curve compared with the ideal one, and the hysteresis between forward and reverse bias are observed[4]. These indicate that at least, two types of interface states exist as shown by red lines in Fig. 3. The first state (trap1) is near the conduction band edge and responds to the gate bias change quickly, which makes the C-V slope gradual. This state is intrinsically formed in 4H-SiC/SiO_2 interface[5]. The second (trap2) is in deep level of the band gap and response speed is slow, which causes the observed hysteresis. After the POA1, the C-V curve shows steeper slope and less hysteresis (see Fig. 2(b)), which indicates appropriate POA reduces both the first and second interface states (shown by green lines in Fig. 3). On the other hand, POA2 invokes the flat band shift during the forward biasing as observed in Fig. 2(c). This indicates the excess POA causes growth of the new state (trap3) shown by a blue line in Fig. 3, whose energy level is deeper than that of trap2 and response speed is faster than the other two.

Based on the above implications, we extracted the energy distribution parameters of these interface states to reproduce the measured C-V curves. As shown in Fig. 4, good agreements between measured and simulated C-V curves are obtained.

III. Analysis of Switching Operation

To analyze the effects of the interface states on the switching operation of SiC power MOSFETs, we investigated the turn-on/off energy losses focusing on the operation speed. The test circuit shown in Fig. 5 consists of a VDMOSFET (Q1) which is the device under the test, and a clamping Schottky barrier diode (D1). The drain node of Q1 is connected to an inductive load (L) with a series resistor (RL) and the gate node of Q1 is connected to the external load (Rin). Figure 6 shows the cross-sectional view of the 600 V class VDMOSFET analyzed in this study.

The turn-on/off switchings of the test circuits are simulated for VDMOSFETs with the above mentioned 3 different interface traps. The ideal VDMOSFET which has no interface state is also simulated as reference. Simulated devices are defined as follows: VDMOSFET w/o N_2 POA (VDMOS1), w/ N_2 POA1 (VDMOS2), w/ N_2 POA2 (VDMOS3) and w/o any interface states (ideal VDMOS). Figure 7 shows the typical simulated waveforms of the (a)turn-on and (b)turn-off in case of 10 μs input pulse rise and fall times, respectively. The turn-on/off gate pulses are applied after a long hold time, 1 s, which sets the interface states to be at thermal equilibrium. The turn-on/off

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waveforms for each VDMOSFET differ, reflecting response speed differences between the various types of interface states.

Evaluated gate pulse rise time dependence of the energy losses during turn-on operation (E_{on}) is shown in Fig. 8, in which every E_{on} is normalized by the ideal VDMOS's one. The VDMOS2, which has the smallest total amount of interface traps among 3 devices, shows the smallest E_{on} in all simulated conditions. The magnitude relation of E_{on} between the VDMOS1 and VDMOS3 depends on the rise time. Under relatively fast pulses ($t_{\text{r}} \leq 10^{-4}$ s), the VDMOS3 shows large E_{on}, which is caused by the fast responding trap3, while the VDMOS1's E_{on} exceeds under the slower pulse ($t_{\text{r}} = 10^{-3}$ s), which is able to be attributed to the slower state (trap2).

Gate pulse fall time dependence of the normalized energy losses during turn-off operation (E_{off}) is shown in Fig. 9. In all conditions, the VDMOS1 shows the largest E_{off} and the VDMOS2 shows the smallest. This result is reflected the total amount of interface traps because the all traps are occupied by the electrons at the starting time of the turn-off switching.

Next, a history effect under periodic gate on/off pulses is investigated by the transient simulation. The rise and fall time and frequency of the input pulse are set to 0.1 μs and 1 kHz respectively. Totally five cycles of the gate pulses are applied in these simulations. The entire simulated waveforms of the VDMOS1's drain voltage and current are shown in Fig. 10. As observed in overlaid turn-on waveforms (Fig. 11), turn-on switchings get slower as the input pulse repeats. The on/off cycle number dependence of E_{on} is compared among 3 types of VDMOSFETs in Fig. 12. The E_{on}(VDMOS3) is largest and shows small cycle dependence, while the E_{on}(VDMOS1) shows the largest dependence. These results are explained by charging/discharging of the interface trapped electrons. Figure 13 shows the transient characteristics of the interface trapped electron at the center of each VDMOSFET channel. The VDMOS3, containing the fast trap3, stores more trapped electrons during first turn-on, which cause large E_{on} from the first cycle. On the other hand, the VDMOS1, which contains large amount of slow trap2, continues to capture more electrons even in "on" time and discharges insufficiently in "off" time, and then, shows gradual increase of the amount of trapped electron as the input pulse repeats. Therefore, the E_{on}(VDMOS1) increases with respect to the cycle number. Above analyses indicate that interface states may cause the switching operation instability. Then, process development to reduce the interface states and circuit/system design considering the response speed of each interface state are important for stable switching operation.

IV. Conclusion

The 4H-SiC/SiO_2 interface states with nitrogen incorporation have been characterized considering the changes of C-V curves. The energy distributions of the interface states have been validated by reproducing the measured C-V curves using TCAD. Then, the impacts of the interface states on the switching operation of SiC power MOSFETs were investigated. The energy losses of turn-on/off switchings have increased with the total amount of interface traps. And the switching speed dependence of the energy losses have been characterized by considering the response speed of each interface state. It was pointed out that interface states may cause the switching operation instability.

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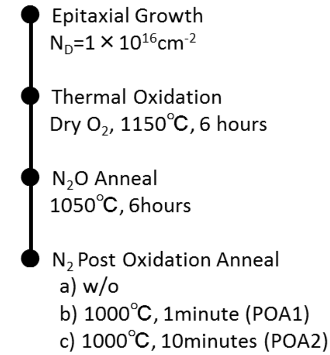

Fig. 1. Process flow to fabricate the SiC-MOS capacitors.

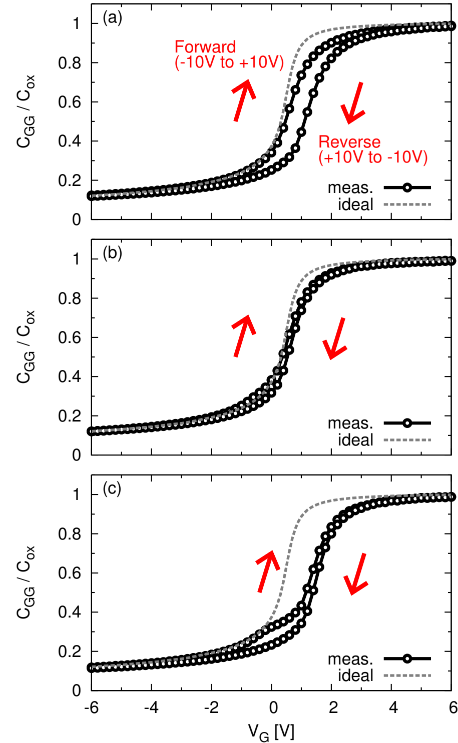

Fig. 2. Bidirectional C-V curves of the MOS capacitors, (a)w/o N_2 POA, (b)w/ N_2 POA1 and (c)w/ N_2 POA2, respectively. Sequential forward (from -10 V to +10 V) and reverse (from +10 V to -10 V) gate biasing is applied.

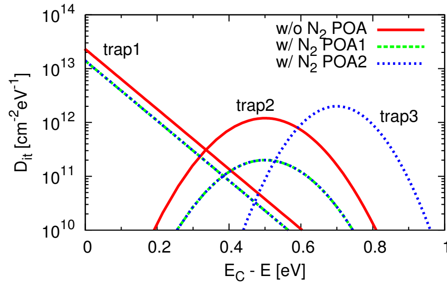

Fig. 3. Energy distributions of the SiC/SiO_2 interface states extracted to reproduce the measured C-V curves.

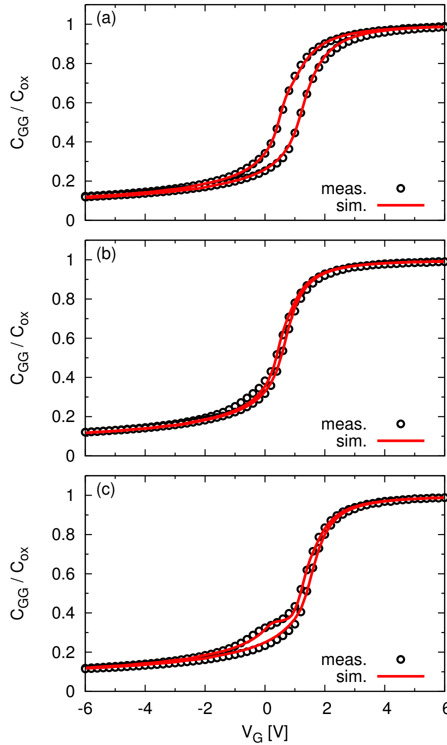

Fig. 4. Measured and simulated C-V curves of the MOS capacitors, (a)w/o N_2 POA, (b)w/ N_2 POA1 and (c)w/ N_2 POA2, respectively. TCAD simulations are executed using the energy distributions of the SiC/SiO_2 interface states shown in Fig. 3.

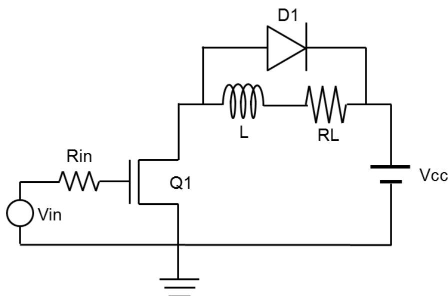

Fig. 5. Test circuit for inductive load switching simulations.

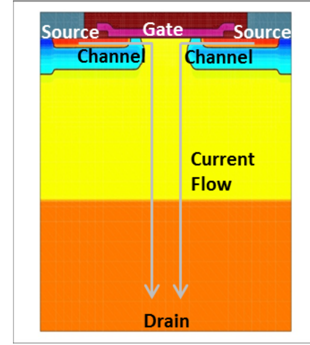

Fig. 6. Cross-sectional view of the 600 V class VDMOSFET used as a Q1 device in Fig 5.

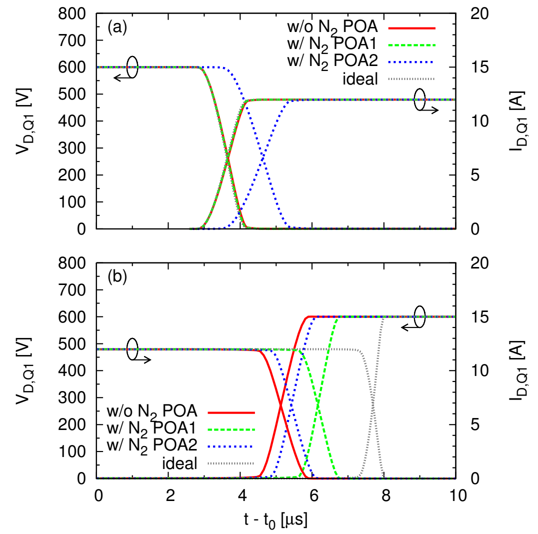

Fig. 7. (a)Turn-on and (b)turn-off waveforms of the test circuits with different VDMOSFETs.

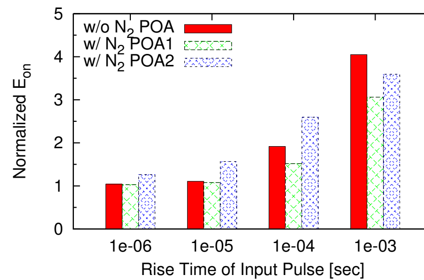

Fig. 8. Gate pulse rise time dependence of the normalized turn-on energy losses.

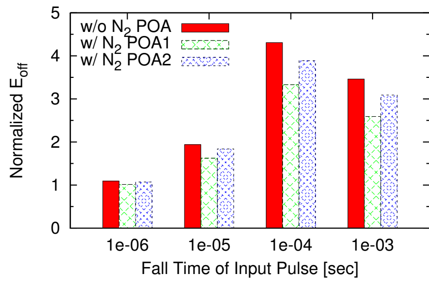

Fig. 9. Gate pulse fall time dependence of the normalized turn-off energy losses.

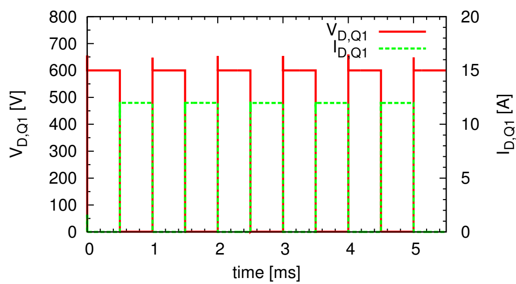

Fig. 10. Entire simulated waveforms of the VDMOS1's drain voltage and current. Totally five cycles of the gate on/off pulses are applied.

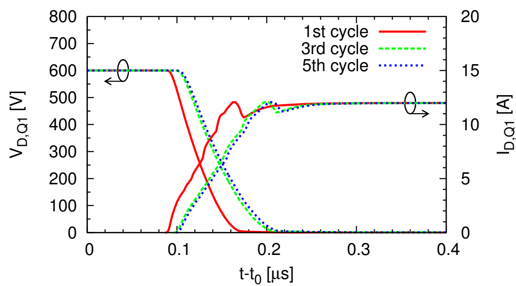

Fig. 11. Overlaid turn-on waveforms of the VDMOS1's drain voltage and current.

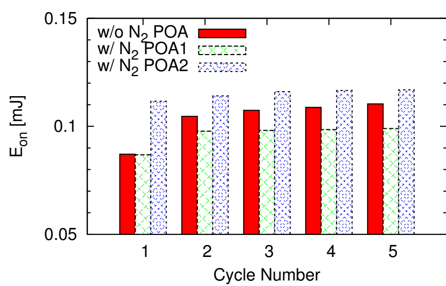

Fig. 12. Cycle number dependence of the turn-on energy losses.

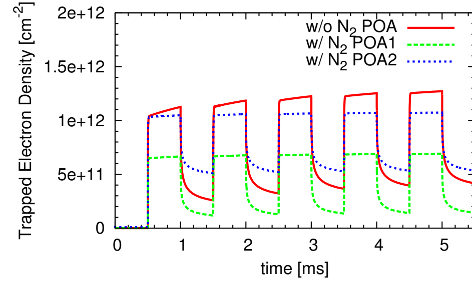

Fig. 13. Transient characteristics of the interface trapped electron at the center of VDMOSFET channel.