TCAD modeling challenges for 14nm FullyDepleted SOI technology performance assessment

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***Abstract*— This paper reviews the main challenges for the TCAD of 14nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology performance assessment. Thanks to a multi-scale approach combining extensive electrical characterization and advanced solvers simulations, ensuring deep physical insight, we provide TCAD simulation framework for device layout optimization, strain engineering and device reliability assessment.**

I. INTRODUCTION

To ensure fast cycle time, 2D process and device Technology Computer Aided Design (TCAD) simulations requiring excellent calibration of empirical model within the advanced CMOS technology development. In the frame of 14nm Fully Depleted Silicon-On-Insulator (FDSOI) [1], we have developed a methodology based on multi-scale modeling tools and extensive electrostatic and transport properties characterization. The performance of planar Ultra-Thin Body and Box (UTBB) FDSOI technologies have been demonstrated in [1] [2]. These technologies offer an excellent control of the device electrostatics and benefit of back-biasing capabilities. Moreover, by means of new materials and smaller dimensions, 14nm FDSOI technologies offer comparable performances as FinFET technologies. This paper reviews the main results of the multi-scale approach developed to achieve accurate TCAD simulation, from process and mechanical simulations, mobility and current calculation to device reliability modeling.

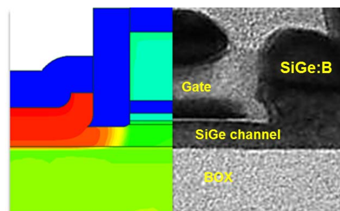

Fig. 1. TEM cross-section superimposed to process 2D TCAD simulation of 14nm pMOS FDSOI device featuring raised SiGe:B source/drain.

II. TECHNOLOGY DESCRIPTION & SIMULATION

The 14nm dual work-function, HighK/Metal Gate-First FDSOI technology has been largely detailed in [1], [3]. The high concentration c-SiGe channel of the pMOS is obtained by Ge condensation. The dual-work function is achieved thanks to native silicon channel nMOS and high concentration (25%) strained SiGe channel on pMOS providing 80mV shift work-function with single TiN metal gate on HfO2 gate dielectric. Tensile SiCP and compressive SiGeB raised source/drain are epitaxied on nMOS and pMOS respectively. Final device is represented Fig. 1.

A. *Modeling of the gate stack*

The modeling of the work-function (WF) in HfO2 gate stack is challenging because doping, capping, anneals are used to adjust the incorporation of nitrogen and oxygen through the gate stacks. The meaningful results provided by the first-principle Ab-initio calculations reported in [7] complement well the cSiGe WF k.p calculations of [6] that account for quantization effects with Vg and Tsi. In-line characterization techniques based on x-ray diffraction (XRD) combined with TCAD simulations are currently in development to determine the WF.

B. *Modeling of Strain*

The formation of bi-axially strained SiGe pMOS channels by condensation process leads to homogenous SiGe layers with high concentration and compressive stress exceeding 2 GPa . When combined with uni-axially strained raised SiGe source/drain, it requires a rigorous 3D mechanical simulation methodology to obtain realistic and layout dependent simulations [8], [9].

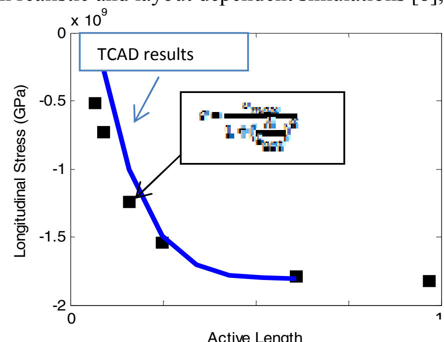

Fig. 2. Extracted stress values (symb.) to match electrical measurements and comparison to TCAD predictions averaged over the active length (lines).

As illustrated Fig. 2 analytical expression of the stress in the channel as function of the distance to the STI is extracted from 3D layout-dependent mechanical simulations and is reused in process and device TCAD simulations.

III. DEVICE MODELING

Modeling of transport in 14FD devices requires accurate description of the mobility. For this purpose, for stress dependent behavior and for each scattering mechanism (phonon surface roughness, remote coulomb, …) a multi-scale modeling approach based on advanced transport solvers such as quantum Non-Equilibrium Green’s Functions (NEGF) [10], Multi Subband Monte Carlo (MSMC) [11] and the Kubo-Greenwood (KG) approach [12] has been developed. The models must be calibrated accounting that the technology features 2 interlayer

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oxide (IL) thicknesses for logic and analog devices and that the electrostatic of the device is tightly controlled by silicon-body thin film thickness (Tsi).

A. Back-biasing

Among the key benefits of the UTBB FDSOI technology is the possibility of applying a high positive or negative back bias to boost dynamic performance of the circuit w.r.t application or to compensate device centering [1]. In forward regime ($V_B>0$ for nMOS and $V_B<0$ for pMOS), it reduces the threshold voltage yield to increase of the ion current. In backward regime ($V_B<0$ for nMOS and $V_B>0$ for pMOS), it increases the threshold voltage and reduce the leakage current. Additionally, front and back interfaces inversion can be controlled by the back-bias [13], [14]. Fig. 3 shows typical threshold voltage shifts as a function of back biases.

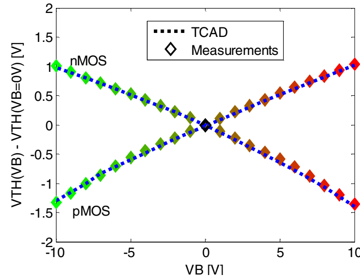

Fig. 3. Threshold voltage for various back biases ranging from -10V to 10V per steps of 2V in n – pMOS devices (Tinv=2.65nm, Tsi=7.5nm, T=300K).

B. Stress-Dependent Mobility Modeling

For the high value of stress applied in 14FD devices, non-linear piezo approach such as MCMob is required [13] [16]. It is a stress-dependent mobility model implemented in Sentaurus Device simulator using a six-order polynomial fit of the electron and hole mobility variation along the channel direction. MCMob model parameters calibration can be found in literature [16]. However, simulations in strained silicon have been performed using 3D k-space Monte-Carlo simulations [16], and the impact of the vertical electric field on the subband structure was not accounted. Significant dependencies on the normal electric field on the mobility variation vs. strain are indeed observable for electrons and holes both in measurements and using advanced solved as described in [5].

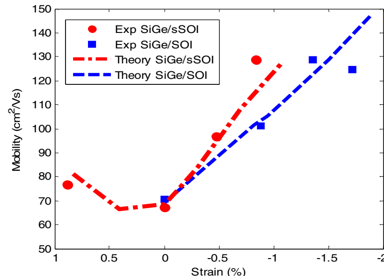

Fig. 4. Measurements and UTOXPP simulations of hole mobility as a function of biaxial strain obtained with various Ge contents. Mobility extracted at a vertical field of 0.5MV/cm. Split CV measurements performed in the linear regime in SiGe-based PFDSOI devices implemented on SOI and tensile sSOI substrates.

For that reason, it is preferable to use Kubo–Greenwood mobility calculations based on 1D self-consistent Poisson *k.p* Schrödinger simulations as reported in [13]. In strained SiGe materials, Kubo Greenwood simulations accounting for alloy-scattering and strain can also be used. Typical results for holes are shown in Fig. 4. The impact of strain and Ge content is de-embedded using tensile strained sSOI wafers, leading to higher Ge content for the same stress level as in SOI wafer.

C. Low field Mobility

The mobility in high-k/MetalGate FDSOI devices is limited by a complex combination of scattering mechanisms: the presence of high-k dielectrics induces mobility degradation through Remote Coulomb (RC) [17], Remote Phonon (RP) [18] and Remote Surface Roughness scatterings (RSR) [19]. Moreover, phonon and Surface Roughness (SR)-limited mobility are strongly dependent on the channel thickness (Tsi) [20]. Additionally, it has been demonstrated that mechanisms limiting the mobility can highly depend on the voltage applied on the front and the back gates [12] as testified by Fig. 5. Full quantum NEGF solvers, describing scattering sources geometrically, have been used to confirm the validity of KG solvers applied to highly confined FDSOI structures [13].

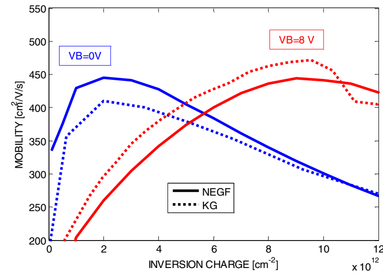

Fig. 5. Effective electron mobility (including PH, SR and RC scattering mechanisms) in silicon at VB=0V and VB=8V. Comparison between NEGF and KG results. Parameters for SR: exponential SR autocorrelation with ΔSR=0.47 nm and Λ=1.3 nm for NEGF and ΔSR=0.62 nm and ΛSR=1.3 nm for KG.

Based on these much faster KG simulations, each TCAD mobility model parameters can be adjusted on a large set of geometries, temperatures, and scattering mechanisms as presented e.g. in Fig. 6 for RC in n and p-devices featuring various IL thicknesses [13].

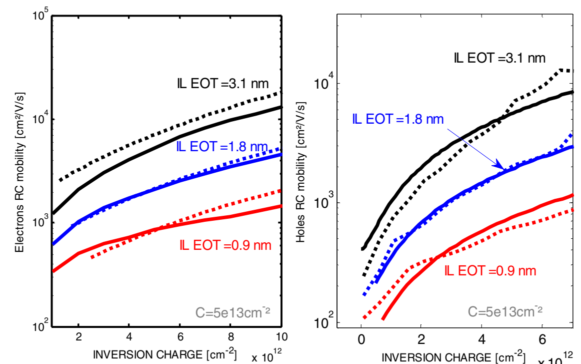

Fig. 6. nMOS (left) and pMOS (right) effective RC electron mobility in FDSOI devices as a function of the inversion charge. KG (dashed) and TCAD (lines) simulations are performed for various IL EOT for a fixed interface charge concentration C=5e13cm-2. Tsi=7.5 nm; T=300 K.

Such a multi-scale approach [13] leads to TCAD models in agreement with split-CV mobility measurements performed in nMOS and pMOS for various interfacial charge densities, IL thicknesses and temperatures as summarized in Fig. 7 and Fig. 8.

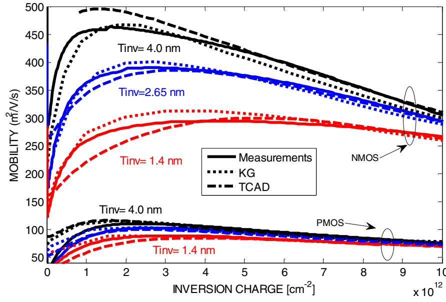

Fig. 7. n- and pMOS mobility as a function of the inversion charge for structures with various IL EOT. Comparison between TCAD, KG solvers and experiments.

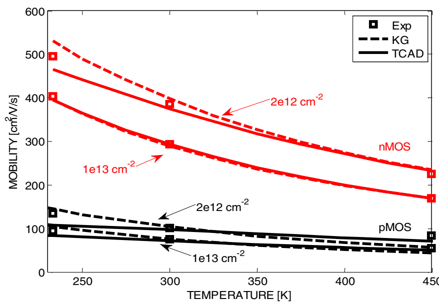

Fig. 8. n- and pMOS mobility as a function of the temperature at fixed inversion densities (2e12 cm-2 and 1e13 cm-2). Comparison between TCAD, KG solvers and experiments. Tinv=2.65 nm; Tsi=7.5 nm..

IV. ACCESS RESISTANCES

Nanoscale Bulk, FinFET and FDSOI MOS device performance enhancement is synonymous of channel length reduction and of channel mobility engineering [13]. Nevertheless, for nominal devices, the weight of the access resistance in the total MOS resistance increases [21].

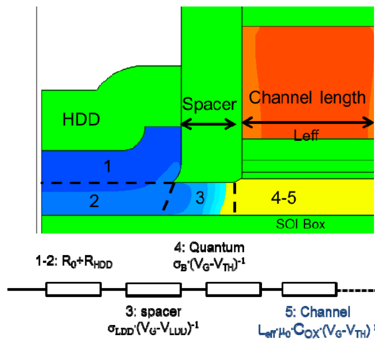

Fig. 9. Resistive network with Vg and L dependencies. The equivalent threshold voltage VLdd of the spacer resistance can be different from the transistor one Vth.

The total MOS transistor resistance can be seen as a Vg and Vd dependent resistive network as described as in Fig. 9.

A. Quantum resistance

As reported in [22] the total device resistance includes a quantum resistance, due to the finite number of available sub-bands [24]. This quantum resistance exhibits a $1/V_G$ dependence, and is of the order of 10-20 Ω.V.µm [23] leading to about 10% decrease of linear current in typical 14nm-like devices.

B. Role of spacer region

Based on device simulations of the gradient of pseudo-Fermi levels, the local resistive path can be monitored as plotted Fig. 10. Both TCAD and NEGF results reveal that a significant voltage drop occurs in the spacer region, while the channel region exhibits a nearly linear trend (the slope of which is proportional to the channel mobility). Following the formulation of [23] and the observation of [22] we verify that due to this highly resistive spacer region, the access resistance exhibits additional $1/V_G$ dependence. This is of major importance for accurate modeling of the device performance and cannot be ignored to interpret split C-V mobility measurements in short devices [22].

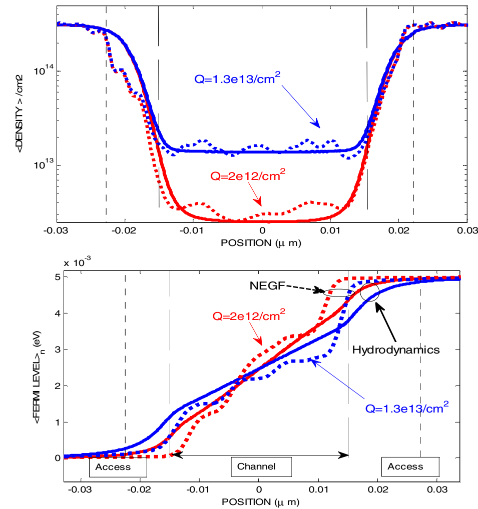

Fig. 10. Charges and Fermi Level along the channel for two gate voltage simulated using NEGF and TCAD solvers.

C. Device layout optimisation

Based on the multi scale approached developed, TCAD tools featuring state-of-the-art stress-dependent models compare favorably with measurements (Fig. 11) and can be used for device layout optimization.

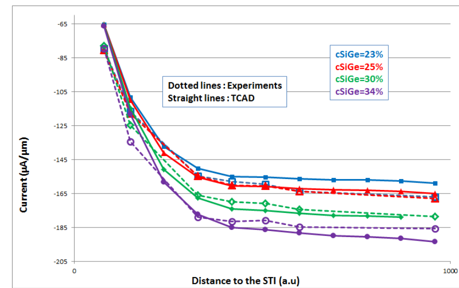

Fig. 11. pMOS measured and simulated linear current at constant Vg-Vth for SiGe channel concentration ranging from 23% to 34% as function of active length .

V. HOT CARRIER DEGRADATION

Dangling silicon bonds at the Si–SiO_2 interface are passivated by hydrogen, however hot carrier degradation and depassivation processes can occur when the device is operating in the On state regime. Device aging can be modeled using the Reaction and Diffusion theory [24]. Typical ID-VG curves obtained for various Hot carrier degradation times can be seen in Fig. 12. The extracted gate voltage at constant Drain current is reported in Fig. 13 as a function of degradation time.

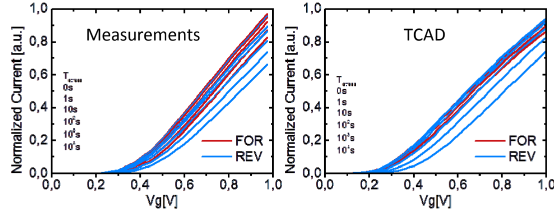

Fig. 12. Measurements and TCAD simulations of Drain current in saturation for various Hot carrier degradation times. Forward and reverse (Source and Drain inverted) regimes are investigated to emphasize defect localisations.

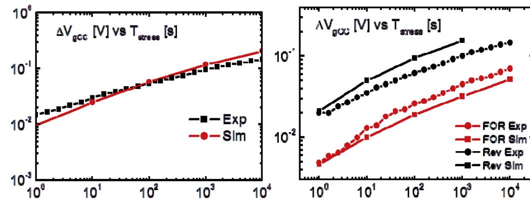

Fig. 13. Degradation time dependencies of the Gate Voltage at constant Drain current in linear (left) and saturation (right) regimes.

VI. VARIABILITY

Since FDSOI features low-doped channel, it is expected to present lower statistic variability than bulk technologies featuring heavily doped channel. In 14FDSOI, the sources of variability that must be accounted for are the classical Random-Dopant Fluctuation (RDF), Metal Gate Granularity, Line Edge Roughness, Width Roughness. Because of this role on the device electrostatic, the Inter-Layer, HK layers and Silicon film thickness roughness must be accounted for introducing a local variation of electrostatic potential and of the mobility. Statistical variability (SV) of typical 22nm FDSOI based on 3D atomistic simulations of are reported in [25] showing competitive advantage of FDSOI w.r.t RDF in sub-threshold regime. SV investigation in saturation regime and accounting for device degradation are discussed in [26] and would require detailed technology description for further comparison against measurements.

CONCLUSION

In this paper, we have shown how the methodology based on complementary electrical measurements and multi-scale modeling simulations could supply to the main challenges for TCAD assessment of 14nm FDSOI device performance.

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REFERENCES

[1] M.Haond "Fully Depleted SOI : Achievements and Future Developments ", invited talk EURSOI 2014 conference

[2] N. Planes et al, "28nm FDSOI Technology Platform for High-Speed Low-Voltage Digital Applications", Symposium of VLSI Technology, p. 133, 2012

[3] O.Weber, "14-nm FDSOI Platform Technology for High-Speed and Energy-Efficient Applications", Symposium of VLSI Technology, 2014

[4] O.Nier "Experimental and physics-based modeling of transport in thin body, strained Silicon-On-Insulator transistors for ultra low power CMOS technologies" GE 2014

[5] O.Nier "Limits and improvements of TCAD piezoresistive models in FDSOI transistors" ULIS Conference 2013

[6] A. Soussou "Understanding Ge impact on VT and VFB in Si1-xGex/Si pMOSFETs"., Microelectronic Engineering 109, 2013 .

[7] C.L Hinkle "Interfacial oxygen and nitrogen induced dipole formation and vacancy passivation for increased effective work functions in TiN/HfO2 gate stacks", JAP, 2010

[8] Andrieux et al. "Strain and Layout Management in dual Channel (sSOI substrate, SiGe channel) planar FDSOI MOSFETs" ESSDERC 2014

[9] B. DeSalvo "A mobility enhancement strategy for sub-14nm power-efficient FDSOI technologies" IEDM 2014

[10] Y. M. Niquet et al., "Quantum calculations of the carrier mobility: Methodology, Matthiessen's rule, and comparison with semi-classical approaches", Journal of Applied Physics, 115(5), 054512 (2014)

[11] D. Esseni, P. Palestri and L. Selmi, « Nanoscale MOS Transistors: Semi-Classical Transport and Applications », Cambridge Univ. Press (2011).

[12] D. Rideau et al., "Mobility in high-K metal gate UTBB-FDSOI devices: From NEGF to TCAD perspectives". IEEE IEDM, p.328, 2013

[13] O.Nier "Multi-scale strategy for high-k metal gate UTBB-FDSOI Devices modeling with emphasis on Back Bias impact on mobility", Journal of Computational Electronics 12.4 (2013): 675-684.

[14] F.G. Perreira "Modeling study of the mobility in FDSOI devices with a focus on near-spacer-region", ULIS 2015.

[15] Manuals Adavanced Calibration for Device Simulation from Synopsys Inc., Version K-2015.06.

[16] F. M. Bufler, A. Erlebach, and M. Oulmane, Symmetry Reduction by Surface Scattering and Mobility Model for Stressed <100>/(001) MOSFETs," SISPAD 2010

[17] Cassé, Mikaël, et al. "Carrier transport in HfO2/metal gate MOSFETs: physical insight into critical parameters." Electron Devices, IEEE Transactions on 53.4 (2006): 759-768

[18] Toniutti, P., et al. "On the origin of the mobility reduction in n-and p-metal–oxide–semiconductor field effect transistors with hafnium-based/metal gate stacks." Journal of Applied Physics 112.3 (2012): 034502-034502

[19] Gamiz, F., and J. B. Roldan. "Scattering of electrons in silicon inversion layers by remote surface roughness." Journal of applied physics 94.1 (2003): 392-399.

[20] Rideau, D., et al. "Mobility in FDSOI Devices: Monte Carlo and Kubo Greenwood Approaches Compared to NEGF Simulations." Proc SSDM 2012

[21] Kim et al , IEEE TED, Vol. 49, N° 3, March 2002.

[22] D. Rideau et al. "Experimental and theoretical investigation of the 'apparent' mobility degradation in Bulk and UTBB-FDSOI devices: a focus on the near-spacer-region resistance." SISPAD 2014

[23] F. Monsieur et al: The importance of the spacer region to explain short channels mobility collapse in 28nm Bulk and FDSOI technologies", ESSDERC 2014

[24] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation,"Microelectronics Reliability, vol. 45, no. 1, pp. 71–81, 2005.

[25] S. Markov, C. Binjie and A. Asenov, "Statistical Variability in Fully Depleted SOI MOSFETs Due to Random Dopant Fluctuations in the Source and Drain Extensions", IEEE Electron Device Letters, vol. 33, no. 3, pp. 315-317, 2012M. Zilli et al., Electron Device Lett. 28, 1036 (2007).

[26] L.Gerrer "3D Atomistic Simulations of Bulk, FDSOI and Fin FETs Sensitivity to Oxide Reliability" SISPAD 2014