High-Accuracy Estimation of Soft Error Rate using PHYSERD with Circuit Simulation

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***Abstract*—Soft error simulations utilizing PHYSERD are presented. The comparison with the experimental data for 28 nm SRAM demonstrates that PHYSERD provides the high-accuracy estimation of soft error rate when combined with circuit simulation, while PHYSERD alone tends to overestimate soft error rate. We also analyze the contributions of transistors constituting SRAM and of secondary ions to soft error rate. We find that circuit simulation has a significant effect on these contributions and is essential to the prediction of soft error rate.**

I. Introduction

Terrestrial neutron-induced single event upset (SEU) remains one of the major concerns in the field of the semiconductor device reliability. This is because of the increase in memory sizes of products and the decrease in a critical charge, which is a minimum charge required for SEU. Predicting soft error rate (SER) with high accuracy is strongly desired because SER depends on a device layout and a circuit balance, both of which can not be altered after the implementation of circuits. Many efforts have been devoted to developing simulation systems to meet such demand [1]. Recently, Abe *et al.* have developed multi-scale Monte Carlo simulation system, named PHYSERD (PHits-HYenexss integrated code System for Effects of Radiation on Devices) [2], [3]. Since this system includes both a particle transport code (PHITS) and a 3D-device simulator (HyENEXSS), it is capable of dealing with any radiation environments and various mechanisms of charge collections [4], [5]. However, the accuracy verification of this system has not been completed. Moreover, there is some uncertainty about the effect of circuit characteristics because PHYSERD adopts a critical charge (Q_{crit}) method, where whether an upset occurs or not is determined by comparing the amount of collected charge with pre-estimated Q_{crit}.

This work evaluates the accuracy of the simulation system by comparing with the experimental data for SRAM fabricated in a 28 nm CMOS process and investigates the effect of circuit characteristics on the estimation of SER by incorporating the additional analysis of circuit simulation into PHYSERD. The contributions of transistors constituting SRAM and of secondary ions to SER are also analyzed.

II. Simulation Setup

Figure 1 shows simplified simulation flows of original PHYSERD (referred to as the Q_{crit} method) and PHYSERD with circuit simulation (referred to as the waveform method), where whether an upset occurs or not is determined by a voltage transition obtained through circuit simulation. Device geometries are designed based on the actual layout of the SRAM cell of the 28 nm node. Calculations are carried out separately for NMOS and PMOS, which correspond to driver and load transistors, respectively. The total SER can be calculated as the sum of contributions from NMOS and PMOS.

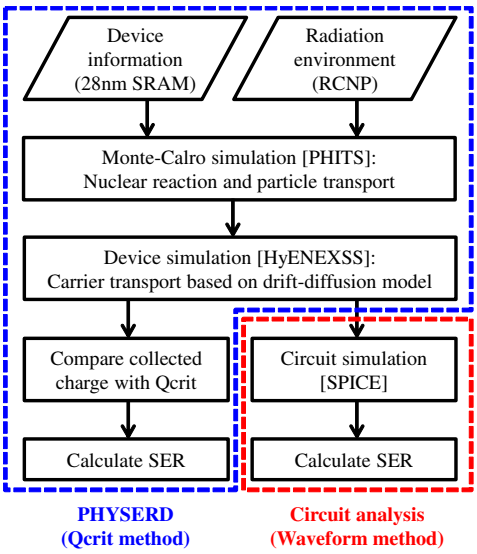

Fig. 1. Simplified simulation flows of original PHYSERD (Q_{crit} method) and PHYSERD with circuit simulation (waveform method). The detailed simulation flow of PHYSERD is described in Ref. [3].

To compare simulated SER with the experimental one fairly, we employ the energy spectrum of neutrons at the experimental facility, which is Research Center for Nuclear Physics (RCNP) at Osaka University. The energy spectrum spans the range between 1.5 MeV and 398 MeV. The simulation structure used in PHITS calculation is composed of a silicon substrate and wiring layers and has the same size as the experimental chip. Neutrons are irradiated normal to the chip surface from the side of the wiring layer in both experiments and simulations. The nuclear reaction model used in PHITS is INCL + GEM for neutrons above 20 MeV [6]. As for neutrons below 20 MeV, the event generator mode with the nuclear data library JENDL-4.0 is employed.

In the case of the Q_{crit} method, Q_{crit} is preliminarily determined for NMOS and PMOS using circuit simulation with the transient current model,

$$I(t) = \frac{Q}{\tau_1 - \tau_2 - a\tau_3}\left[\mathrm{e}^{-\frac{t}{\tau_1}} - \mathrm{e}^{-\frac{t}{\tau_2}} + a\mathrm{e}^{-\frac{t}{\tau_3}}\right], \quad (1)$$

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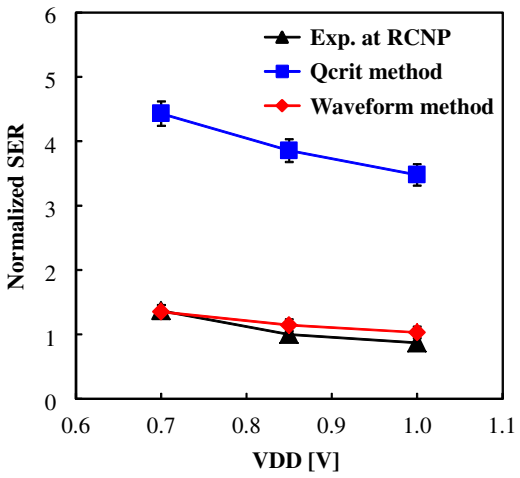

Fig. 2. Measured and calculated SERs as a function of VDD for 28 nm SRAM. SERs are normalized by the experimental value at 0.85 V. Error bars correspond to standard errors.

where Q denotes the amount of charge collected in this model. $\tau_{1,2,3}$ and a are fitting parameters and extracted from transient current waveforms obtained by device simulation for several secondary ion strikes. This model is the extended version of the double-exponential current model described in Ref. [7]. In both methods, load capacitances and resistances are estimated using circuit simulation and taken in device simulation to fully consider circuit characteristics.

III. Results and Discussions

A. Comparison between Simulation and Experiment

Figure 2 shows the VDD dependences of SER obtained by experiments and simulations. SERs are normalized by the experimental value at 0.85 V. Results of the waveform method demonstrate good agreement with experimental results. On the other hand, SER calculated by the Q_{crit} method is more than three times higher than experimental results.

To explore the reason for this difference between two methods, we focus on charge collections induced by secondary ions. Figure 3 shows time evolutions of charge collections for SEU events in NMOS at 0.85 V. Figs. 3 (a) and (b) correspond to SEU events in Q_{crit} and waveform methods, respectively. Blue lines are events which cause SEU in both Q_{crit} and waveform methods. Red lines are events which cause SEU in the Q_{crit} method but not in the waveform method. Note that there is no event causing SEU only in the waveform method. Blue lines show rapid increases compared to red lines in Fig. 3. Thus, it can be said that the Q_{crit} method includes extra events with slow charge collections in SEU events and this is the reason for the overestimation observed in Fig. 2.

The time elapsed between an ion strike and a data upset is extracted from SEU events obtained through the waveform method. Figure 4 shows average times to upsets for NMOS and PMOS, where zero time corresponds to the moment of a secondary ion strike. These times are shorter than the duration of charge collections observed in Fig. 3. This indicates that charges collected after these times are not attributed to SEU.

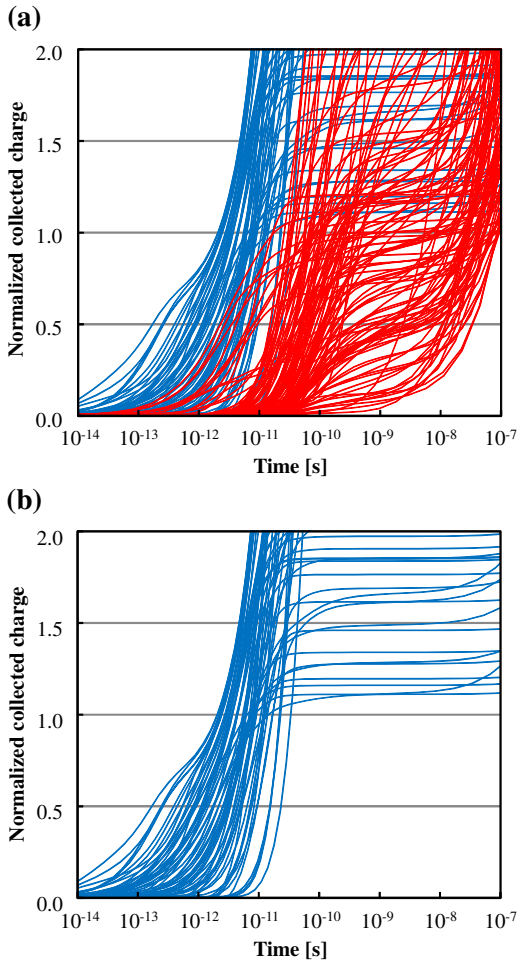

Fig. 3. Time evolutions of charge collections for SEU events in NMOS at 0.85 V. The upper (a) is for the Q_{crit} method and (b) is for the waveform method. Blue lines correspond to events which cause SEU in both Q_{crit} and waveform methods. Red lines correspond to events which cause SEU in the Q_{crit} method but not in the waveform method. Collected charges are normalized by Q_{crit} of NMOS.

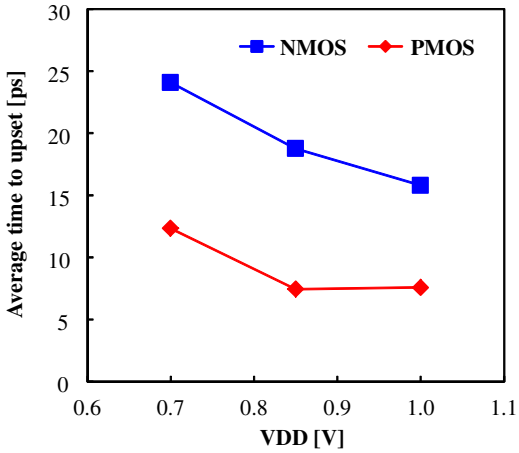

Fig. 4. The average times to upset of NMOS and PMOS. Zero time corresponds to the moment of a secondary ion strike.

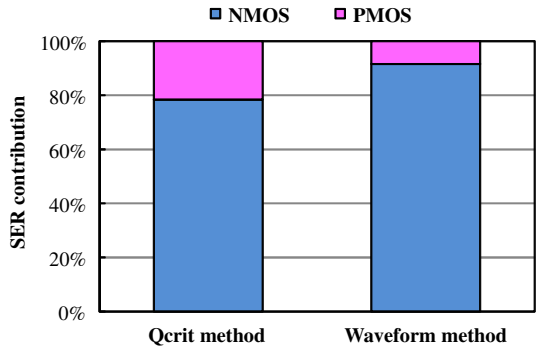

Fig. 5. SER contributions of NMOS and PMOS in Q_{crit} and waveform methods at 0.85 V.

This is because when charge collections occur in SEU-sensitive NMOS (PMOS), paired PMOS (NMOS) acts to compensate the voltage fluctuation. If the charge collection is slow, the paired transistor can stabilize the voltage of the affected node. In such a case, the charge collection does not result in SEU even though the total collected charge exceeds Q_{crit}. On the other hand, if the charge collection is fast, the paired transistor can not complete the voltage stabilization before the data is flipped. Such a charge collection causes SEU corresponding to each event shown in Fig. 3 (b). It is therefore important for the accurate SER estimation to consider the compensable time-period, which is roughly defined as the period after the moment shown in Fig. 4.

Since the Q_{crit} method almost lacks the factor of time and determines whether SEU occurs or not by comparing a total collected charge with Q_{crit}, the effect of the compensable time-period can not be considered. This leads to the overcounting of SEU events because the total collected charge contains charges collected during the compensable time-period. Consequently, events with a slow charge collection are included in SEU events, as seen in Fig. 3 (a).

B. Contribution of NMOS and PMOS

Figure 5 shows the ratio of contributions from NMOS and PMOS to SER for Q_{crit} and waveform methods at 0.85 V. It is obvious that the PMOS contribution in the Q_{crit} method is larger than that in the waveform method. In the case of the Q_{crit} method, these ratios are mainly determined by differences in Q_{crit} and a sensitive area, which is the area of nodes that can cause SEU by collecting charges, between NMOS and PMOS. In addition to these factors, the difference in the compensable time-period between NMOS and PMOS affects their relative contributions to SER in the case of the waveform method. As seen in Fig. 4, the time to upset of NMOS is longer than that of PMOS. This is due to the difference in the driving power: NMOS has higher driving power than PMOS. The shorter time of PMOS represents the immediate voltage compensation by NMOS leading to the suppression of SEU in PMOS. This mechanism is the reason for the discrepancy between two methods, observed in Fig. 5. The difference in the driving power is partly considered in the parameter Q_{crit} by estimating Q_{crit} using circuit simulation. However, this is not sufficient because the transient current model of Eq. 1 can not express a wide variety of responses in the charge collection.

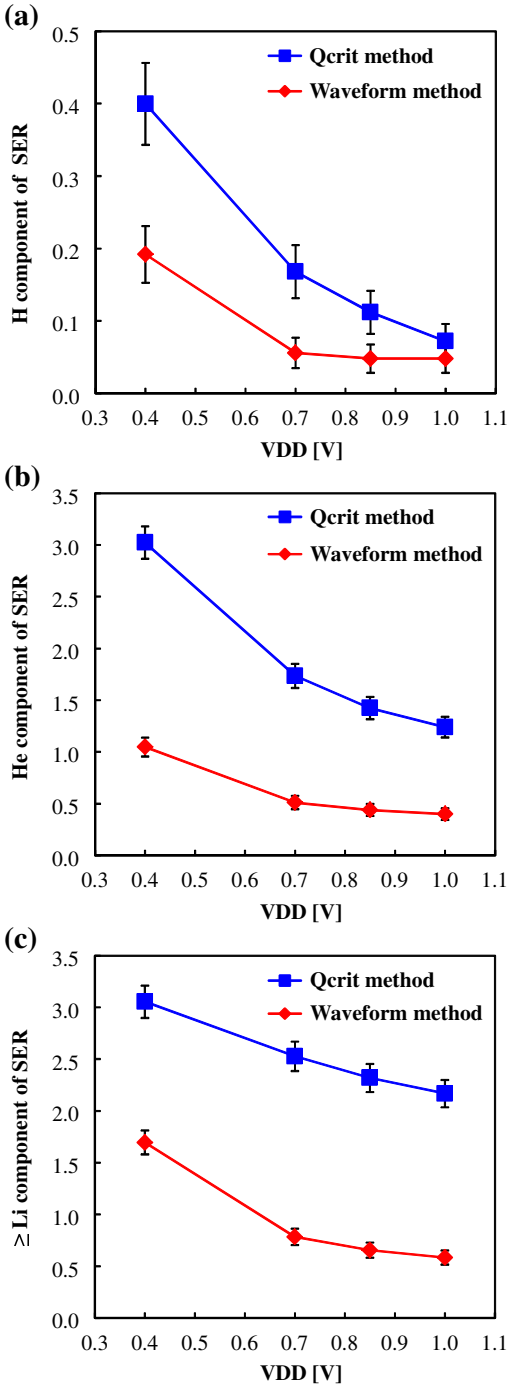

Fig. 6. (a) H, (b) He and (c) $\geq$ Li components of SER as a function of VDD. SERs are normalized by the experimental value at 0.85 V. Error bars correspond to standard errors.

C. Contribution of Secondary Ions

SER contributions of secondary ions are compared between Q_{crit} and waveform methods. For the purpose of investigating SRAM with a low Q_{crit}, SER at 0.4 V is additionally simulated. In this study, secondary ions are classified into three groups: (1) hydrogen, (2) helium and (3) lithium and above, and these are referred to as H, He and $\geq$ Li, respectively.

Figure 6 shows H, He and $\geq$ Li components of SER as a function of VDD for Q_{crit} and waveform methods. All components in the Q_{crit} method are larger than that in the waveform method. This is due to the effect of the compensable time-period as discussed in Sec. III-A. Comparing SER differences between two methods for these ions, the difference in the H component is smaller than that in other ions. One possible reason for this is that these ions have different linear energy transfers (LET), which is a unit expressing the amount of charges induced by a secondary ion per unit length. Since LETs of He and $\geq$ Li are comparatively high, these ions can deposit a large amount of charges in SRAM. In contrast, the LET of H is low resulting in the deposition of a small amount of charges. When considering the charge collection induced by a parasitic bipolar effect which causes a transient current by turning on of a parasitic bipolar transistor consisting of drain, well and source regions, the contribution of this effect is presumably small in the H component. The reason for this is that the bipolar effect is triggered by the potential fluctuation in the well region and H can not deposit enough charges to drastically disturb the well potential. Moreover, the parasitic bipolar effect causes relatively slow charge collections comparing to a drift mechanism. This is because in the case of NMOS, the potential fluctuation is induced by remaining holes in the well region and their diffusion to the well contact after the electron collection through the drift mechanism. Thus, the H component possibly consists of fast charge collections and the SER difference between two methods due to the effect of the compensable time-period is small resulting in the small discrepancy seen in Fig. 6 (a).

The ratios of contributions from secondary ions to SER are shown in Fig. 7. In the case of the Q_{crit} method (Fig. 7 (a)), the relative contribution of each ion monotonically depends on VDD. The percentages of H and He increase with decreasing VDD. On the other hand, in the case of the waveform method (Fig. 7 (b)), the relative contribution of each ion shows the non-monotonic dependence on VDD. This discrepancy reflects the SER differences between two methods for secondary ions as seen in Fig. 6. The difference in the relative contribution is significant at 0.4 V, where the percentages of H and He in the Q_{crit} method are clearly higher than those in the waveform method. These results suggest that circuit simulation plays an important role not only in the accurate estimation of SER but also in the analysis of the contributions from secondary ions.

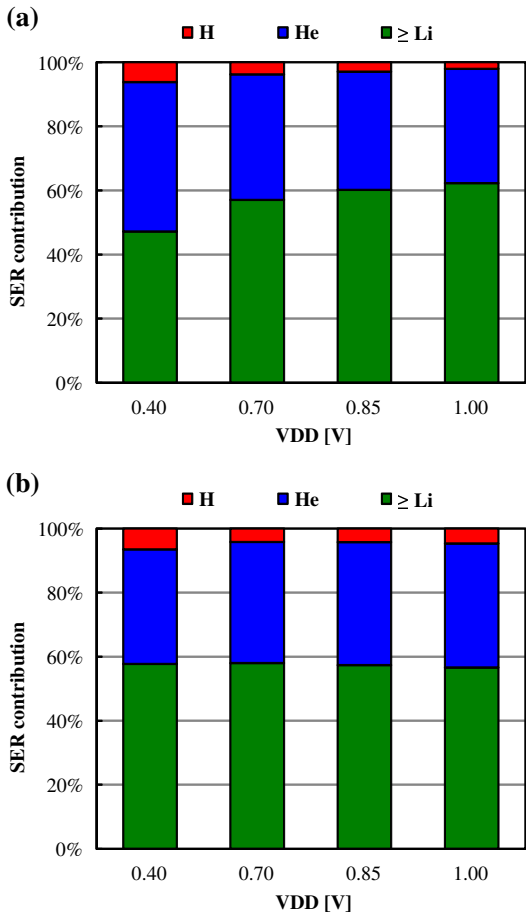

Fig. 7. SER contributions of secondary ions in (a) the Q_{crit} method and (b) the waveform method.

IV. Conclusion

We have presented the accuracy verification of PHYSERD and the impact of circuit simulation on the SER estimation. The results obtained by PHYSERD with circuit simulation have demonstrated good agreement with experimental data for 28 nm SRAM. On the other hand, the results obtained by PHYSERD alone overestimate SER by three times due to the lack of the voltage compensation mechanism, which is introduced by circuit simulation. We have also found that circuit simulation significantly affects the relative contributions of transistors constituting SRAM and of secondary ions to SER. We have concluded that PHYSERD with circuit simulation is a high-accurate approach to predict SER and useful for the realistic analysis of contributing factors to SER.

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