Compact Modeling of Carrier Trapping for Accurate Prediction of Frequency Dependent Circuit Operation

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***Abstract*—We have investigated the influence of carrier traps on device characteristics in TFTs. In particular, our focus was given on transient characteristics influenced by carrier trapping during device operations. A compact model for circuit simulation of TFTs has been developed by considering the time constant of the trapping. The model was verified with measured frequency dependent TFT characteristics.**

Keywords—TFTs; carrier traps; compact model; surface potential; transient charactersitics

I. INTRODUCTION (*HEADING 1*)

Thin-film transistors (TFT) have been applied for large area displays as well as for solar panels [1]. Our focus is given on the poly-crystalline silicon TFTs, for which it has been demonstrated that the laser annealed technique makes the device applicable even in the high-frequency operating range [2]. It is known that trap states located at the grain boundaries of the poly-silicon are still partly remained even after the annealing and captures carriers [3]. Our purpose is to achieve accurate prediction of TFT circuit performances under different switching operation conditions. For the purpose, we have experimentally characterized the transient behavior of the poly-silicon TFTs on focus of the traps. By analyzing the data, the time constant of the trap states causing frequency dependent switching performance is extracted. A compact model considering this time constant for circuit simulation is developed. It is shown that the rather long time constant of trapping events results in the history effect, similar to the effect caused by the remained accumulated mobile-charge in SOI-MOSFETs even after switching-off [4].

II. MEASUREMENT ANALYSIS

The studied TFT device structure is shown in Fig. 1 [2]. Fig. 2 shows measured I_d-V_g characteristics for two different devices (Device A and B) at V_d =0.1V with the same device size on a chip [5]. The reason for selecting the small V_d is to exclude the hot electron effect in our investigation. Clear differences in the I_d-V_g characteristics observed are the threshold voltage V_{th} shift and the degraded subthreshold slope (Device B). Even though the device size is the same, a big variation in the DC characteristics is obvious. Measured switching performances of the same devices (Device A and Device B) with the rise time of 10μs are shown in Fig. 3. For both devices, current decay is observed according to the duration of the applied bias. The decay is stronger for Device B, for which the I_d-V_g characteristic is strongly degraded.

It is known that a specific feature of TFTs is the high density of trap states located at the boundaries of crystallized grains. The current decay observed in Fig. 3 is attributed to the gradually increasing carrier trapping in accordance with the duration of the carrier injection into the substrate from the source. Therefore the different I_d-V_g characteristics of Device A and B are attributed to the different trap densities to be fulfilled. Fig. 4 shows that the same waveform is observed for pulse repetition without degradation of the current. This concludes that the trapped carriers are easily detrapped after the bias is released, causing no device degradation.

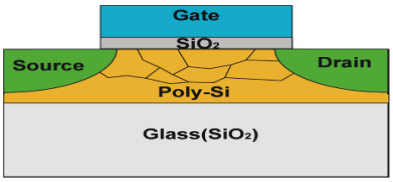

Fig. 1. Studied TFT structure fabricated with the ploy-Si substrate on glass. The device size is fixed to width/length=2μm/0.5μm for the present investigation.

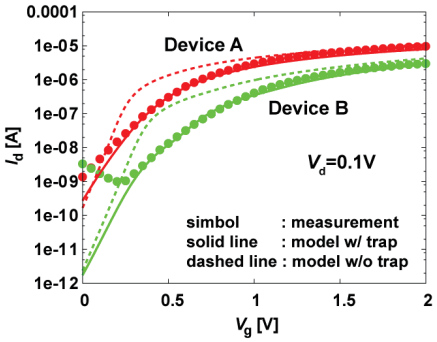

Fig. 2. Comparison of model calculation results with measurements at V_d for two different devices (Device A and Device B) as a function of V_g. Calculation results without trap densities are also depicted by dashed lines.

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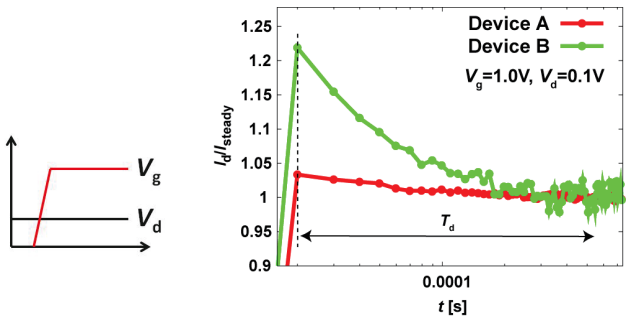

Fig. 3. Measured transient current response under constant drain voltage V_d of 0.1V. The currents are normalized by the saturation values. The measurement condition is shown in the left-hand-side figure. The rise time of switching is fixed to 10μs, which causes no non-quasi-static effect.

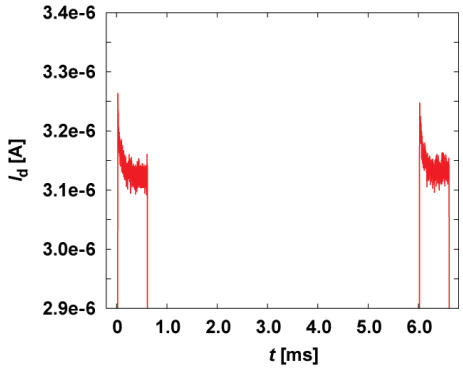

Fig. 4. Measured transient current response for repeated pulse input. The measurement condition is the same as that shown in Fig. 2.

III. Modeling and Calculation Results

The trap density distribution is usually approximated by a logarithmic function of the energy difference E_f-E_c

$$g_A(E) = g_c \exp\left(\frac{E - E_c}{E_s}\right) \qquad (1)$$

where g_c is the density at E_f-E_c=0, and the inverse of E_s is the slope of the density of state. We considered two independent trap-density distributions as schematically shown in Fig. 5: One represents the shallow trap density distribution and the other represents the deep trap density distribution [6]. Circuit simulators work only with node potentials. Therefore, the density-of-states must be integrated with respect to the energy and calculated as a function of E_f-E_c [7]

$$N_{trap-A} = N_0 \exp\left(\frac{E_f - E_C}{E_s}\right)$$
$$N_0 = g_c E_s \frac{\frac{kT}{qE_s}}{\sin\left(\frac{kT}{qE_s}\right)} \qquad (2)$$

where the elementary charge, Boltzmann constant, and the temperature in Kelvin are denoted by q, k, and T, respectively. The energy difference E_f-E_c can be written as a function of the surface potential ϕ_s to transform into a function of V_g [8,9],

$$E_f - E_C = -\left(V_{ds} - E_V - kTln\frac{N_V}{N_A}\right) + \left(\phi_s - E_C\right) \qquad (3)$$

Since ϕ_s increases as V_g increases, the E_f-E_c value approaches to zero according to the V_g increase. This leads the condition that carriers are mostly affected by traps with the shallow density-of-states under normal operation condition. Whereas the deep density affects device characteristics for small V_g values.

From DC measurements as depicted in Fig. 2, these trap-density distributions of Fig. 5 can be extracted. For the extraction the V_g dependent carrier trapping at different trap states described through the V_g dependent surface potential ϕ_s is inevitable. The trap density is then implemented in the Poisson equation to consider its overall effect in a self-consistent way as

$$\nabla^2\phi = \frac{q}{\varepsilon_s}\left(p - n + N_D - N_A + N_{trap\_D} - N_{trap\_A}\right) \qquad (4)$$

where the donor like trap density N_{trap_D} is ignored in this study and only N_{trap_A} is considered. Since the investigation here is done for the nMOSFET, the major carriers are electrons under normal operation conditions, and thus hole can be ignored. The compact model HiSIM solves the Poisson equation explicitly without any approximations [10]. The simulation speed is similar to the simple V_{th}-based models such as BSIM due to accurate derivation of analytical initial guesses for the surface potential ϕ_s calculation. Thus the influence of the trapped carrier is consistently considered not only on the carrier density but also such as mobility, which are determined by charges calculated with the potential values. The extracted trap density as a function of E_f-E_c is shown in Fig. 6 [5].

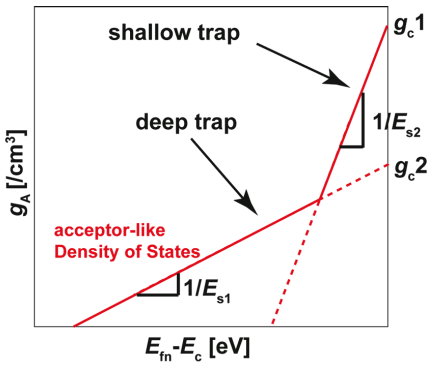

Fig. 5. Schematic of the trap density-of-states distribution used for our investigation, where E_{fn} is the quasi-Fermi level for electrons. Two independent density0of-states are depicted.

It is observed that carriers require time to be trapped by grain boundaries characterized by the capture cross section. The time constant T_d for trapping and detrapping process is modeled as the response delay as [11]

$$N_{trap}(t) = N_{trap}(t - \Delta t) + \Delta t / (\Delta t + T_d)\left(N_{trap}(V(t)) - N_{trap}(t - \Delta t) \right) \quad (5)$$

where $N_{trap}(t\text{-}\Delta t)$ is the trap density at previous time step of t-Δt. $N_{trap}(V(t))$ gives the trap density at the bias condition of $V(t)$ at time t. The second term on the right-hand-side equation describes the amount of the trap density increased within the time interval of Δt. The amount is dependent on whether trap states are easily captured or not, which is determined by T_d. The time constant T_d is extracted to reproduce measured transient characteristics shown in Fig. 6.

IV. Discussions

A. Frequency Dependent Trap Density-of-Sates

Fig. 7 shows different measured results for different devices on a chip with the same size of a different wafer from those shown in Fig. 2. Four measurements (I, II, III, and IV) show different features. As expected the I_d-V_g characteristics vary strongly from device to device, even though their device parameters are identical. Especially the normalized transient current (see Fig. 7c) shows two typical decay characteristics, the rapid decay and the slow decay. The transient current reduction is due to the gradually increasing carrier traps, which causes the reduction of the effective V_g. Device I possesses the minimum amount of trap densities both at the deep level and the shallow level. Three devices (II, III, IV) possesses clearly high density at the deep level recognized from the subthreshold shift. Two of the devices (II and III) have less shallow level trap densities, whereas Device IV has the high density-of-states both at the deep and the shallow levels. It is expected that the shallow trap levels can be easily captured during switching-on, whereas the deep levels takes time to be captured. Here after our focus is given on two devices (I and II) with two different transient features. The device I shows rapidly decaying feature, where as the device II shows gradually decaying feature.

Fig. 8 shows 2D-device simulation experiments. The trap density applied is kept the same as shown in Fig. 8a, and the capture cross section is varied (see Fig. 8b). For simplicity trap energy-level dependence of the capture cross section is ignored. It is seen that the observed different transient characteristics are reproduce as can be seen in Fig. 9. This concludes that the origin of the different normalized transient currents is attributed to the difference of the capture cross sections at different trap sites. It is seen that a large cross-section value can be attributed to a short time constant of the responsible traps, resulting in increased trapping during switching on.

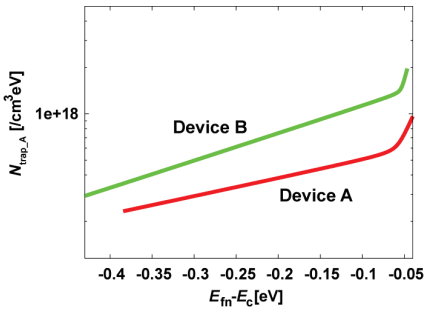

Fig. 6. Extracted trap density-of-states from Fig. 1 , where only N_{trap_A} is depicted.

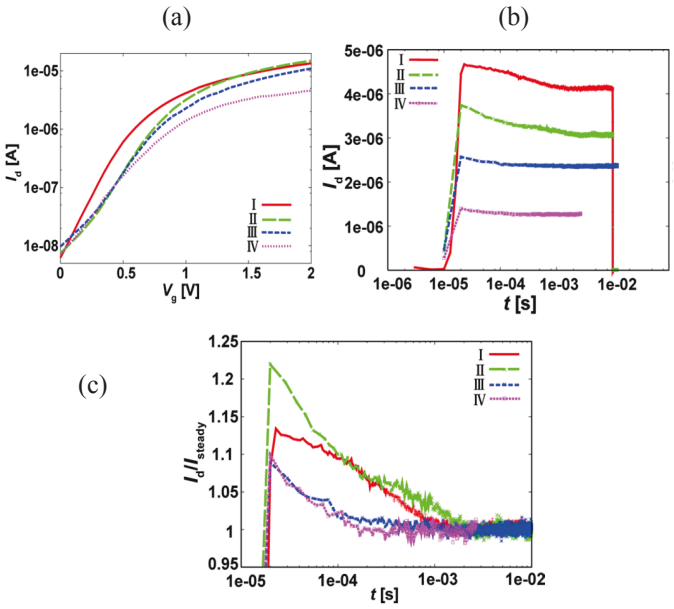

Fig. 7. Measured characteristics for four different devices on another wafer. The device size is fixed to W/L=0.5mm/2mm and the drain voltage is fixed to 0.1V. (a) Id-Vg characteristics, (b) transient characteristics, and (c) transient characteristics normalized by saturation currents.

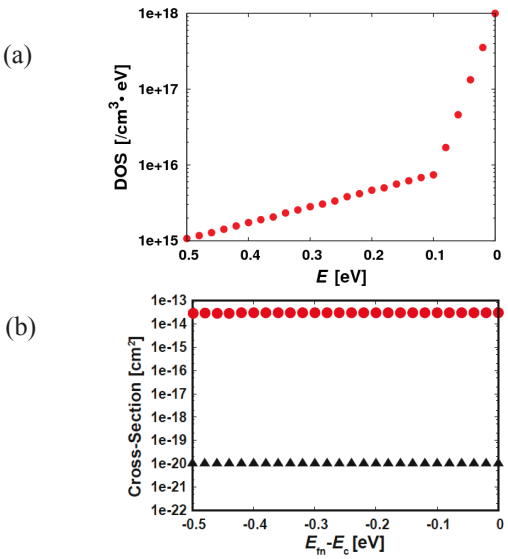

Fig. 11. 2D numerical device simulation results, (a) studied capture cross-section of trap sites, (b) simulated transient drain current as a function of time.

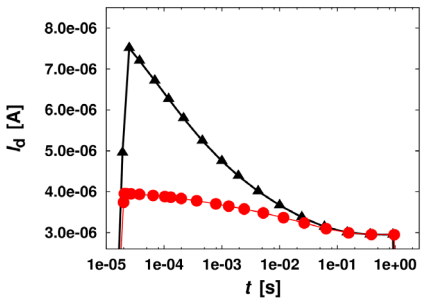

Fig. 9. 2D numerical device simulation results, (a) studied capture cross-section of trap sites, (b) simulated transient drain current as a function of time.

To model the feature of trap density-of-states, the time constant T_d applied for compact modeling of transient characteristics is rewritten with physical quantities as

$$T_d = \frac{A}{n \cdot v_{th,n} \cdot \sigma} \qquad (6)$$

where the capture cross section σ is modeled as a function of the energy level. The parameter A represents the trapping probability which is treated as a fitting parameter. Also included are: the cross-section of the trap density σ, responsible for the transient current characteristics, as well as the effects of the V_g dependence by the carrier density n calculated by HiSIM and of the temperature by the carrier velocity v_{th}. A constant σ for any trap energy level is applied for the 2D-device simulation results shown in Fig. 9.

B. Frequency Dependent Circuit Operation

Usually circuits operate under certain frequencies of repeating switch on/off conditions. Measured transient current characteristics are different for different frequencies applied as can be seen in Fig. 10a. For the measurement two different pulse durations are investigated: One is with very long duration of the V_g stress and the other is a relatively high frequency repetition of on/off. The long duration of the switched-on state leads to occupation of all trap states, and thus the current decay is obvious. However, the short duration can only induce mostly the occupation of shallow trap levels, which corresponds to a large cross section. This means also easy detrapping at the same time. The total tap density as a function of duration time is shown in Fig. 10b. It can be seen that the high frequency operation shows reduced degradation by trapping, while relatively slow switching demonstrates an obvious history effect. Since the deep trap density-of-states have small capture cross section, the current decay within a small stress time cannot be observed. This concludes that a constant trap density extracted from I_d-V_g measurements cannot predict the accurate switching performance of circuits. Inclusion of a time constant for trap occupation, resulting in a dynamic variation of the trapped charges, is the key to enable accurate simulation of TFT circuits.

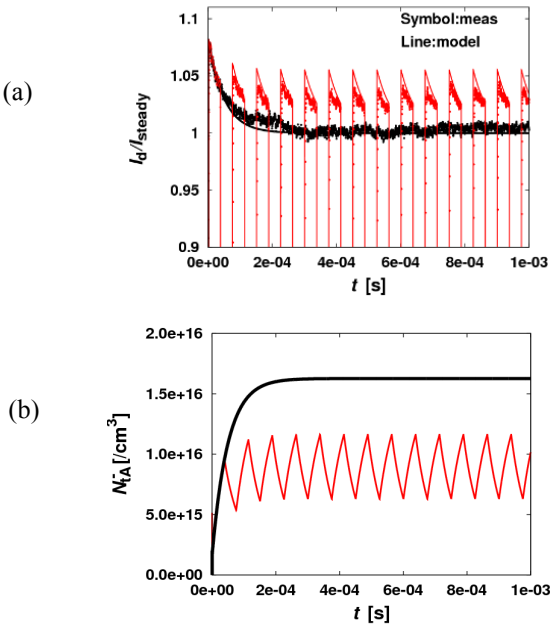

Fig. 10. (a) Comparison of measured transient drain current with the developed model for different frequencies, two different pulse durations with different frequencies, comparison to measurements. (b) Transient trap densities calculated for the transient current shown (a).

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