Multigate transistors:

Pushing Moore's law to the limit

J.-P. Colinge
TCAD Division, Taiwan Semiconductor Manufacturing Company (TSMC)
E-mail: jcolinge@tsmc.com

***Abstract*—Improvements in electrostatic channel control allow FinFETs and trigate FETs to extend Moore's law down to gate lengths of 15-20nm. Further scaling may require the better control that is provided by multigate devices. Using multigate FET architectures, gate length scaling down to 5 and 3 nm has been demonstrated experimentally and theoretically, respectively. At these dimensions, quantum confinement begins to appear and new effects such as drain current oscillations and tunneling through soft barriers can be observed. FET to SET and metal-semiconductor transitions resulting from quantum confinement present opportunities for new types of devices.**

Keywords— 1D confinement; multigate FET; GAA transistor, FinFET

I. INTRODUCTION

The semiconductor industry has relentlessly shrunk transistor size over the last 50 years, doubling integration density every 18 months (Figures 1 and 2).

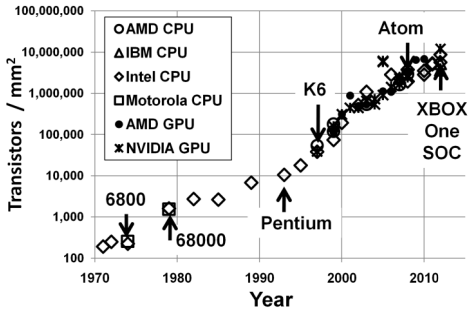

Figure 1. Evolution of the number of transistors per square millimeter with time. Microprocessors (CPU) and graphics processors (GPU) from different vendors are shown. Data from [1].

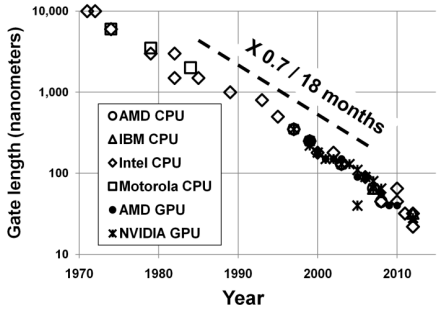

Figure 2. Evolution of the gate length with time [1].

The industry pushed the scaling of the bulk planar MOSFET to its limit, and was forced to move to new device architectures such as FinFETs, trigate FETs and ultrathin FDSOI devices, in order to cope with short-channel effect. The different existing gate architectures are shown in Fig. 3.

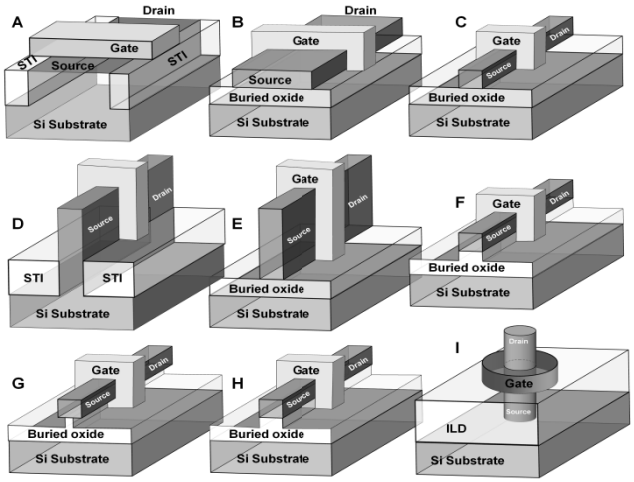

Figure 3: Different types of MOSFET gate configurations. A: Single-gate planar bulk MOSFET. B: Single-gate SOI MOSFET with mesa isolation. C: Triple-gate (trigate) SOI MOSFET with square cross section. D: Bulk trigate MOSFET with high aspect ratio (bulk FinFET). E: SOI trigate MOSFET with high aspect ratio (SOI FinFET). F: Pi-gate (Π-gate) SOI MOSFET. G: Omega-gate (Ω-gate) SOI MOSFET. H: Horizontal gate-all-around (GAA, quadruple-gate, quad-gate) transistor with square section. I: Vertical gate-all-around (GAA) MOSFET with circular cross section) [2,3,4,5,6,7].

II. ELECTROSTATICS

The electrostatics in the channel region of a MOSFET is governed by Poisson's equation:

$$\frac{dE_x}{dx}+\frac{dE_y}{dy}+\frac{dE_z}{dz}=\frac{\rho}{\varepsilon}=\text{a constant value}$$

which clearly shows that the electric fields in the 3 directions of space "compete" for any charge (even a zero charge) in the channel. The influence of the electric field in the x-direction, which causes short-channel effects, can be reduced by increasing the influence of the y and z components of the field (Fig. 4). Based on Poisson's equation it is possible, using a few simplifying assumptions, to calculate a parameter called the "natural length", λ, that represents the extension of the electric field lines from the source and drain in the channel region. A device will be free of short-channel

effects if the gate is at least 6 times longer than λ (Fig.5). For instance, in the case of a double-gate MOSFET, one can show that the subthreshold swing, *SS*, increases as gate length is decreased according to the following relationship, valid for $L_G > 2\lambda$ [8].

$$SS = \frac{k_B T}{q}\ln(10)\frac{1}{1-2\exp\left(-\frac{L_G}{2\lambda}\right)}$$

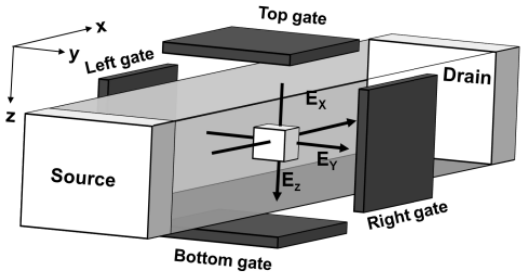

Figure 4. "Competition" between x, y and z components of the E-field in the channel region of a MOSFET.

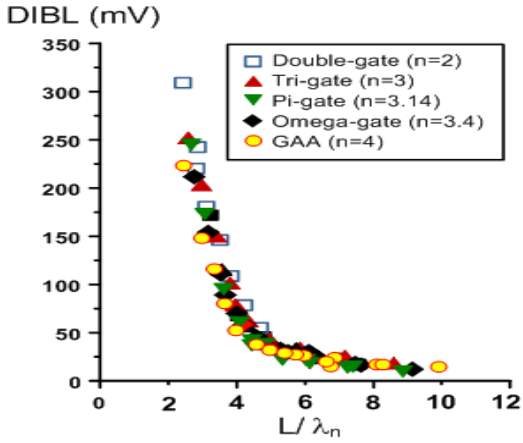

Figure 5. Drain-induced barrier lowering (DIBL) and subthreshold swing in multiigate transistors as a function of the normalized gate length, L_G/λ [5].

The analytical expressions for the natural length are given in Table 1. Quite clearly, increasing the number of gates decreases λ and improves short-channel effects.

Gate architecture	Natural length	Ref.
Single gate	$\lambda_1 = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}$	[9]
Double gate	$\lambda_2 = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right) t_{si} t_{ox}}$	[10]
Triple gate, square section	$\lambda_3 = \sqrt{\frac{\varepsilon_{si}}{3\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right) t_{si} t_{ox}}$	[11]
Quadruple gate, square section	$\lambda_4 = \sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right) t_{si} t_{ox}}$	[12]
Cylindrical GAA	$\lambda_{GAA} = \sqrt{\frac{2\varepsilon_{si} R^2 \ln\left(1+\frac{t_{ox}}{R}\right)+\varepsilon_{ox} R^2}{4\varepsilon_{ox}}}$	[13]

Table 1: Natural length, λ, for different gate architectures. *R* is the semiconductor radius (cylindrical case), t_{si} is the semiconductor width and height (square section case), and t_{ox} is the gate oxide thickness.

Based on the expressions in Table 1 one can plot an estimate of the minimum gate length that is achievable with the different gat architectures, and the cylindrical GAA architecture is a clear winner (Figure 6). The shortest-gate multigate MOSFETs reported to date have a gate length of 5nm (Ω gate, experimental) and 3nm (GAA, simulations) [14,15].

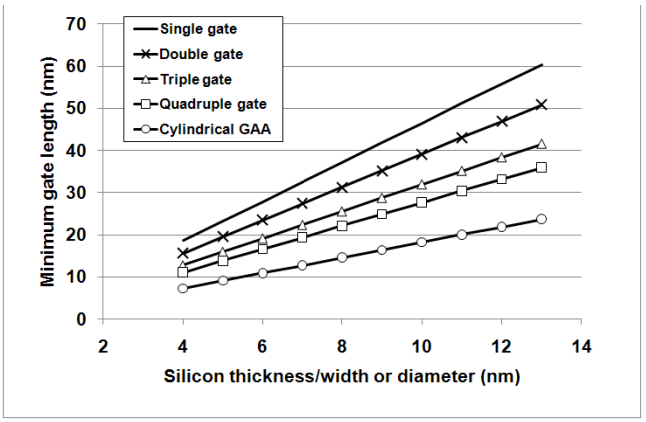

Figure 6. Minimum gate length as a function of silicon thickness/width or diameter. Double-gate, triple-gate and quadruple-gate MOSFETs have a square cross section. The equivalent oxide thickness (EOT) is taken as one-fifth the silicon thickness/diameter. One assumes that the minimum channel length is equal to six time the natural length in order to avoid short-channel effects ($L_{min}=6\lambda$).

III. CONFINEMENT EFFECTS

Carriers in thin and narrow FETs are confined in 2 directions (*y* and *z* in Fig. 4). If the section (diameter) of the wire is large enough, confinement can be neglected and surface channels are formed (see example of SOI trigate transistor in Fig 7). In smaller section FETss, carriers mostly flow in the center of the semiconductor. The transition occurs around 5nm in silicon and at larger sections in low-effective mass semiconductors.

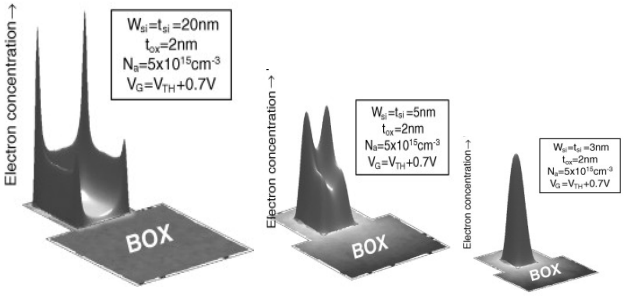

Figure 7. Carrier concentration profile in trigate SOI transistors in strong inversion, for different square cross-sections.[16]

Confinement gives rise to the formation of subbands and the DoS becomes a succession of spikes (Fig. 8). If the temperature and the drain voltage are low enough, oscillations can be measured in the $I_D(V_G)$ curves of thin

and narrow transistors. These correspond to the successive filling of subbands as gate voltage is increased (Figure 9 .[17]. If the section is small enough, these oscillations can be observed at room temperature [18]. Figure 8 shows the calculated DoS in the conduction band of a trigate transistor with a cross section of 40nm × 60nm and the corresponding measurement of drain current at different temperatures and drain voltages [19].

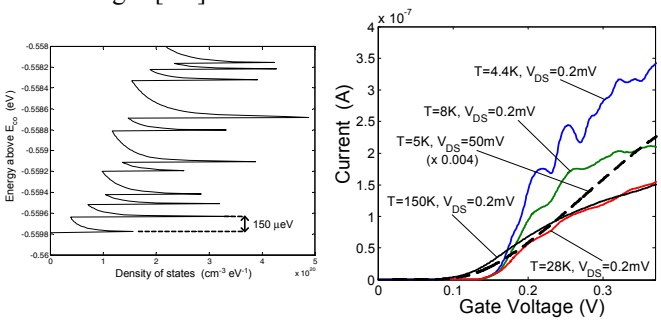

Figure 8: DoS in the conduction band of a trigate transistor and measurement of $I_D(V_G)$ at different temperatures and drain voltage values.

IV. TRANSITIONS

Confinement effects give rise to two interesting "transition" effects. The first one occurs if small potential barriers are created along the channel of a nanowire FET. These small barriers can arise from diameter variations (constrictions or simply line edge roughness) or localized surface or oxide charges. These barriers can isolate a portion of the channel (0D confinement) and transform the nanowire FET into a single-electron transistor (SET). The FET/SET transition is temperature dependent and has recently been observed at room temperature [20,21].

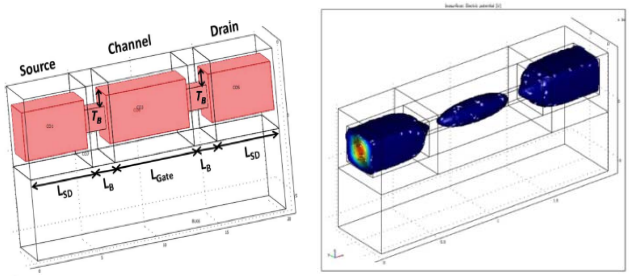

Figure 9: Nanowire FET with constrictions (left) and electron isoconcentration contours showing the formation of a quantum dot in the channel.

The energy bandgap of semiconductor nanowires increases as the semiconductor diameter is decreased due to adding confinement energy to "bulk" energy levels [22]. This property is also applicable to semimetals which can transform into semiconductors when in a nanowire form. Bismuth nanowires, for example, show a semimetal behavior for diameters above 100nm and a semiconductor behavior for smaller diameters (Fig 10) [23]. Schottky junction behavior has been observed in bismuth step nanowires (diameter is varied in a step-like manner), indicating the larger part of the nanowire is metallic and the thinner part is a semiconductor [24].

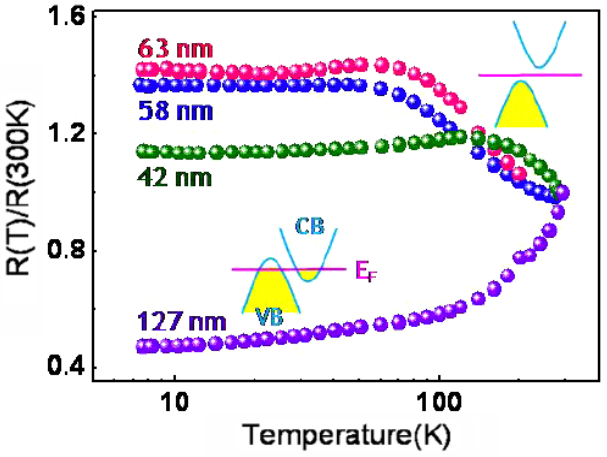

Figure 10: Resistance *vs.* temperature in Bismuth nanowires with different diameters [23].

Tin is a semiconductor with zero-energy (or slightly negative) bandgap. *Ab-initio* DFT simulations carried out on a GAA tin nanowire transistor with variable diameter (Figure 11) reveal that source and drain are metallic and the channel is semiconducting. In such a device there is no need for doping. Well- behaved transistor characteristics are obtained, with a subthreshold slope of 72 mV/dec and an I_{Dsat} of 3000 μA/μm at V_G=0.44V and V_D=0.25V (Figure 12) [25].

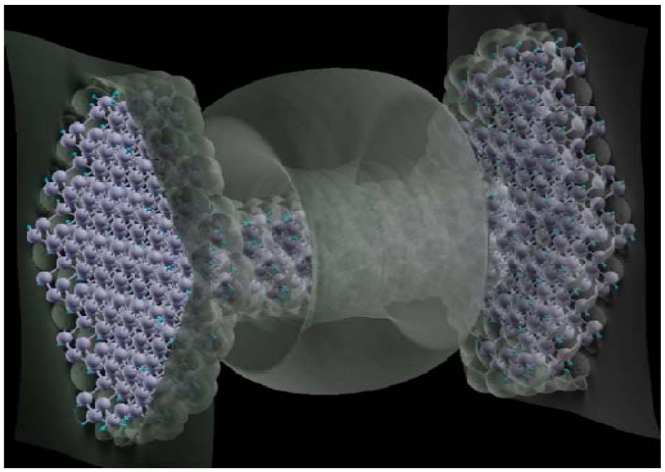

Figure 11: Tin (Sn) GAA nanowire transistor. L=2.3nm, Ø = 1 nm.

I. CONCLUSION

The multigate transistor structure achieves improved control of short-channel effects. The formation of subbands due to quantum confinement results in observable modifications of the electrical characteristics of MOSFETs. Metal-to-

semiconductor and FET to SET transitions can be observed using certain materials and using variations of nanowire diameter.

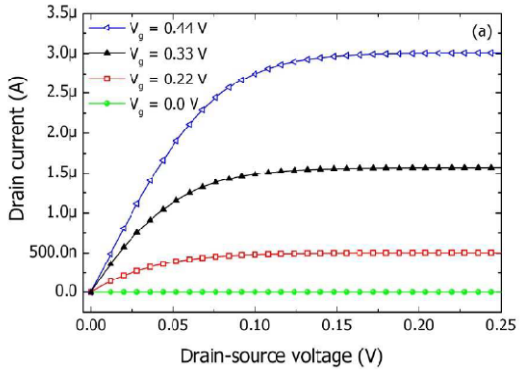

Figure 12: Output characteristics of a Tin nanowire FET.

REFERENCES

[1] http://en.wikipedia.org/wiki/Transistor_count

[2] J.T. Park, C.A. Colinge, J.P. Colinge, "Comparison of gate structures for short-channel SOI MOSFETs", *Proceedings of the IEEE International SOI Conference*, pp. 115-116 (2001)

[3] J.T. Park, J.P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines", *IEEE Transactions on Electron Devices*, Vol. 49, no. 12, pp. 2222-2229 (2002)

[4] J.P. Colinge,"Multiple-gate SOI MOSFETs", *Solid-State Electronics*, Vol. 48, no. 6, pp. 897-905 (2004)

[5] I. Ferain, C.A. Colinge, J.P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors", *Nature*, Vol. 479, pp. 310-316 (2011)

[6] K.J. Kuhn, "Considerations for Ultimate CMOS Scaling", *IEEE Transactions on Electron Devices*, Vol. 59, no. 7, pp. 1813-1828 (2012)

[7] J. Goldberger, A.I. Hochbaum, Rong Fan, Peidong Yang, "Silicon Vertically Integrated Nanowire Field Effect Transistors", *Nano Letters*, Vol. 6, no. 5, pp. 973-977 (2006)

[8] Y. Tosaka, K. Suzuki, T. Sugii, "Scaling-Parameter-Dependent Model for Subthreshold Swing S in Double-Gate SOI MOSFET's", *IEEE Electron Device Letters*, Vol. 15, no. 11, pp. 466-468 (1994)

[9] R.H. Yan, A. Ourmazd, K.F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk", *IEEE Transactions on Electron Devices*, Vol. 39, no. 7, pp. 1704-1710 (1992)

[10] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Arimoto, "Scaling theory for double-gate SOI MOSFETs", *IEEE Transaction on Electron Devices*, Vol. 40, no. 12, pp. 2326-2329 (1993)

[11] Chi-Woo Lee, Se-Re-Na Yun, Chong-Gun Yu, Jong-Tae Park, J.P Colinge, "Device design guidelines for nano-scale MuGFETs", *Solid-State Electronics*, Vol. 51, pp. 505-510 (2007)

[12] J.P. Colinge, "Multiple-gate SOI MOSFETs", *Solid-State Electronics*, Vol. 48, no. 6, pp. 897-905 (2004)

[13] C.P. Auth, J.D. Plummer, "Scaling theory for cylindrical, fully depleted, surrounding-gate MOSFET's", *IEEE Electron Device Letters*, Vol. 18, no. 2, pp. 74-76 (1997)

[14] Fu-Liang Yang, Hsin-Chu, Di-Hong Lee, Hou-Yu Chen, Chang-Yun Chang, Sheng-Da Liu, Cheng-Chuan Huang, Tang-Xuan Chung, Hung-Wei Chen, Chien-Chao Huang, Yi-Hsuan Liu, Chung-Cheng Wu, Chi-Chun Chen, Shih-Chang Chen, Ying-Tsung Chen, Ying-Ho Chen, Chih-Jian Chen, Bor-Wen Chan, Peng-Fu Hsu, Jyu-Honig Shieh, Han-Jan Tao, Yee-Chia Yeo, Yiming Li, Jam-Wem Lee, Pu Chen, Mong-Song Liang, Chenming Hu, "5nm-gate nanowire FinFET" , *Symposium on VLSI Technology. Digest of Technical Papers*, pp. 196-197, 2004

[15] L. Ansari, B. Feldman, G. Fagas, J.P. Colinge J.C. Greer, "Simulation of junctionless Si nanowire transistors with 3 nm gate length", *Applied Physics Letters,* Vol. 97, p. 062105 (2010)

[16] J.P. Colinge, "Quantum-wire effects in trigate SOI MOSFETs", *Solid-State Electronics*, Vol. 51, pp. 1153–1160 (2007)

[17] J.P. Colinge, X. Baie, V. Bayot, E. Grivei, "A silicon-on-insulator quantum wire", *Solid-State Electronics*, Vol. 39, pp. 49-51, 1996

[18] Kyung Soo Yi, K. Trivedi, H.C. Floresca, Hyungsang Yuk, W. Hu, Moon J. Kim, "Room-Temperature Quantum Confinement Effects in Transport Properties of Ultrathin Si Nanowire Field-Effect Transistors", *Nano Letters*, Vol. 11, n0. 12, pp 5465–5470 (2011)

[19] J.P. Colinge, A.J. Quinn, L. Floyd, G. Redmond, J.C. Alderman, W. Xiong, C.R. Cleavelin, T. Schulz, K. Schruefer, G. Knoblinger, P. Patruno, "Low-Temperature Electron Mobility in Trigate SOI MOSFETs", *IEEE Electron Device Letters*, Vol. 27, no. 2 , pp. 120- 122 (2006)

[20] N. Dehdashti Akhavan, A. Afzalian, Chi-Woo Lee, Ran Yan, I. Ferain, P. Razavi, Ran Yu, G. Fagas, J.P. Colinge, "Nanowire to Single-Electron Transistor Transition in Trigate SOI MOSFETs", *IEEE Transactions on Electron Devices*, Vol. 58, no. 1, pp. 26-32 (2011)

[21] V. Deshpande , S. Barraud, X. Jehl, R. Wacquez, M. Vinet, R. Coquand, B. Roche, B. Voisin, F. Triozon, C. Vizioz, L. Tosti, B. Previtali, P. Perreau, T. Poiroux, M. Sanquer, O. Faynot, Scaling of Trigate nanowire (NW) MOSFETs to sub-7 nm width: 300 K transition to Single Electron Transistor", *Solid-State Electronics*, Vol. 84, pp. 179–184 (2013)

[22] M. Nolan, S. O'Callaghan, G. Fagas, J.C. Greer, T. Frauenheim, "Silicon nanowire band gap modification", *Nano Letters,* Vol. 7, no. 1, pp. 34-38 (2007).

[23] Seunghyun Lee, Jinhee Ha, Kyejin Jeon, Jin-Seo Noh and Wooyoung Le, "Direct observation of the semimetal-to-semiconductor transition of individual single-crystal bismuth nanowires grown by on-film formation of nanowires", *Nanotechnology* Vol. 21, p. 405701 (2010)

[24] Y.T. Tian, G.M. Meng, G.Z. Wang, F. Phillipp, S.H. Sun, L.D. Zhang, "Step-shaped bismuth nanowires with metal–semiconductor junction characteristics", *Nanotechnology*, Vol. 17, pp. 1041–1045 (2006)

[25] L. Ansari, G. Fagas, J.P. Colinge, J.C. Greer, "A Proposed Confinement Modulated Gap Nanowire Transistor Based on a Metal (Tin)", *Nano Letters*, Vol. 12-5, pp. 2222-2227 (2012)