0.5V operation and performance of nonvolatile SRAM cell based on pseudo-spin-FinFET architecture

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***Abstract*—0.5V operation and power-gating ability of nonvolatile SRAM (NV-SRAM) cell using pseudo-spin-FinFETs (PS-FinFETs) are investigated. The cell is configured so as to achieve a minimum occupied-area design, i.e., all the FinFETs used in the cell are designed with a single fin channel. The 0.5V operations are analyzed from various static noise margins (SNMs) for the normal operation and nonvolatile power-gating (NVPG) modes. The SNMs for all the normal (hold, read, and write) operations are satisfactorily large even for the 0.5V operation, although the wordline underdrive technique is needed to be introduced for the read operation. The SNMs for the store operations of the NVPG mode also satisfy requirements for the shutdown and wake-up operations, when bias-assisted techniques are employed for the PS-FinFETs of the cell. Energy performance of the NV-SRAM cell is evaluated using break-even time (BET). A sufficiently short BET applicable to fine-grained NVPG of microprocessors and SoCs can be achieved even for the 0.5V operation with the various bias-assisted techniques. In addition, store-free shutdown architecture is further effective at reducing BET. Average power of the cell can be dramatically reduced by 0.5V operation, although the reduction rate depends on the leakage current during shutdown mode and the proportion of shutdown period. This FinFET-based NV-SRAM cell using pseudo-spin-transistor architecture is promising for NVPG of low-voltage logic systems.**

Keywords— power-gating; nonvolatiel SRAM; break-even time; low-voltage operaion; FinFET; Spintronics

I. Introduction

Low-voltage operation (e.g., 0.5V) of CMOS logic systems has received considerable attention owing to its ability of dramatic reduction of dynamic and static power dissipation [1]. Since the proportion of static power to dynamic power increases for low-voltage operations, various reduction techniques for static power would still be important even for low-voltage CMOS logic systems. In particular, nonvolatile power-gating (NVPG) [2-9] is expected to be a promising architecture for low-voltage CMOS logic systems, since it can achieve highly energy-efficient power-gating with spatially- and temporally-optimized granularity. Recently, we proposed a NVPG architecture using nonvolatile bistable circuits such as nonvolatile SRAM (NV-SRAM) and nonvolatile flip-flop (NV-FF) using pseudo-spin-transistors [2-12]. These bistable circuits can simply be configured by connecting pseudo-spin-MOSFETs (PS-MOSFETs) to the storage nodes of standard/conventional SRAM/FF cells. The PS-MOSFET is a circuit for reproducing spin-transistor functions using a spin-transfer-torque magnetic tunnel junction (STT-MTJ) connected to the source terminal of an ordinary MOSFET [2,4-12]. These NV-SRAM and NV-FF circuits can be realized by application of present MRAM technology to CMOS logic platform.

Pseudo-spin-transistors employing FinFETs (hereafter, referred to as PS-FinFETs) are attractive for the NVPG architecture adaptable to FinFET-based high-performance logic systems, since PS-FinFETs have excellent spin-transistor performance with higher current drivability and lower leakage characteristics [13]. The high current drivability of PS-FinFETs is remarkably suitable for low-voltage operations, and thus PS-FinFETs would introduce nonvolatile functionality into low-voltage CMOS logic systems.

In this paper, we computationally investigated 0.5V operation and energy performance of a NV-SRAM cell employing PS-FinFETs.

II. PS- FinFET Design and Characteristics

Figures 1(a) and (b) show the schematic illustration and circuit configuration of the proposed PS-FinFET, respectively. The effective input bias V_{GS0} and also body-source (substrate) bias V_{BS0} are modulated by the magnetization configuration of

TABLE I. FinFET and STT-MTJ parameters

FinFET	
Channel length: L	20nm
Supply voltage: V_{DD}	0.9V 0.5V
Fin width	15nm
Fin height	28nm
Fin No. of NV-SRAM Load,Driver,Pass,PS-FinFET: (N_{FL},N_{FD},N_{FP},N_{FPS})	(1,1,1,1)
STT-MTJ	
Tunneling magnetoresistance: TMR	100%
Resistance-area product: RA (P mag.)	2 Ω·μm^2
Voltage at half-maximum of TMR: V_{half}	0.5 V
CIMS critical current density: J_C	5×10^6 A/cm^2
Device diameter: ϕ	20 nm
CIMS critical current: I_C	15.7 μA
Resistance: $R_P(0)$ (P mag.)	6.36 kΩ
$R_{AP}(0)$ (AP mag.)	12.7kΩ

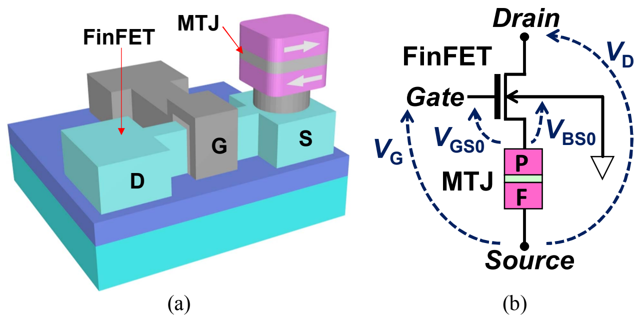

Fig. 1. (a) Schematic illustration and (b) circuit configuration of a pseudo-spin-FinFET (PS-FinFET). The STT-MTJ is not need to be formed directly on the source region of the FinFET and it would be integrated in multilevel interconnect layers.

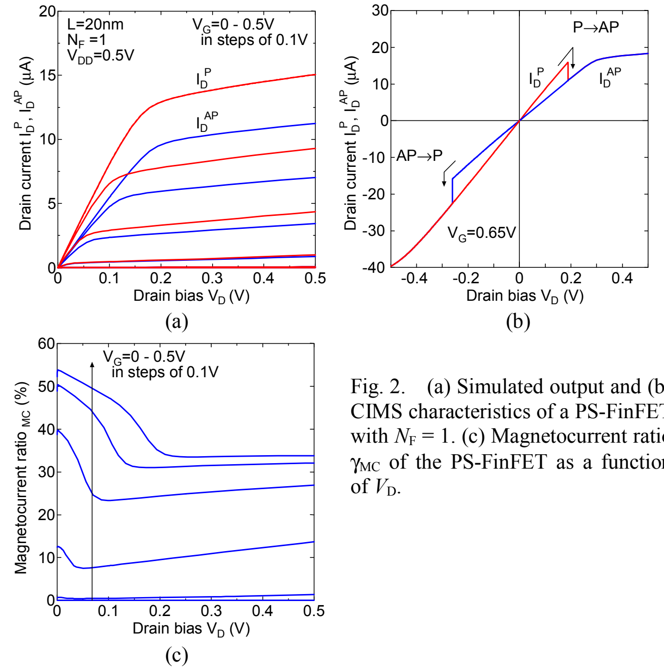

Fig. 2. (a) Simulated output and (b) CIMS characteristics of a PS-FinFET with N_F = 1. (c) Magnetocurrent ratio γ_{MC} of the PS-FinFET as a function of V_D.

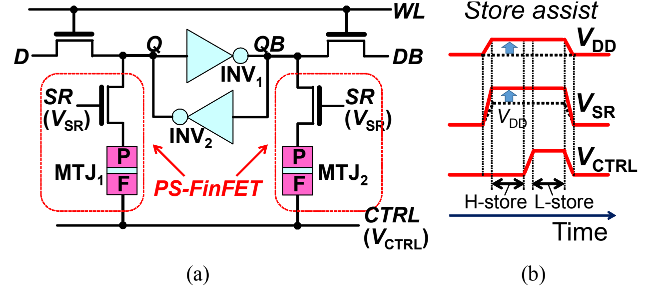

Fig. 3. (a) Circuit configuration of a NV-SRAM cell using PS-FinFETs. (b) Schematic waveforms of V_{DD}, V_{SR}, and V_{CTRL} during the store operation.

the STT-MTJ owing to the negative feedback effect of the STT-MTJ, resulting in magnetization- configuration-dependent (high and low) current drivabilities.

All the simulations examined here were performed using the HSPICE program with a predictive technology model for a 20nm FinFET [16] and our developed STT-MTJ macromodel [10]. The STT-MTJ parameters were determined by reference to recently reported STT- MTJs [17-19], as shown in Table I. Assuming the usage of a device process for the full-swing operation, the threshold voltages V_{th} of the FinFETs for the low-voltage operation were set to the same as those for the full-swing (0.9V) operation. Although the V_{th} is not optimized for low-voltage operation, the usage of an already-developed process would yield a benefit for production cost. Note that our developed simulation technique can accurately reproduce the experimental results of fabricated PS-MOSFETs [2,14,15].

Figures 2(a) and (b) show output characteristics of a PS-FinFET with the fin-channel number N_F of unity, in which V_G and V_D are varied from 0 to 0.5V. The magnetization-configuration-dependent high and low drain currents (I_D^P and I_D^{AP}) can be achieved in the parallel (P) and antiparallel (AP) magnetization configurations of the STT-MTJ, respectively. Furthermore, current-induced magnetization switching (CIMS) for both the P-to-AP and AP-to-P magnetization changes successfully occurs when V_G is raised to more than 0.6V, as shown in Fig. 2(b). Note that critical V_G for CIMS depends on J_C. In the case of J_C = 1×10^6 A/cm^2, V_G = 0.5V is enough for CIMS. The magnetocurrent ratio γ_{MC} (= (I_D^P-I_D^{AP})/I_D^{AP})) of the PS-FinFET increases with decreasing V_D (for lower V_D) and with increasing V_G (Fig. 2(c)). γ_{MC} can be designed by N_F of the FinFET and by *RA* and *TMR* of the STT-MTJ [15].

III. NV-SRAM Cell Operation

Figure 3(a) shows the circuit configuration of the proposed NV-SRAM cell using PS-FinFETs. The cell consists of a cross-coupled inverter loop and two PS-FinFETs connected to the storage nodes of the inverter loop. Hereafter, N_F of the load transistors, driver transistors, pass transistors, and PS-FinFETs are denoted by N_{FL}, N_{FD}, N_{FP}, and N_{FPS}, respectively. Design of N_{FL} and N_{FD} is highly important, since it restricts the occupied area and SNMs of the cell. Using the base design of (N_{FL}, N_{FD}) = (1,2), large SNMs can easily be obtained. However, its cell area overhead is not minor. The base design of (N_{FL}, N_{FD}) = (1,1) is beneficial to minimize cell area, although the cell stability is lowered.

In the shutdown and wake-up operations for NVPG, the NV-SRAM cell executes store and restore operations, respectively. The store operation is divided into two steps, as shown in Fig. 3(b). In the first step, H-level data on the storage node (Q or QB) is stored into the STT-MTJ connected to the node (H-store operation), and in the second step, L-level data of the other storage node is stored in the other STT-MTJ (L-store operation) [12]. At the initial stage of the restore operation, the PS-FinFETs are turned on, and the data stored in these STT-MTJs are restored to the storage nodes of the bistable circuit by pull-up of power supply voltage V_{DD} for the cell.

IV. SNMs and Energy Performance

Figures 4(a)-(c) show SNMs for the hold, read, and write operations of a NV-SRAM cell with the design of (N_{FL}, N_{FD}, N_{FP}, N_{FPS}) = (1,1,1,1) for V_{DD} = 0.9V and 0.5V. Satisfactorily large SNMs (> 100mV) can be achieved even for the 0.5V operation, although the wordline underdrive technique [20] is used for the read operation. Note that the SNMs for these

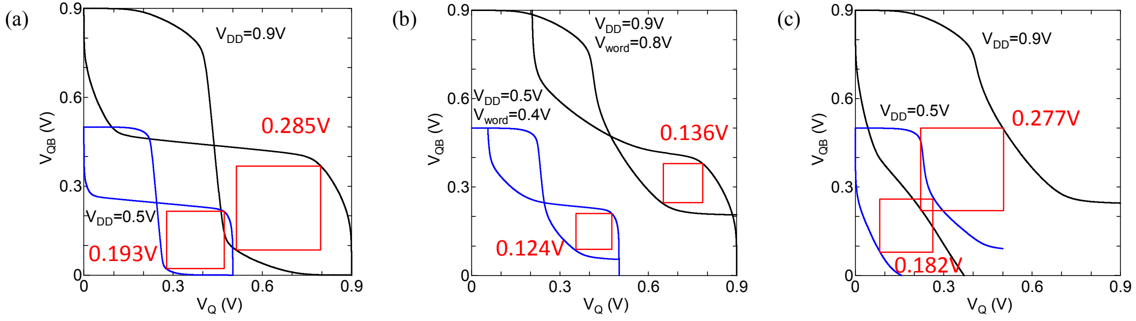

Fig. 4. Butterfly curves for the (a) hold, (b) read, and (c) write operations of a NV-SRAM cell with the design of (N_{FL},N_{FD},N_{FP},N_{FPS}) = (1,1,1,1) for full-swing (0.9V) and low-voltage (0.5V) operations, in which the wordline underdrive is employed for the low-voltage read operation. All the curves completely correspond to those of equivalent volatile FinFET-based 6T-SRAM cell.

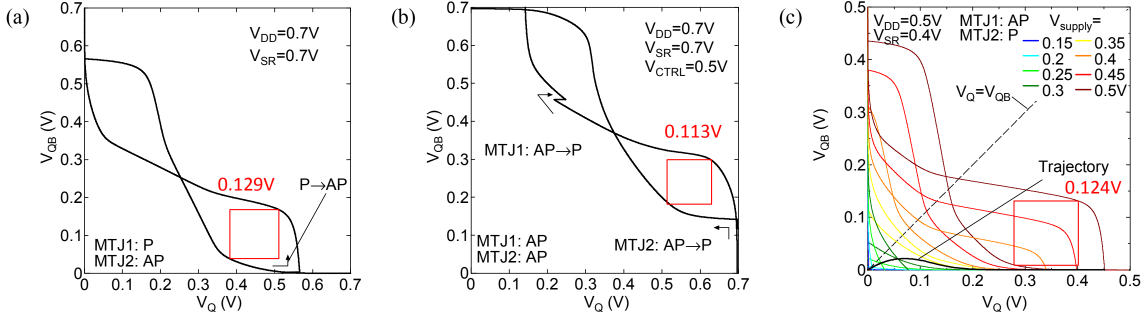

Fig. 5. Butterfly curves of (a) the H-store and (b) L-store operations for the NV-SRAM cell with the design of (N_{FL},N_{FD},N_{FP},N_{FPS}) = (1,1,1,1) for the low-voltage operation. V_{DD} and V_{SR} are boosted so that the store currents $I_{MTJ}^{P\rightarrow AP}$ and $I_{MTJ}^{AP\rightarrow P}$ for the H-store and L-store operations are equal to 1.5×J_C. (c) Butterfly curves and transient trajectory for the node voltages of the NV-SRAM cell during the low-voltage restore operation, in which V_{SR} underdrive is employed.

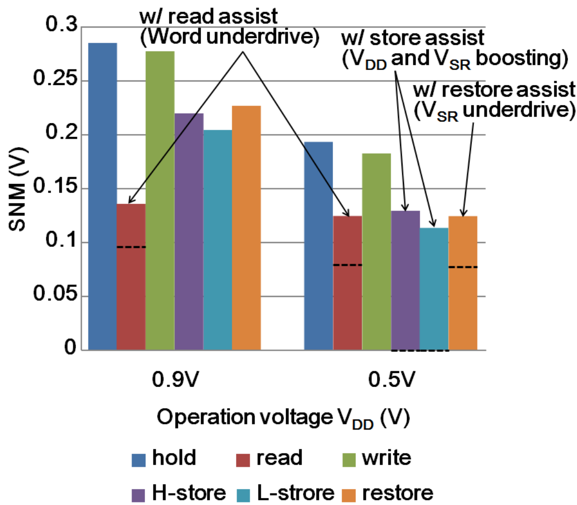

Fig. 6. SNMs for the hold, read, write, H-store, L-store, and restore operations of the NV-SRAM cell with the cell design of (N_{FL}, N_{FD}, N_{FP}, N_{FPS}) = (1,1,1,1) for the 0.9V and 0.5V operations. Dotted lines show the SNMs without the assist techniques.

normal SRAM operations are completely the same as those of the equivalent volatile FinFET-based 6T-SRAM cell, since the STT-MTJs can be electrically separated from the bistable circuit part of the cell by the PS-FinFETs during these normal operations. Figures 5(a) and (b) show the butterfly curves for the H-store and L-store operations of the NV-SRAM cell with the design of (N_{FL}, N_{FD}, N_{FP}, N_{FPS}) = (1,1,1,1) for the low voltage operation mode, respectively. When J_C and error margin for CIMS are 5×10^6 A/cm^2 and 1.5×J_C, it is difficult to create a current required for CIMS. However, CIMS can be accomplished by the V_{SR} and V_{DD} boosting (see Fig. 3(b)). In the case of J_C = 5×10^6 A/cm^2 and error margin of 1.5×J_C, V_{SR} = 0.7V, V_{DD} = 0.7V, and V_{CTRL} = 0.5V is suitable, as shown in Figs. 5(a) and (b). Figure 5(c) shows transient trajectory for the node voltages (V_Q and V_{QB}) of the NV-SRAM cell during the restore operation, in which butterfly curves for various V_{DD} are also shown. Just after the pull-up of V_{DD}, V_Q and V_{QB} increase with increasing V_{DD}. Then, only V_Q increases with increasing V_{DD}, while V_{QB} quickly approaches zero (Fig. 5(c)). The SNM for the restore operation is satisfactorily large even for the 0.5V operation, when V_{SR} underdrive is used (which is similar to the wordline underdrive technique). Figure 6 summarizes the various SNMs of the cell for the 0.9V and 0.5V operation modes. The SNMs depend on the operation voltage. Nevertheless, even for the 0.5V operation, the cell can satisfy sufficient margins (> 100mV) using the read, store, and restore assist techniques.

Figures 7(a) and (b) show break-even time (BET) of the NV-SRAM cell [8] as a function of τ_{exe} (normal SRAM operation duration) for the 0.9V and 0.5V operations, respectively. For the 0.9V operation, previously-developed store bias and leakage controls [2,6,7,11] are employed (the former controls V_{SR} and V_{CTRL} and the latter V_{CTRL}). The leakage control and the above-described store and restore assist techniques are used for the 0.5V operation. The store-free

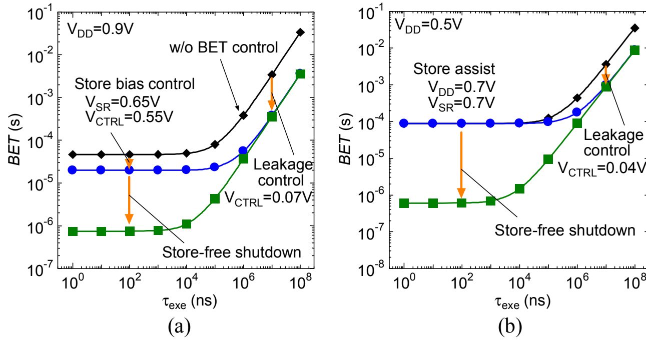

Fig. 7. BET as a function of τ_{exe} (normal SRAM operation duration) for the NV-SRAM cell with the design of (N_{FL}, N_{FD}, N_{FP}, N_{FPS}) = (1,1,1,1) for the (a) 0.9V and (b) 0.5V operations.

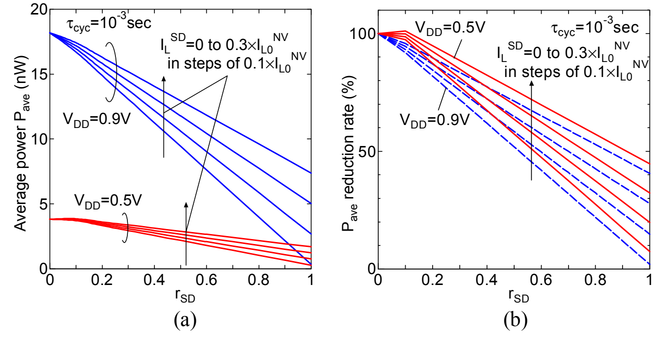

Fig. 8. (a) Average power P_{ave} and (b) reduction rate of P_{ave} as a function of r_{SD} for the 0.9V and 0.5V operations, in which leakage current I_L^{SD} during shutdown is varied from 0 to 0.3×I_{L0}^{NV} (I_{L0}^{NV} = 9.47nA and 26.1nA for the 0.5V and 0.9V operations, respectively. I_{L0}^{NV} represents the leakage current of the NV-SRAM cell during standby mode).

shutdown architecture [11] for reducing BET can also be applied for both the cases. Since the static leakage current is suppressed for the 0.5V operation, the low-voltage operation slightly prolong the BET (see blue curves in Figs. 7(a) and (b)). Using the store-free shutdown, a BET of less than 1µs would be achieved on average even for the 0.5V operation, which is sufficiently short for fine-grained NVPG application of microprocessors and SoCs.

Figure 8(a) shows the average power P_{ave} of the static leakage power including the power for the NVPG operations for the NV-SRAM cell as a function of proportion r_{SD} of shutdown period. P_{ave} can be dramatically reduced by lowering the operation voltage. Although the reduction rate for P_{ave} to r_{SD} depends on the leakage current I_L^{SD} during the shutdown, P_{ave} can be effectively reduced by the shutdown for the 0.5V operation as with the 0.9V operation, as shown in Fig. 8(b).

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