Simultaneous Simulation of Systematic and Stochastic Process Variations

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***Abstract*—An efficient approach is presented and demonstrated which enables the simultaneous simulation of the impact of several sources of process variations, ranging from equipment-induced to stochastic ones, which are caused by the granularity of matter. Own software is combined with third-party tools to establish a hierarchical simulation sequence from equipment to circuit level. Correlations which occur because some sources of variability affect different devices and different device quantities can be rigorously studied.**

Keywords—process variations; systematic variations; statistical variations; lithography; etching; equipment simulation; process simulation; device simulation; RDF; LER; MGG

I. INTRODUCTION

Advanced nanoelectronic devices and circuits are subject to a wide range of systematic and stochastic process variations. Most results published so far refer to stochastic variations which result from the granularity of matter, e.g. Random Dopant Fluctuations RDF [1]. However, especially with further shrinking device sizes, variations of device geometries or of (continuum) doping profiles caused by non-idealities and drift of process equipment, or by proximity effects of features within a non-regular chip layout increasingly gain importance and may especially for fully depleted devices dominate about stochastic variations. The impact of variations must be simulated starting from their source in order to be able to include correlations e.g. between features which were subject to the same process step. This requires a hierarchical statistical simulation from equipment to device and circuit level as sketched in Fig. 1.

II. METHODOLOGY AND RESULTS

In earlier publications (e.g. [2][3]) we discussed the impact of variations of different topography steps, especially optical lithography, on transistor geometries and performance. Among others we demonstrated that a Gaussian distribution of defocus in optical lithography leads to a highly asymmetric distribution of Critical Dimensions CD (e.g. gate length and width). In Fig. 2 (a) variations of defocus and dose are shown which are used in this work and which represent those occurring in typical 193nm proximity steppers. Fig. 2 (b) then shows in a colour plot the gate length variations caused for a typical 20 nm planar CMOS transistor, caused by these lithography variations. Other process steps such as etching add further variations to the CD,

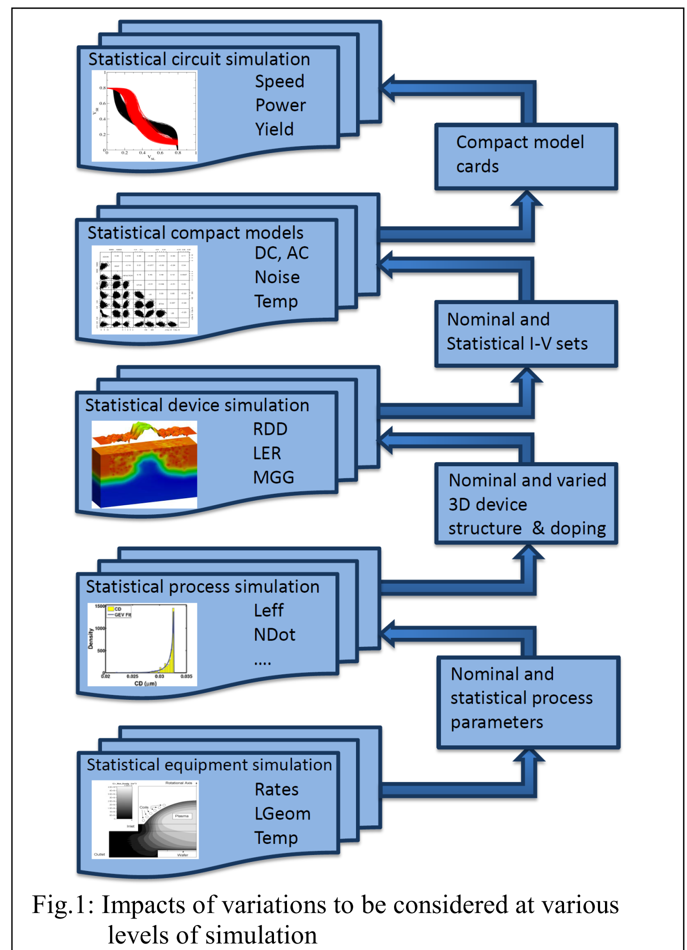

Fig.1: Impacts of variations to be considered at various levels of simulation

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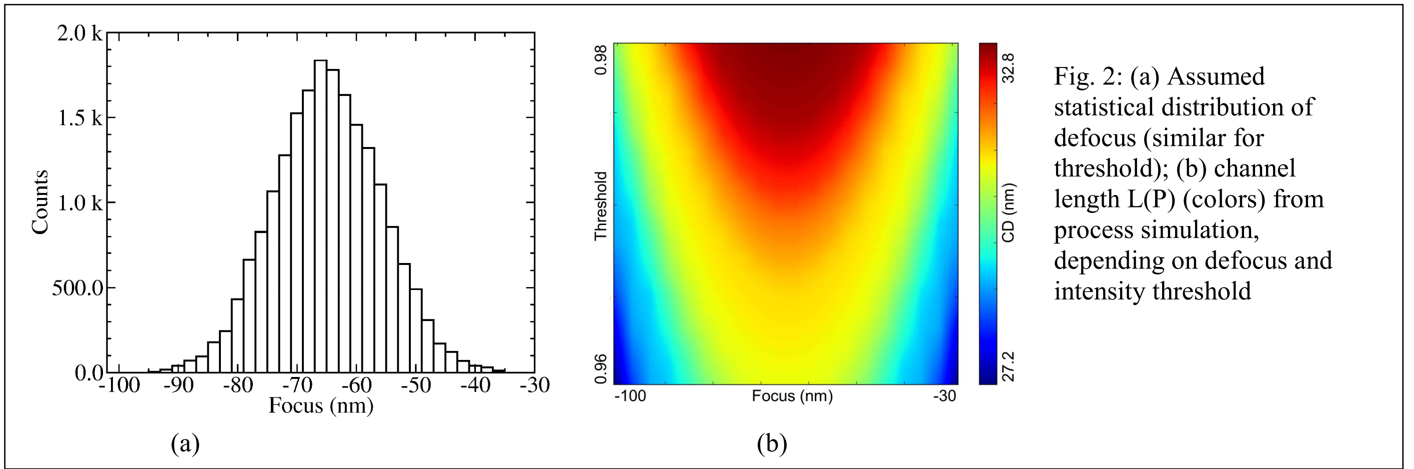

Fig. 2: (a) Assumed statistical distribution of defocus (similar for threshold); (b) channel length L(P) (colors) from process simulation, depending on defocus and intensity threshold

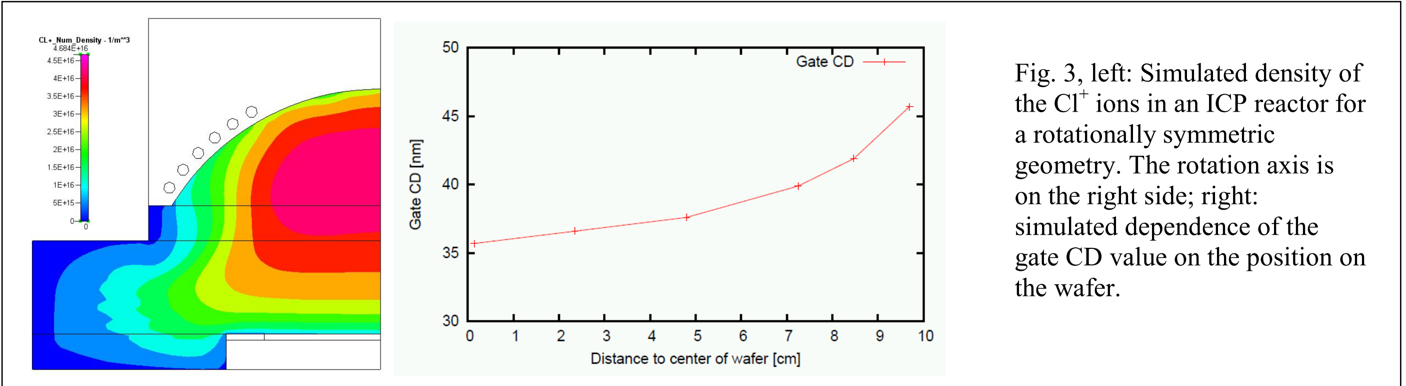

Fig. 3, left: Simulated density of the Cl^+ ions in an ICP reactor for a rotationally symmetric geometry. The rotation axis is on the right side; right: simulated dependence of the gate CD value on the position on the wafer.

as exemplarily shown in Fig. 3 for polysilicon etching in an inductively coupled plasma (ICP) reactor. In consequence, the geometry of the device to simulated has a statistical distribution which depends on the variation of some technological parameters, such as defocus in lithography or position on the wafer.

In order to enable the simultaneous simulation of systematic and stochastic variations, the own (Dr.LiTHO [4], DEP3D [5], ANETCH [6]) and the commercial process simulation tools (SENTAURUS [7]) used have been interfaced via the DF-ISE file format [7] with the stochastic device simulation tool GARAND from GSS [8], as described more in detail elsewhere [9]. As an example, in Fig. 4 (a) the I_d-V_g characteristics at low drain voltage (V_d=0.05V) simulated by GARAND for transistors with different channel length L and width W are shown, without considering RDF and other stochastic variations. In order to study the combined effect of systematic variations of transistor geometry and statistical variations, namely RDF, Line Edge Roughness LER and Metal Gate Granularity MGG, stochastic device simulations were performed with GARAND for transistors with nominal sizes L = 23.5 nm and W = 33nm, and for corner devices with combinations of minimum and maximum values of L and W, respectively. Fig. 4 then also shows as an example the I_d-V_g characteristics of a transistor with RDF and nominal size, and that of transistors with RDF assuming minimum L / maximum W and maximum L / minimum W considered. From these simulations, probability density functions for relevant parameters such as the threshold voltage V_{th} are extracted. Fig. 5 shows these distributions for the nominal device and the two corner devices of Fig. 4 b) to d), with shifts of the PDFs for different L.

From such simulations the statistical distribution (due to RDF, LER and MGG) g(L,W) of a key transistor parameter G (such as V_{th}, I_{on} or SS) can easily be extracted for a given fixed combination of channel length L and width W. The dependence of channel length and width on varying process parameter(s) P (e.g. defocus in lithography) and position on the wafer (which affects etch bias as shown in Fig. 3), L(P) and W(P), is known from the lithography/topography simulation employed before. The overall distribution h of the transistor parameter G is then given by integrating across all values of the varying technological parameters P and employing the probability density p(P) of these parameters:

$$h = \int g(L(P),W(P))\, p(P)\, dP \qquad (1)$$

This distribution which results from sequential stochastic equipment/process and device simulation then includes both the impact of the systematic and the stochastic variations considered, and moreover also correlations which occur if different device quantities are influenced by the same source of variations. The identification of a small set of parameters (here L and W) which well represent the variability resulting from equipment and process allow for the factorization between equipment/process and device level according to eq. (1) and therefore for an efficient study of variability impacts. An efficient approach to extract the compact model kernel g is

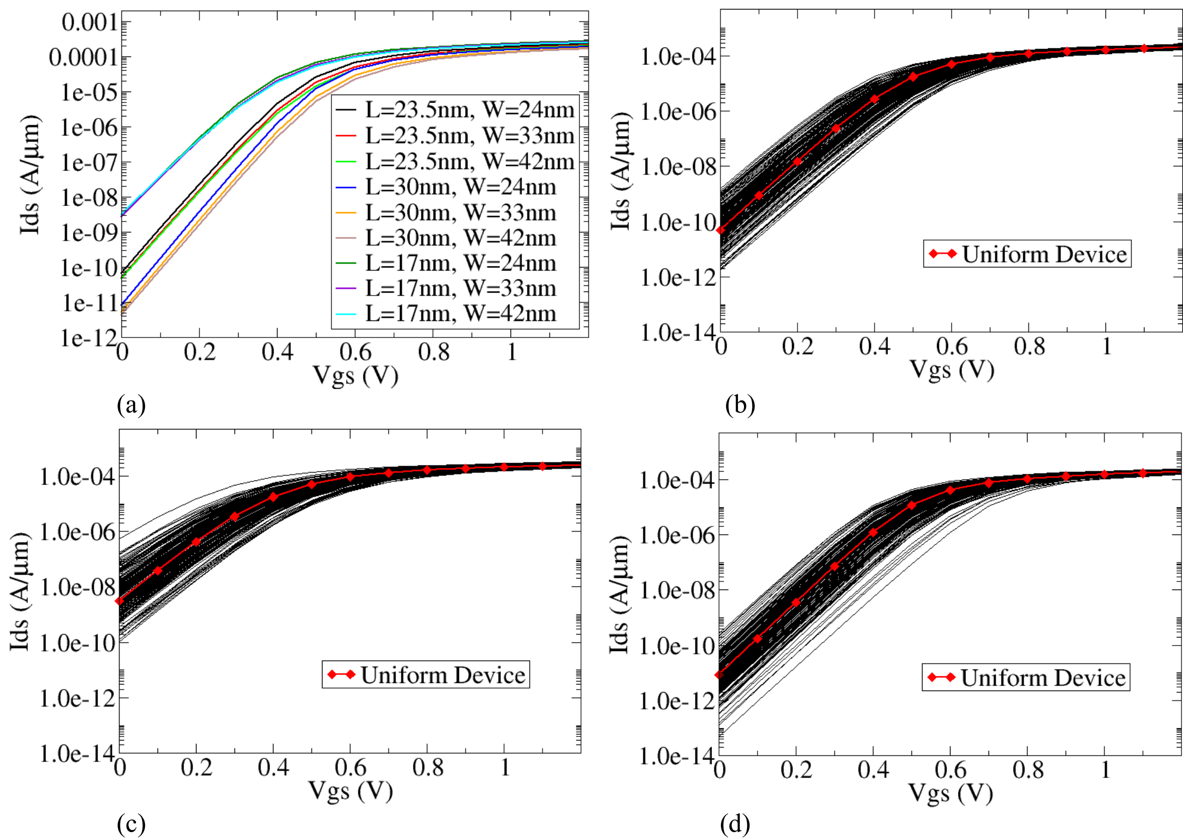

Fig. 4: (a) I_d-V_g characteristics at low drain voltage (V_d=0.05V) for transistors with different L and W caused by process variations and no RDF (left); (b) with RDF for nominal device (L=23.5nm, W=33nm); for corner devices with (c) minimum L / maximum W (L=17nm, W=42nm) and (d) maximum L / minimum W (L = 30 nm, W = 24 nm)

presented elsewhere [10]. In Fig. 6 the probability distribution function PDF of the threshold voltage is shown, which results from variations of the lithography step as show in Fig. 2, RDF/LER/MGG, assuming different situations for the etch bias: In Fig. 6a, a nominal fixed etch bias of 5nm is assumed, whereas Figs. 6b and Fig. 6c) show the distributions at the center of the wafer (10 nm etch bias) and near the edge of the wafer (0 nm etch bias), respectively. These different fixed values of the etch bias mainly lead to a considerable shift of the PDF to smaller voltages for larger etch bias which equals to shorter gate length. However, taking also the distribution of the etch bias across the wafer into account, the overall PDF is significantly broadened as show in Fig. 6d.

III. Conclusions

An efficient approach for the simultaneous simulation of systematic variations, caused by the equipment used, and stochastic variations resulting from the granularity of matter has been presented and been demonstrated for the example of lithography and etch bias variations together with RDF, LER and MGG. It allows for the assessment of the importance of such variations on the devices in question, which depends both on the architecture and the physical quantity considered.

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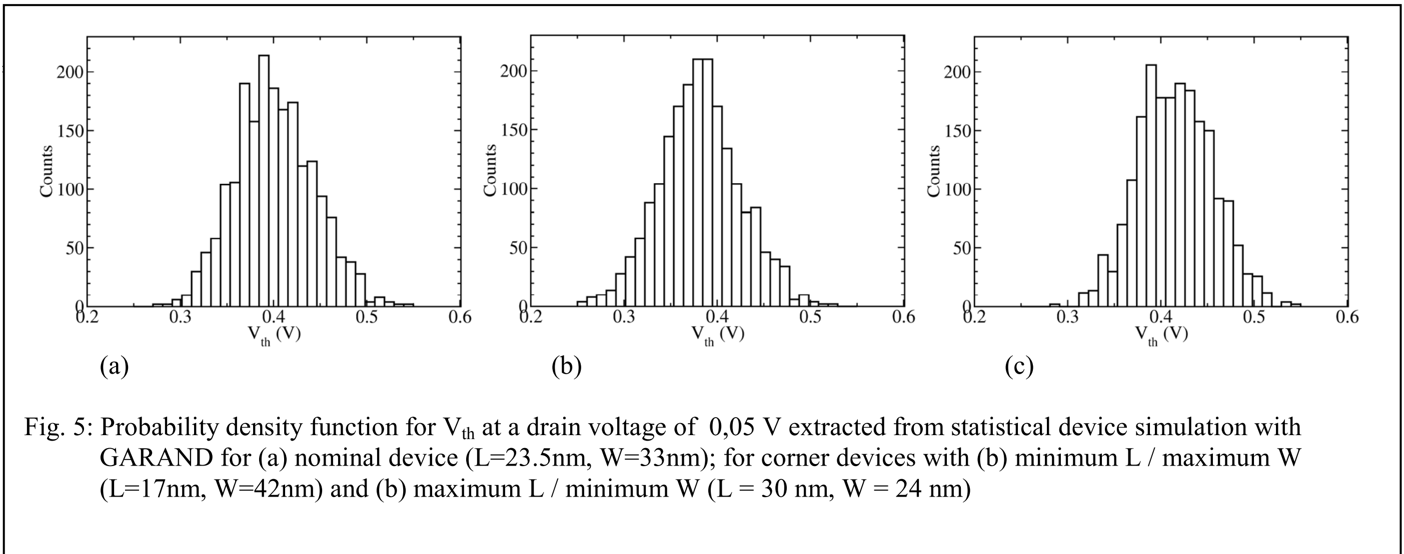

Fig. 5: Probability density function for V_{th} at a drain voltage of 0,05 V extracted from statistical device simulation with GARAND for (a) nominal device (L=23.5nm, W=33nm); for corner devices with (b) minimum L / maximum W (L=17nm, W=42nm) and (b) maximum L / minimum W (L = 30 nm, W = 24 nm)

Fig. 6: Overall distribution of threshold voltage at a drain voltage of 0,05 V caused by process and stochastic variations. In all cases, variation of lithography focus and dose is assumed as shown in Fig. 1, and RDF as shown in Figs. 3 and 4. (a): Transistors with nominal etch bias of 5 nm; (b) transistors at center of wafer (etch bias10 nm); (c) transistors near edge of wafer (etch bias = 0 nm); (d) overall distribution of all transistors on the wafer taking variation of etch bias into account