The Impact of Fin/Sidewall/Gate Line Edge Roughness on Trapezoidal Bulk FinFET Devices

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***Abstract*—In this work, the DC characteristic variability of 14-nm-gate HKMG trapezoidal bulk FinFET induced by different line edge roughness (LER) is for the first time studied by using experimentally validated 3D device simulation. By considering a time-domain Gaussian noise function, we compare four types of LER: Fin-LER inclusive of resist-LER and spacer-LER, sidewall-LER, and gate-LER for the trapezoidal bulk FinFET with respect to different fin angles. The resist-LER and sidewall-LER have large impact on characteristics fluctuation. For each type of LER, the V_{th} fluctuation is comparable among fin angles.**

Keywords*—line edge roughness; fin-LER; sidewall-LER; gate-LER; trapezoidal bulk FinFET

I. INTRODUCTION

Downscaling of CMOS technology node beyond the sub-20 nm causes the transistor to go through a transition from planar to multi-gate FETs because of the requirement of better gate control and suppression on short-channel effects (SCEs) [1-4]. However, many variability issues emerge from scaling. For low-standby-power devices, random dopant fluctuation (RDF) is a critical fluctuation source [5-8] due to the need of channel doping in increasing the threshold voltage (V_{th}). For high-speed operation, the work function fluctuation (WKF) [9-11] plays a significant role in characteristic variation. Moreover, different line edge roughness (LER), which comes from the lithography processes and etching steps, also causes variation which is comparable to WKF and does not scale down with technology node [12]. It would be more severe in nano-sized vertical-channel devices. In particular, multi-gate FETs are sensitive to LER because of the close relationship between their physical geometry and gate control ability. Furthermore, due to the limitation of process, the actual fins channel may be fabricated as trapezoidal shape and degrade the device performance by significant SCEs. Though various studies about LER and nonideal geometry of FinFET devices were reported [13-18], separately, the research which includes both issues simultaneously has not been investigated yet. It will be an interesting study for us if process variation effects could be considered in nonideal channel fin shape of bulk FinFET devices.

In this work, the DC characteristic variability of 14-nm-gate HKMG trapezoidal bulk FinFET induced by fin-LER, sidewall-LER, and gate-LER is analyzed. In addition, the sensitivity of DC characteristics induced by the fin height variation is also studied and discussed.

TABLE I. LIST OF THE SIMULATION SETTINGS FOR THE BULK FINFETS

Fin angle θ(°)	70	75	80	85	90
Top fin width W_{top} (nm)	8	8	8	8	8
Bottom fin width W_{bottom} (nm)	19.7	16.6	13.6	10.8	8
Fin height H_{fin} (nm)	16				
Equivalent oxide thickness EOT (nm)	0.5				
Gate length L_g (nm)	14				
Source/Drain Doping (cm^{-3})	1.0E20				
Punch Through Stopper (cm^{-3})	1E19				
Channel Doping (cm^{-3})	1E17				
Drain voltage V_{DD} (V)	0.8				
On-state current I_{on} (A)	3.17E-5	3.12E-5	2.93E-5	2.79E-5	2.63E-5
Off-state current I_{off} (A)	2.9E-10	2.1E-10	1.4E-10	1.0E-10	7.9E-11
On/Off Current Ratio	1.1E5	1.5E5	2.03E5	2.71E5	3.3E5
SS (mV/dec)	77.7	74.4	71.4	68.9	66.7
DIBL (mV/V)	76.2	63.7	53.2	42.9	33.7

II. THE LER SIMULATION METHOD

Fig. 1(a) shows the graphical view of bulk FinFET's structure and the cross-section of fin channel. The fin angle, which is defined as the angle between bottom line and sidewall of fin channel. Table 1 lists the simulation settings for the bulk FinFETs with different fin angle. The top-fin width is fixed and the fin angle ranges from 70° to 90°. Fig. 1(b) shows the LER simulation method, where a time-domain Gaussian noise function is used to generate random edge profiles and then appends them on the regular edges of nominal trapezoidal bulk FinFETs. The standard deviation is set to 1 nm. The magnitude distribution of line edge profiles is followed by Gaussian distribution. To capture devices' characteristic affected by the surface roughness and LER scattering, a normal electric field dependent mobility model is included in the 3D quantum-mechanically corrected device simulation [19]. Figures 1(c)-(f) shows four types how LER affects the fin channel; they are fin-LER by resist-defined process (donated as resist-LER), sidewall-LER, gate-LER, and fin-LER by spacer-defined process (donated as spacer-LER).

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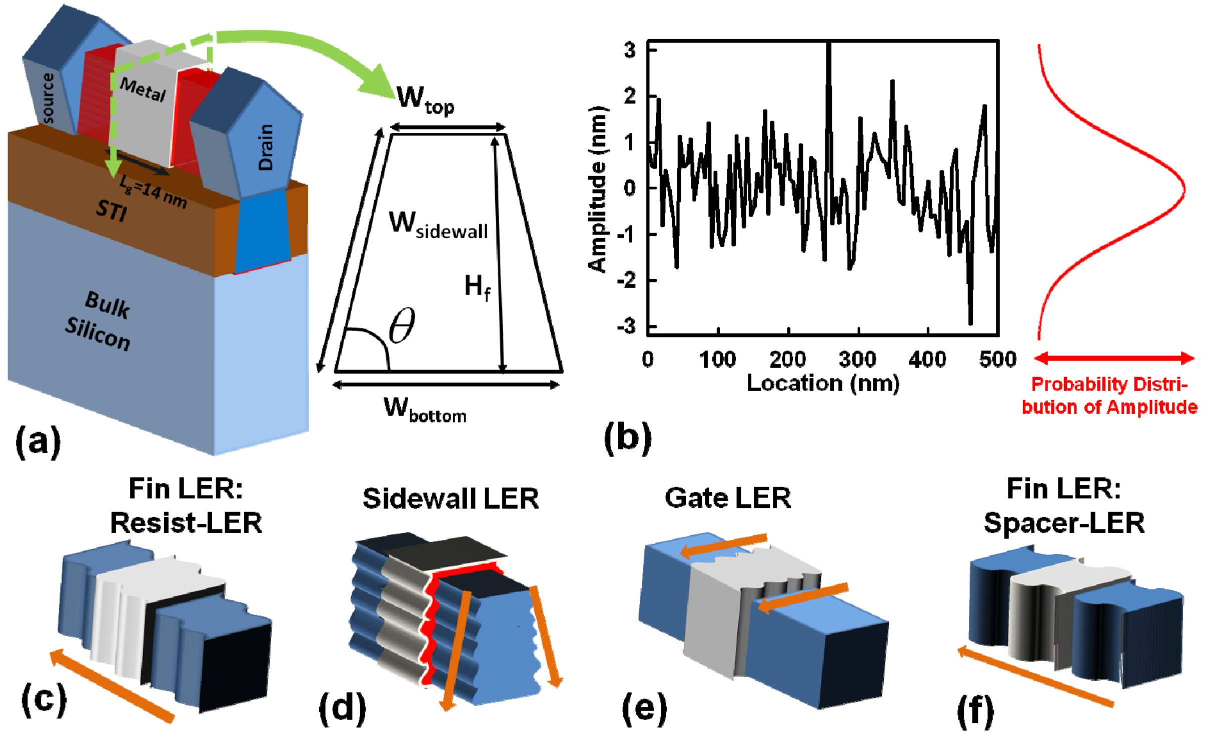

Fig. 1. (a) The bulk FinFET's structure and the cross-section of the fin channel. The impact of the line edge roughness on the electrostatic characteristics variation of the trapezoidal bulk FinFETs with different angles is studied. (b) The simulation method of LER. Time-domain Gaussian noise function is used to generate random edge profiles and then append them on the regular edges of trapzoidal bulk FinFET devices. The standard deviation is set to 1 nm. The distribution of line edge profiles follows Gaussian distribution. (c)-(f) Four LER types: (c) fin LER by resist-defined process (resist-LER); (d) sidewall LER along the fin-height direction; (e) gate LER; and (f) fin LER by spacer-defined process (spacer-LER); on the bulk FinFET device.

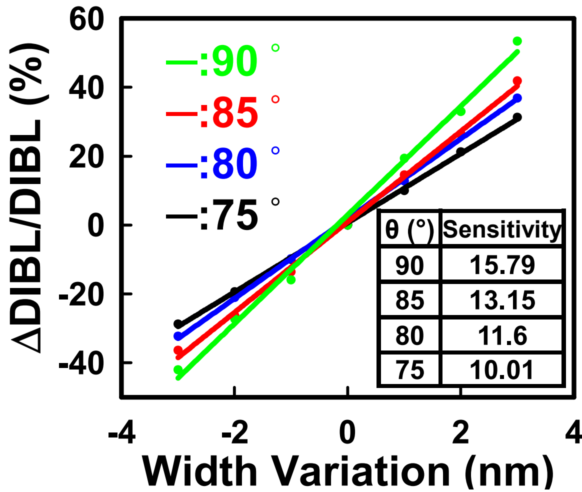

Fig. 2. The DIBL variation versus the fin width variation of the devices with respect to different fin angles. The DIBL variation is getting larger with increasing width because the degradation of gate control.

III. Results and Discussion

Figure 2 shows the drain induced barrier lowering (DIBL) variation versus the fin width variation of the bulk FinFETs with different fin angles. When the fin width is getting larger, DIBL variation is also getting larger because the degradation of gate control. The 90°-bulk FinFET suffers the most serious influence due to the largest variation of inversion charge which gate can control. The DIBL variation of 90°-bulk FinFET is two times larger than that of 75°-bulk FinFET. Overestimation may occur while using an ideal rectangle-channel FinFETs for process variation analysis. Due to the aforementioned characteristic difference in the explored bulk FinFETs with different fin angles and extreme difficulty in fabricating completely ideal 90°-bulk FinFETs, the following discussion will mainly focus on the trapezoidal bulk FinFETs' characteristic variation.

Figure 3 shows the V_{th} fluctuation of the fin-LER inclusive of resist-LER and spacer-LER, sidewall-LER, and gate-LER. The fin-LER is that the fin width varies along the direction from the source side to the drain side. The difference of resist-LER and spacer-LER is the correlation of LER's profiles between two edges of the fin channel. The spacer-LER has almost the same extent of LER at two sides of fin edges [20], which the fin width is identical along the direction from the source side to the drain side. Therefore, the spacer-LER has the same gate control on the entire fin channel. However, for the resist-LER, the LER's profiles are independent between two edges of the fin channel and the fin width varies dramatically. Thus, the gate control would seriously be affected and surface roughness is severe. The sidewall-LER is the fin width variation perpendicular to the direction from the source to drain sides. The gate-LER can be treated as the parallel connection of many FETs with different gate lengths. Among four LER types, the resist-LER is intuitive causing

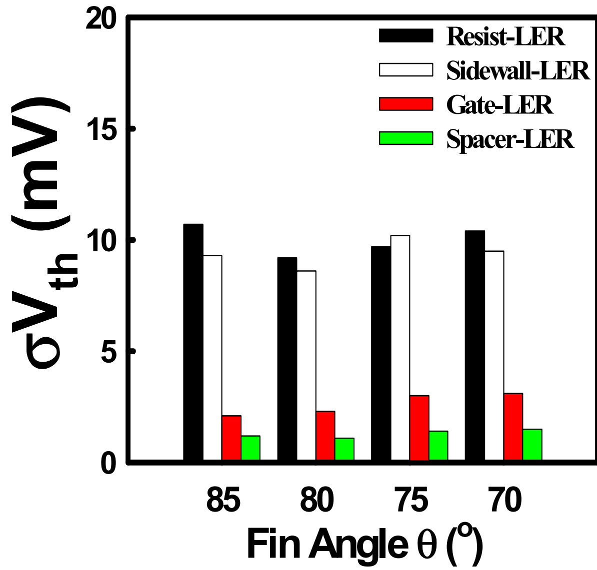

Fig. 3. The V_{th} fluctuation of the resist-LER, sidewall-LER, gate-LER, and spacer-LER. Among four types LER, the resist-LER and sidewall LER would cause sizeable surface roughness scattering, which may reduce the carrier's mobility and increase characteristic variation.

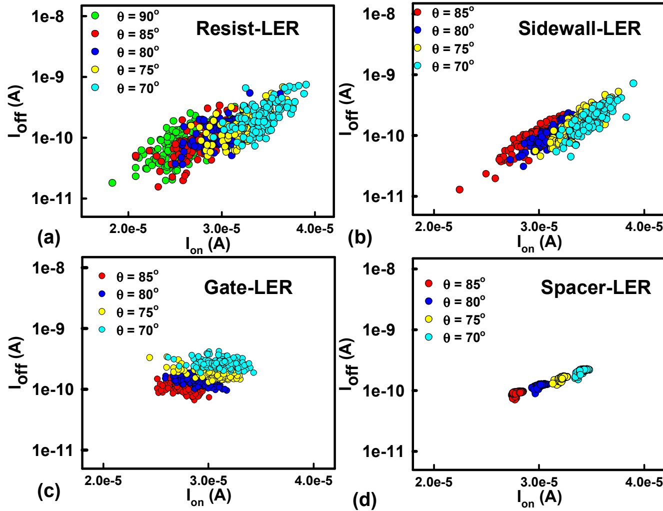

Fig. 4. The I_{on}-I_{off} characteristics of the bulk FinFET devices with respect to different fin angles under the (a) resist-LER, (b) sidewall-LER, (c) gate-LER, and (d) spacer-LER. The bulk FinFETs with a larger fin angle has small on-state current due to the small effective width, however, the on-/off-state current ratio is better because the off-state current can be significantly reduced by good gate control of narrow fin width.

carriers suffer the surface roughness scattering. For the sidewall-LER, because of the coupling of electric field from the top gate and the lateral gates, the carriers do not flow from the source side to the drain side straightly. Therefore, conduction carriers also suffer considerable surface roughness scattering compared with the resist-LER. However, the seriousness of the surface roughness scattering is almost the same for the bulk FinFETs with the same fin width, the gate-LER and spacer-LER has slight V_{th} fluctuation. And, the spacer-LER causes the smallest V_{th} fluctuation of all. From

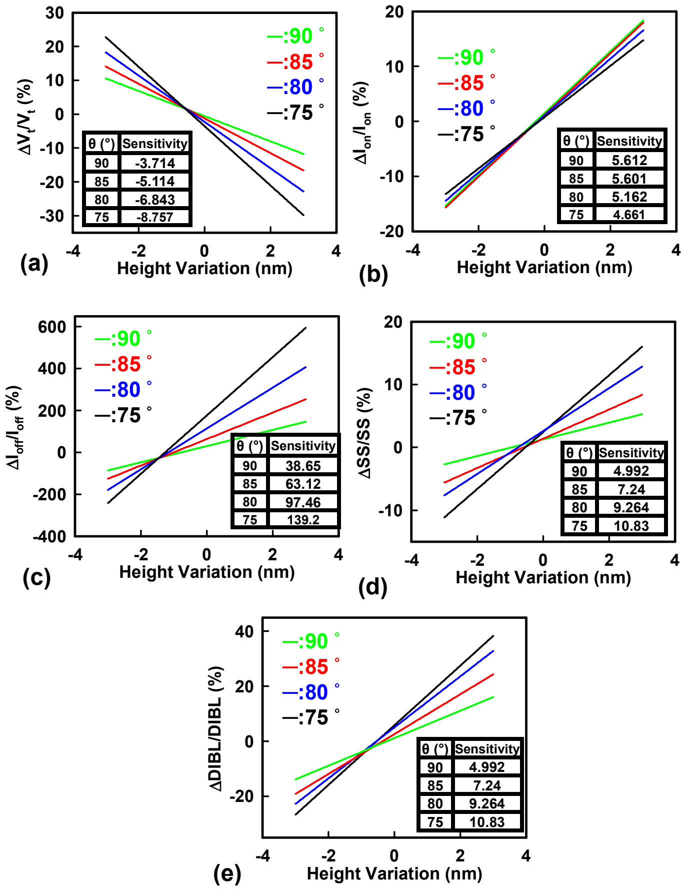

Fig. 5. The fin height sensitivity analysis of the studied bulk FinFETs with respect to different fin angle. A larger channel fin height means a larger effective width, therefore, the conduction current would be increased and V_{th} is decreased. The slight variation of on-state current and the sharp variation of the off-state current would give rise to the increasing trend of SS variation when the fin height is getting larger. The DIBL variation is increasing when the fin height increases.

Fig. 3, the comparable V_{th} fluctuation in each type of LER among the bulk FinFET with respect to different fin angle can be observed.

The I_{on}-I_{off} characteristics of the bulk FinFET devices with different fin angles under the resist-LER, sidewall-LER, gate-LER, and spacer-LER are shown in Figs. 4(a)-(d), respectively. For bulk FinFETs with a larger fin angle has small on-state current due to the small effective width, however, the on-/off-state current ratio is better because the off-state current can be significantly reduced by good gate control of narrow fin width.

Figure 5 shows the fin height sensitivity analysis of the bulk FinFET devices with different fin angles. A larger channel fin height means that a larger effective channel width, therefore, the current would be increased and V_{th} is decreased when using a constant current method to extract V_{th}. The slight variation of the on-state current and the sharp variation of the off-state current would give rise to the increasing trend of SS variation when the channel fin height is getting larger. The

DIBL variation is also increased when the channel fin height increases. Compared with the nonideal trapezoidal bulk FinFETs in real world, relatively small variation of the ideal 90°-bulk FinFET in V_{th}, DIBL, and subthreshold swing (SS) with respect to the fin height is estimated. The sizeable underestimation should be modeled in FinFET circuit design.

IV. CONCLUSIONS

In summary, the fin-LER inclusive of resist-LER and spacer-LER, sidewall-LER, and gate-LER on trapezoidal bulk FinFET devices with different fin angles have been analyzed. The resist-/sidewall-LER induces large V_{th} fluctuation. the comparable V_{th} fluctuation in each type of LER among the bulk FinFET with different fin angle can be observed. The on-/off-state current ratio is better in the bulk FinFETs with a larger fin angle. Notably, the fin height variation would lead to considerable characteristic variation of trapezoidal bulk FinFETs. Notably an ideal 90°-bulk FinFET has relatively smaller sensitivity of V_{th}, SS, and DIBL and would underestimate the process variation effect on device characteristic variability.

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