Monte Carlo Simulation of InAlAs/InGaAs HEMTs with Various Shape of Buried Gate

Akira Endoh[1,2], Issei Watanabe[1], Akifumi Kasamatsu[1], and Takashi Mimura[1,2]
[1]National Institute of Information and Communications Technology, 4-2-1 Nukui-kitamachi, Koganei, Tokyo 184-8795, Japan
[2]Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0197, Japan
E-mail: aendoh@nict.go.jp, aendoh@jp.fujitsu.com

***Abstract*—We carried out Monte Carlo (MC) simulation of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ high electron mobility transistors (HEMTs) with various shape of buried gate. Especially, we examined the HEMT with a "realistic" buried gate in which the tip of gate foot is "round." We found that the "effective" gate length is determined by the length of gate foot tip from the electron velocity profiles and electric field in the channel layer. Furthermore, the "round" tip of gate electrode is convenient to prevent breakdown.**

Keywords—HEMTs; Monte Carlo simulation; InAlAs; InGaAs; Buried gate; Gate length; Electron velocity; Electric field

I. Introduction

InP-based $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 0.53$) high electron mobility transistors (HEMTs) are one of the most promising candidates for millimeter-wave (30 to 300 GHz) and sub-millimeter-wave (300 GHz to 3 THz) applications, since these material systems provide high electron mobilities, high electron velocities, and high sheet-electron densities. To achieve higher-speed operations, reducing gate length L_g is a straightforward method. Besides reducing the L_g, the gate-channel distance d must be reduced to suppress the short-channel effects [1]. To reduce the gate-channel distance, the buried gate structure is very effective to achieve high cutoff frequency f_T [2, 3]. There are mainly two methods to reduce d: one is the recessed-gate technology [4] and another is the gate metal sinking process [5]. In these techniques, the fabricated gate foot is not rectangular, i.e. the tip of the gate electrode is "round" as shown in Fig. 1 [4]. Therefore, it is very important to grasp electron transport and potential profile in HEMTs with nonrectangular gate foot. Furthermore, recent progress in electron beam (EB) lithography enables us to fabricate sub-10-nm-long gate electrodes. Therefore, we can fabricate an original shape at the gate foot tip.

In this work, we carried out Monte Carlo (MC) simulation of $In_{0.52}Al_{0.48}As/In_{0.53}Al_{0.47}As$ HEMTs with various shape of buried gate. Especially, we examined the HEMT with a "realistic" buried gate in which the tip of the gate foot is round.

II. Monte Carlo Simulation

MC simulations were carried out at a lattice temperature of 300 K by using the program, "COSMOS," developed by Mizuho Information & Research Institute, Inc. [6]. Figure 2 shows a model structure of the HEMT with buried gate. We changed the shape of the buried gate (slanted line region in Fig. 2). The shapes of gate foot are shown in Table I. We used a three-valley model (Γ, L, X) with nonparabolicity for the conduction band structures of $In_{0.53}Ga_{0.47}As$, $In_{0.52}Al_{0.48}As$, and InP layers. $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ layers are lattice-matched to InP layer. The band parameters of AlAs, GaAs, and InP were taken from the literature [7, 8]. On the other hand, the band parameters of InAs were obtained by the calculation results using all-electron full-potential linearized augmented-plane-wave (FLAPW) method in the local density approximation (LDA) [9]. The electron scattering mechanisms [10, 11] considered were polar optical phonon scattering, non-polar optical phonon scattering, acoustic phonon scattering, inter-valley phonon scattering, and ionized impurity scattering. Dirichlet boundary conditions were applied to all metal-semiconductor interfaces, and Neumann boundary conditions

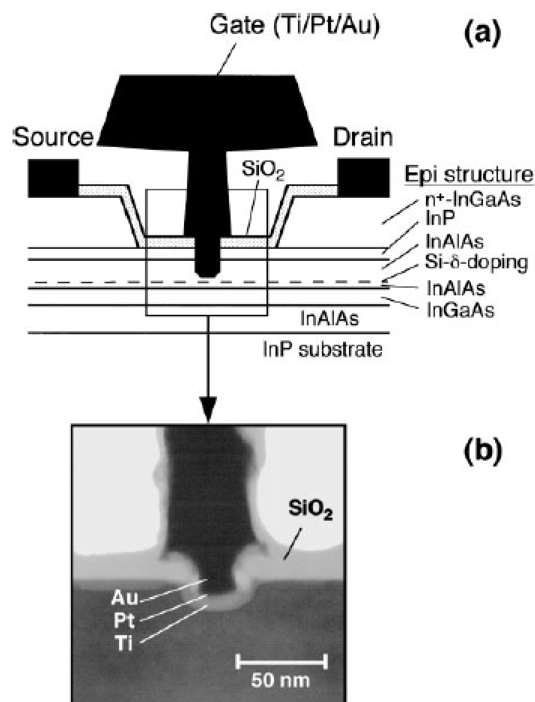

Fig. 1 Schematic cross-sectional view of the HEMT with buried gate (a), and a cross-sectional TEM image around the bottom of the 25-nm-long T-shaped gate of the HEMT (b) [4].

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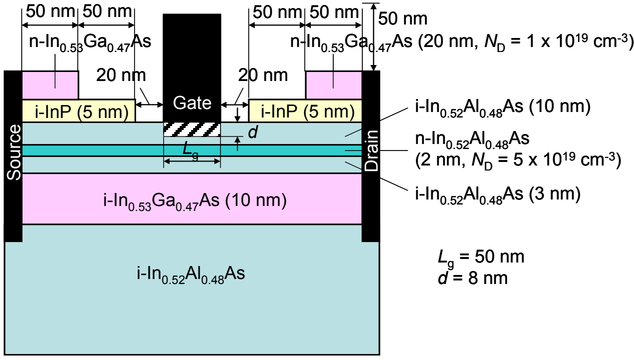

Fig. 2 Schematic cross-sectional model structure of HEMT.

Table I Shape of gate foot (See slanted line region in Fig. 1).

	Shape of gate foot
Model A	8 nm; 50 nm
Model B	4 nm, 4 nm; 10 nm 30 nm 10 nm
Model C	4 nm, 2 nm, 2 nm; 5, 5 nm 30 nm 5, 5 nm
Model D	4 nm, 4 nm; 40 nm 10 nm
Model E	4 nm, 4 nm; 10 nm 40 nm

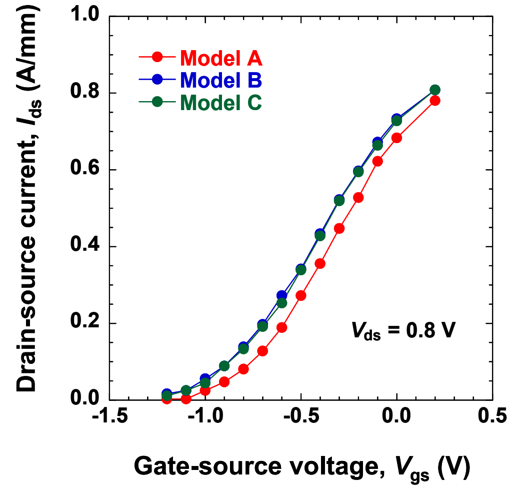

Fig. 3 Drain-source current vs. gate-source voltage (I_{ds}-V_{gs}) characteristics of HEMTs (Models A, B, and C). The drain-source voltage V_{ds} is 0.8 V.

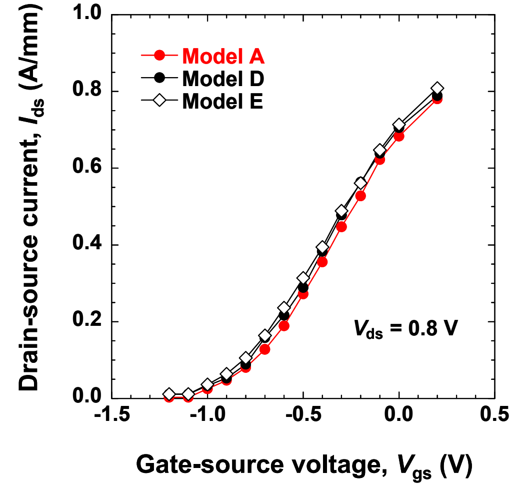

Fig. 4 Drain-source current vs. gate-source voltage (I_{ds}-V_{gs}) characteristics of HEMTs (Models A, D, and E). The drain-source voltage V_{ds} is 0.8 V.

(the zero normal derivative of the potential) were applied to other surfaces. Potential was calculated by the finite difference method. The time step was set to 0.5 fs. The width of gate foot was 50 nm.

III. Results and Discussion

Figure 3 shows the drain-source current vs. gate-source voltage (I_{ds}-V_{gs}) characteristics of Models A, B, and C under a drain-source voltage V_{ds} of 0.8 V. The I_{ds}-V_{gs} curves of Models B and C shift negatively from that of Model A. Note that the significant difference was not observed between Models B and C. To clarify the negative shifts in the I_{ds}-V_{gs} curves of Models B and C, we carried out MC simulations of Models D and E (See Table I). The Models D and E are the part of Model B. Figure 4 shows the I_{ds}-V_{gs} characteristics of Models A, D, and E under a V_{ds} of 0.8 V. The I_{ds}-V_{gs} curves of Models D and E shift negatively from that of Model A. The shift of I_{ds}-V_{gs} curves of Models D and E are almost half of those of Models B and C.

To understand the trend of I_{ds}-V_{gs} curves of the HEMTs, we obtained the electron velocity profile in the channel layer from source to drain. The electron velocity was obtained by taking the average for the whole channel depth of 10 nm. Figure 5 compares the electron velocity profiles in the channel layer of Models A, B, and C under a V_{ds} of 0.8 V and a V_{gs} of -0.3 V. There is a velocity overshoot under the gate electrode. Here, the velocity overshoot regions in Models B and C are smaller than that in Model A. Figure 6 compares the electron velocity profiles in the channel layer of Models A, D, and E under a V_{ds} of 0.8 V and a V_{gs} of -0.3 V. In the Models D and E, the velocity in the region under the "dent" is lower than that in the corresponding region of Model A. From these results, the "effective" gate length is determined by the length of gate foot tip. Therefore, the negative shifts in the I_{ds}-V_{gs} curves result from the short-channel effects [1].

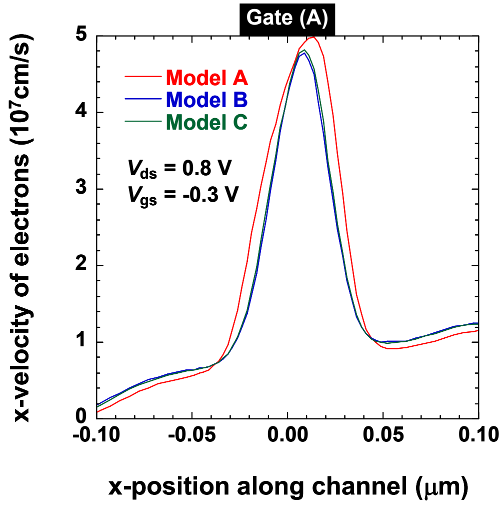

Fig. 5 Electron velocity profiles in the InGaAs channel layer of HEMTs (Models A, B, and C). The drain-source voltage V_{ds} is 0.8 V, and the gate-source voltage V_{gs} is -0.3 V.

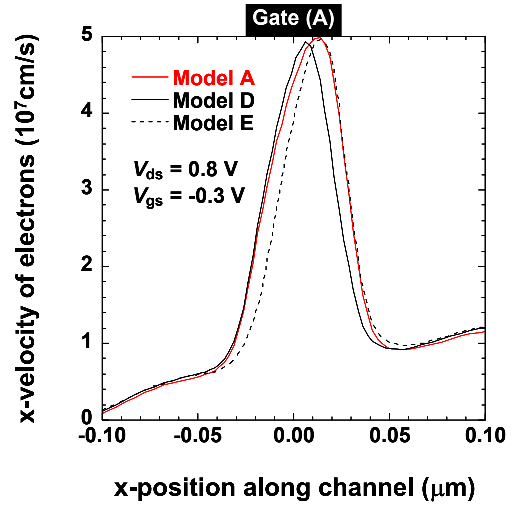

Fig. 6 Electron velocity profiles in the InGaAs channel layer of HEMTs (Models A, D, and E). The drain-source voltage V_{ds} is 0.8 V, and the gate-source voltage V_{gs} is -0.3 V.

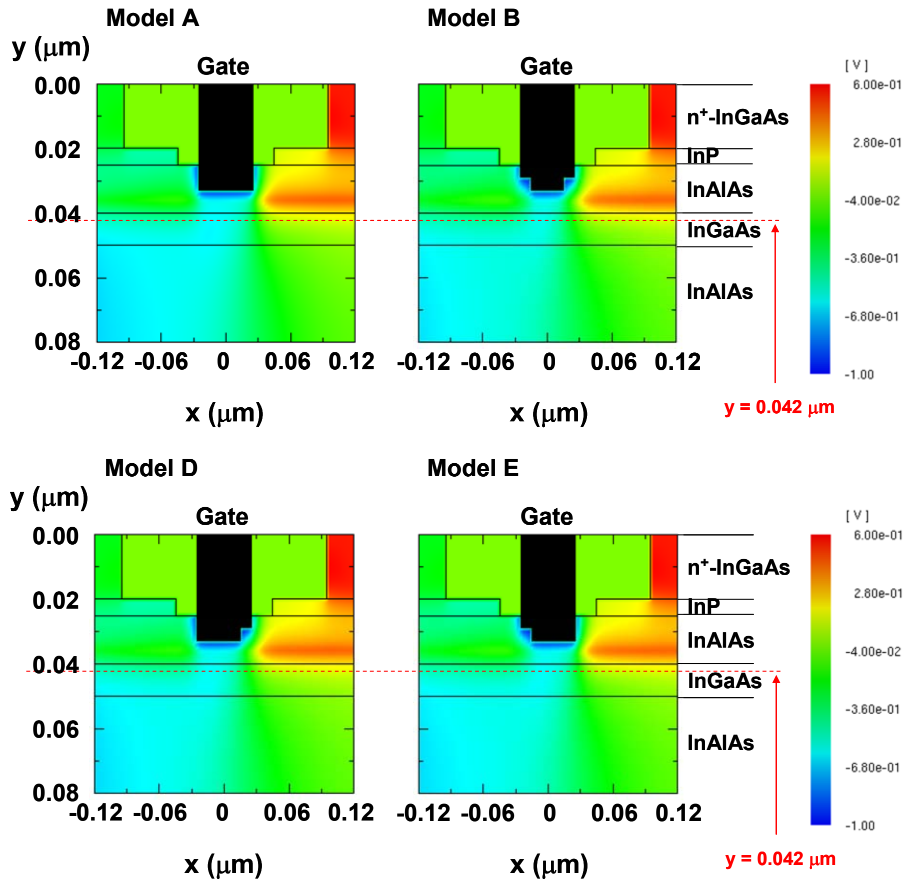

Fig. 7 Potential profiles in HEMTs (Models A, B, D, and E). The drain-source voltage V_{ds} is 0.8 V, and the gate-source voltage V_{gs} is -0.3 V.

Figure 7 shows the potential profiles in the HEMTs of Models A, B, D, and E under a V_{ds} of 0.8 V and a V_{gs} of -0.3 V. Figure 8 shows the one-dimensional potential and electric field profiles along the InGaAs channel layer at y = 0.042 μm in Fig. 7. In Model A, i.e. rectangular gate, the valley of electric field is the source-side edge of the gate and the peak of electric field is the drain-side edge of the gate. On the other hand, the positions of valley and peak shift according to the positions of the "dents" for Models B, D, and E. These results also support that the "effective" gate length is determined by the length of gate foot tip. Furthermore, the electric field at the gate edge in Model B is weaker than that in Model A. Therefore, round tip

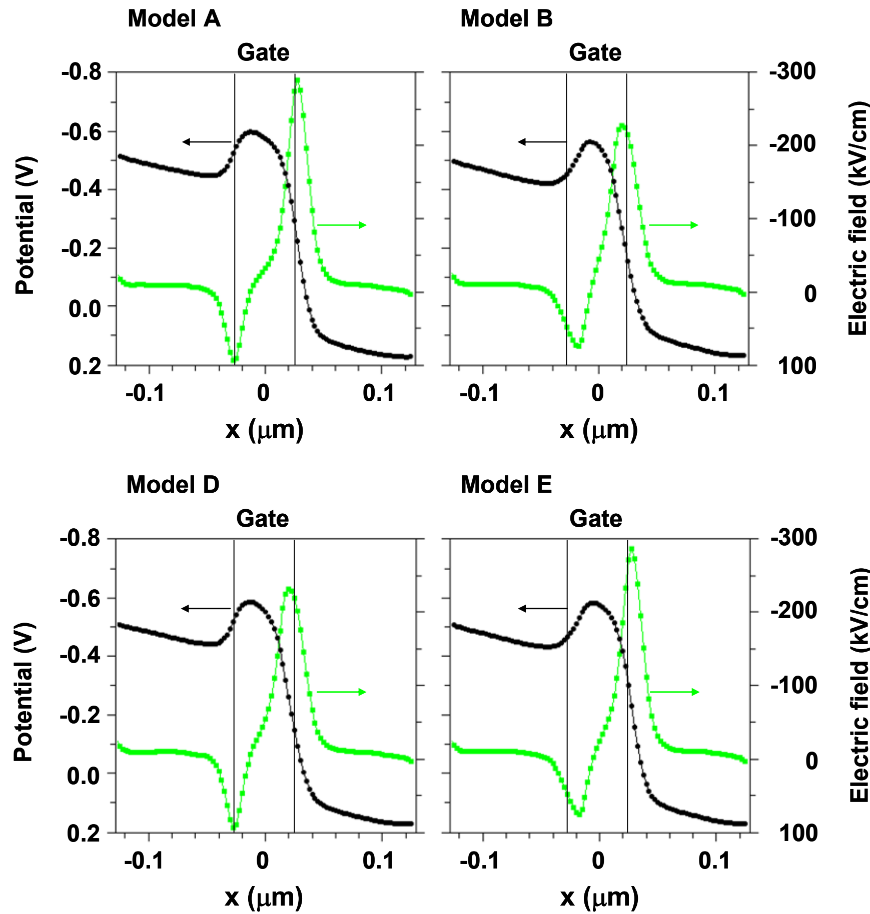

Fig. 8 One-dimensional potential profile and electric field along the InGaAs channel layer at y = 0.042 μm in HEMTs (Models A, B, D, and E). The drain-source voltage V_{ds} is 0.8 V, and the gate-source voltage V_{gs} is -0.3 V.

of gate electrode is convenient to prevent breakdown of HEMTs.

IV. Summary

In summary, we carried out MC simulation of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HEMTs with various shape of buried gate. The I_{ds}-V_{gs} curves shift negatively by the existence of the "dent." From the electron velocity profiles and electric field in the channel layer, the "effective" gate length is determined by the length of gate foot tip. To consider the "effective" gate length is indispensable for designing device structure of HEMTs with buried gate to suppress the short-channel effects. Furthermore, the round tip of gate electrode is convenient to prevent breakdown of HEMTs.

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