MC/DD Study of Metal Grain Induced Current Variability in a Nanoscale InGaAs FinFET

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***Abstract*—The on- and off-current variability due to TiN metal grain workfunction fluctuations in a 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET is analysed using two in-house simulation tools based on the finite element method: a 3D Drift-Diffusion device simulator and a 3D ensemble Monte Carlo simulator, that include quantum-corrections through the density gradient approach.**

The I_D-V_G characteristics have been compared in the sub-threshold region against ballistic NEGF simulations, showing an excellent agreement.

Monte Carlo simulations, considering a $\langle 100 \rangle$ channel orientation, show a larger on-current variability, over a 120% increase, compared with the results from Drift-Diffusion simulations. In this study, three different metal grain sizes (10, 7 and 5 nm) have been analysed. We have observed that the underestimation of the variability when using Drift-Diffusion simulations is increasing with a reduction in the grain size.

I. Introduction

III-V materials are actively considered to replace the Si channel in future digital applications because they have notably higher electron mobility and saturation velocity than Si. However, III-V FinFETs, as any nano-transistor, will be affected by the statistical variability due to random dopant (RD) fluctuations, line-edge roughness (LER), or metal gate workfunction (MGW) variations [1].

In this work, we present a 3D quantum-corrected Monte Carlo (MC) and Drift-Diffusion (DD) simulation study of TiN metal gate workfunction variability in the on- and off-currents of a 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET. Both simulation techniques are based on a tetrahedral decomposition of the simulation domain via the finite element method which allow us to accurately describe the 3D device geometry of the device.

The structure of the paper is as follows. Section II describes the structure of the FinFET device, the main features of the two different simulation techniques employed in the study and the implementation of the MGW variability. Section III presents and analyses the on- and off-current variability results and Section IV summarises the main conclusions of this work.

II. Simulation Methodology

The design of the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET follows the requirements specified by the 2012 ITRS [2] for high-performance logic III-V multigate devices. Table I collects the dimensions, doping concentrations, drain currents and (I_{On}/I_{Off}) ratio for the device with a ideal gate (MGW=4.72 eV). This device has a Gaussian n-type doping profile in the source/drain (S/D) regions and an uniform p-type doping in the channel. The on-current (I_{On}) values are slightly larger than the predicted by the ITRS, since we have not included any contact resistances. The off-state power dissipation is a critical factor for digital applications. The I_{On}/I_{Off} ratio for the 10.4 nm gate length device is close to 10^5 which is acceptable.

TABLE I. Dimensions, doping concentrations, applied drain bias, nominal currents and (I_{On}/I_{Off}) ratio for the simulated devices.

L_G(nm)	10.4	Physical gate length
EOT(nm)	0.59	Equivalent oxide thickness
W_{fin}(nm)	6.1	Fin width
H_{fin}(nm)	15.2	Fin heigth
L_{SD}(nm)	10.4	Length of n-doped S/D regions
N_c(cm^{-3})	10^{17}	Channel p-doping
N_{SD}(cm^{-3})	5x10^{19}	Peak value S/D n-doping
V_D(V)	0.60	Supply voltage
I_{Off-DD}(μA/μm)	0.047	Off-current from DD
I_{On-DD}(mA/μm)	2.36	On-current from DD
I_{On-MC}(mA/μm)	3.19	On-current from MC
I_{On}/I_{Off}	6.8x10^4	(I_{On-MC}/I_{Off-DD}) ratio

The 3D ensemble MC [3] and DD [1] simulators are both based on the finite-element method (FEM), consider Fermi-Dirac statistics (due to the high level of degeneracy of the S/D regions [4]), and include quantum corrections through an optimised FEM density gradient (DG) approach for multi-gate transistors [5]. Quantum corrections are calibrated via the effective masses that characterise the DG solution, which are related to the source-to-drain tunnelling and quantum confinement effects [1]. The electron effective mases in the x-direction were set to $0.175m_0$ and $0.109m_0$ at a V_D of 0.05 and 0.6 V, respectively. In the y- and z-direction, the electron effective masses were fixed to $0.1m_0$ for both analysed drain biases. Fig. 1 shows the I_D-V_G characteristics comparing results from 3D DD-DG simulations against Silvaco's ballistic NEGF data [6] at both low and high drain biases on a logarithmic scale, with an excellent agreement in all the sub-threshold region.

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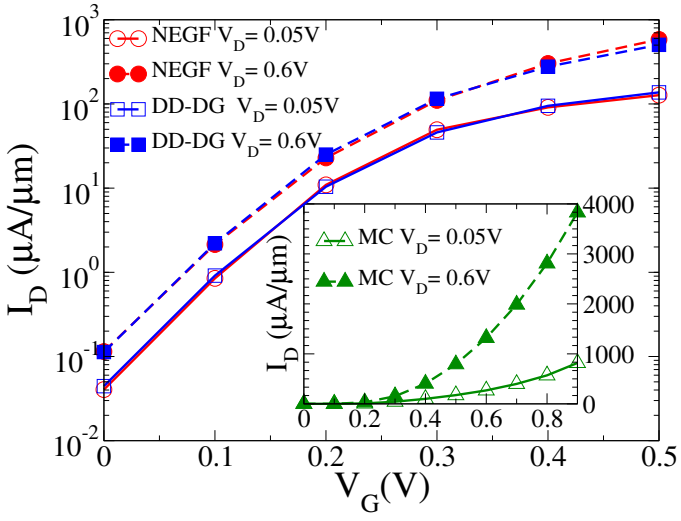

Fig. 1. I_D-V_G characteristics comparing the 3D DD-DG results against Silvaco's ballistic NEGF simulations [6] on a logarithmic scale at both low (0.05 V) and high (0.6 V) drain biases. The inset shows the Monte Carlo results on a linear scale.

The 3D ensemble MC results are also shown in Fig. 1 (see the inset) on a linear scale. The channel orientation is $\langle 100 \rangle$. This MC simulation tool uses an analytic non-parabolic anisotropic model for the dispersion relation in the valleys [7] and includes the interface roughness via Ando's model, described in [8]. The scattering mechanisms considered in the simulator are acoustic phonon scattering, non-polar optical equivalent intra-valley scattering, non-polar optical equivalent inter-valley scattering, ionized impurity scattering using the third-body exclusion model by Ridley [9], optical phonon scattering and alloy scattering [10].

To simulate the TiN metal grains in InGaAs FinFETs [11], we follow the methodology described in [12]. An ensemble of 100 devices, each with a different metal gate work function distribution, was generated and simulated for three different grain sizes (GSs) (10, 7 and 5 nm) at a high drain bias of V_D=0.6 V. Fig. 2 shows an example of a TiN metal gate work function distribution due to MGW variability for a 5 nm average GS. Note that TiN has two possible grain orientations with MGWs of 4.8 and 4.6 eV and probabilities 60% and 40%, respectively [13].

III. Variability Results

Fig. 3 shows the scatter plot of the on-current variation from MC against DD simulations due to MGW variability, for three different GSs. The correlation coefficient between both magnitudes (ρ) has been included for comparison, as well as a linear fitting as guide for the eye. The slope of the fitting is around 2 for the three analysed grain sizes. The corresponding standard deviations of the distributions are given in Table II. MC results show a greater variability, over a 120% increase, compared with the DD. The underestimation of the variability when using DD is increasing with a reduction in the GS. The MC and DD simulation results are strongly correlated with $\rho \sim$0.9 for the three analysed GSs. As expected, the on-current standard deviation decreases with reducing the GS. For instance, the GS reduction from 10 nm to 5 nm reduces the

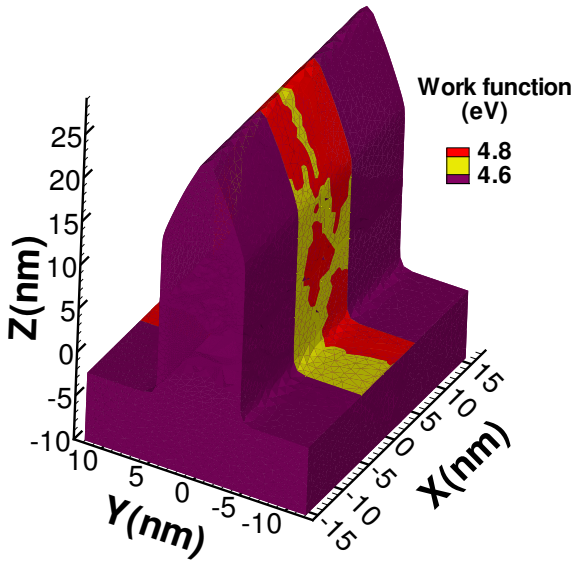

Fig. 2. Example of the TiN metal gate work function variability for a grain size 5 nm. The TiN metal has 2 possible grain orientations with MGWs of 4.8 and 4.6 eV.

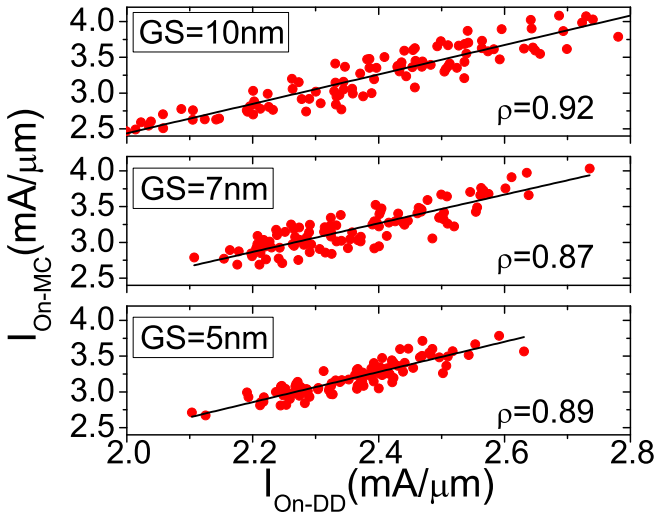

Fig. 3. Scatter plot of the on-current from the MC vs. the DD due to MGW variations for three different grain sizes (GSs). The correlation coefficient (ρ) is shown for comparative purposes.

spread in both I_{On-MC} and I_{On-DD} by approximately 43% and 47%, respectively. The MC simulations, unlike the DD, include the impact of potential variation on non-equilibrium carrier transport due to the statistical MGW induced variability between physically different devices [14].

Fig. 4 shows the on-current distributions as simulated with the MC and the DD for the three analysed GSs. The mean value of the on-current along with the value for a device with the ideal gate (having an uniform MGW) are also shown. For both simulation methods, the on-current distributions are close to a Gaussian behaviour only when the GS is small.

We have defined the on-current shift ($I_{On_{shift}}$) due to MGW variability as the difference between the mean value of the

statistical sample and the value of the magnitude for the device with an ideal gate. When GS=10 nm, the $I_{On_{shift}}$ coming from the MC simulations is 62 μA/μm, a value twice as large as the $I_{On_{shift}}$ coming from the DD simulations. For smaller grain sizes, the on-current shift becomes very small for both simulation techniques (< 10 μA/μm). The large differences in the observed variability between the MC and the DD transport modelling techniques seriously questions the use of the DD technique approach for variability studies on the on-current region often used [15].

Fig. 5 shows a scatter plot of the off-current obtained from the DD against the on-current from the MC for three different GSs for the MGW variability. A linear fitting has been added for comparative purposes. The slopes of the regression line are 1.24, 1.10 and 1.06 for the 10, 7 and 5 nm grain sizes, respectively. There is a strong correlation between the on- and off-currents pointing out that the main effect of the MGW fluctuations is a shift in the I-V characteristics. The corresponding mean value of $\log_{10}(I_{On}/I_{Off})$ ratio for each GS is listed in Table II. Both the off-current and the I_{On}/I_{Off} ratio distributions are close to a log-normal distribution, as seen in Fig. 6 for a 5 nm grain size. Note that, for both magnitudes, there is practically no shift between the the mean value of the statistical distributions and the value for the device with an ideal gate.

The MGW variability strongly affects the I_{On}/I_{Off} ratio of $In_{0.53}Ga_{0.47}As$ FinFET devices. We have observed 45%, 38%, and 30% excursions in I_{On}/I_{Off} when compared to the ideal gate device for the 10, 7 and 5 nm GSs, respectively. When GS=5 nm, the mean value of $\log_{10}(I_{On}/I_{Off})$ is equal to that of the ideal gate device (4.82), as seen in Fig. 6. An increase in the GS produces a slight worsening (less than 5%) in the I_{On}/I_{Off} ratio of the device.

IV. Conclusion

In this paper, we have presented a 3D density-gradient quantum-corrected Drift-Diffusion [5] and Monte Carlo [10] simulation study of the TiN metal gate workfunction variability on the off- and on-currents for a 10.4 nm gate length $In_{0.53}Ga_{0}.47As$ FinFET [1]. Three grain sizes have been considered in this study: 10, 7 and 5 nm which are observed experimentally in TiN metal gates [13]. Both simulators include Fermi-Dirac statistics due to the heavily doped source/drain regions [4]. Quantum corrections are calibrated via the effective masses in x, y and z-directions that characterise the DG approach, which can mimic the source-to-drain tunnelling and quantum confinement effects [5]. MC simulation results show a greater on-current variability, over a 120% increase, compared with DD simulations. We have also observed a strong correlation between the on- and off-currents pointing out that the main effect of the MGW fluctuations is a shift in the I-V characteristics.

Finally, the MGW variability strongly affects the I_{On}/I_{Off} ratio of $In_{0.53}Ga_{0.47}As$ FinFET devices, observing 45%, 38%, and 30% excursions in I_{On}/I_{Off} when compared to the ideal gate device for the 10, 7 and 5 nm grain sizes, respectively.

TABLE II. Off- and on-current standard deviations from MC (I_{On-MC}) and DD (I_{On-DD}) and the mean value of the I_{On}/I_{Off} ratio due to MGW variability for 10, 7 and 5 nm metal grain sizes (GSs).

GS	$\sigma(I_{On-MC})$ (μA/μm)	$\sigma(I_{On-DD})$ (μA/μm)	$\sigma(\log_{10}(I_{Off-DD}))$	$\log_{10}(I_{On}/I_{Off})$
10	422	191	0.577	4.69
7	302	131	0.408	4.78
5	238	101	0.299	4.82

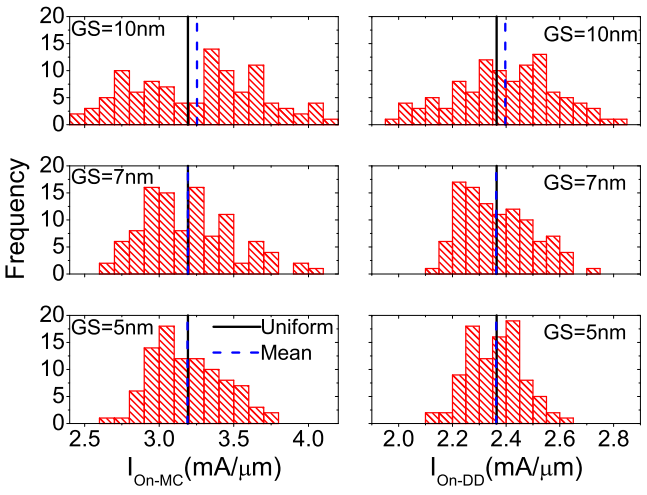

Fig. 4. Distribution of on-currents from MC (I_{On-MC}) and DD (I_{On-DD}) simulations due to MGW variability for three different grain sizes. The on-current for a device with an uniform gate and the mean value of the statistical distribution are included for comparison.

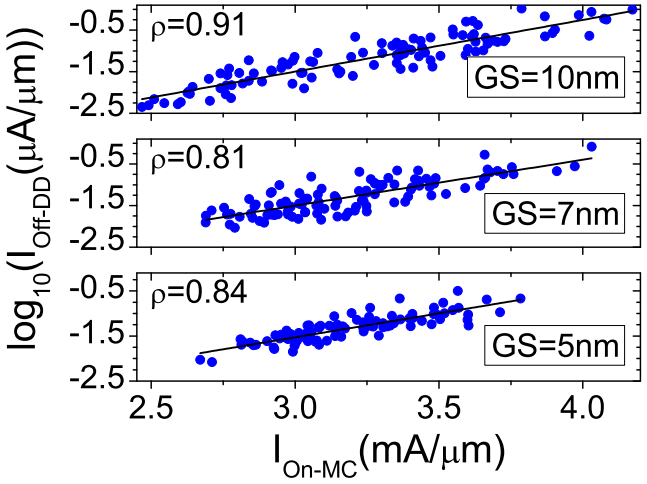

Fig. 5. Scatter plot of the off-current from DD vs. the on-current from MC due to MGW variations for three different grain sizes. The correlation coefficient (ρ) is shown for a reference.

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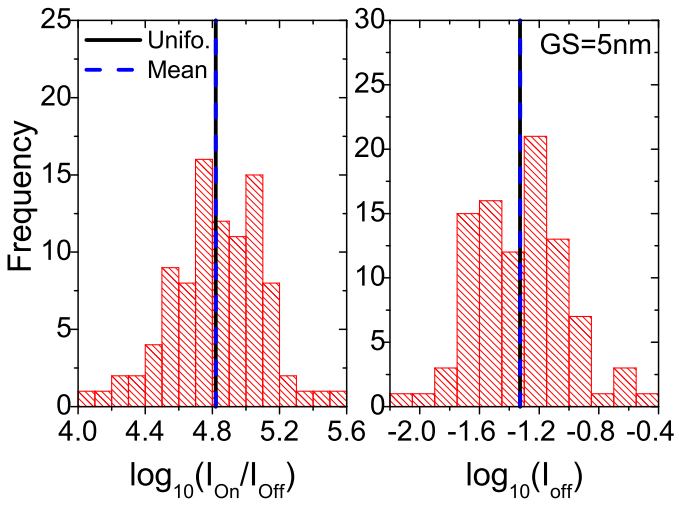

Fig. 6. Distribution of the I_{On}/I_{Off} ratio and of the off-currents from DD simulations due to MGW variability for a grain size 5 nm. The value for a device with an uniform gate and the mean value of the statistical distribution are included for comparison.

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