Nano-meter Scaled Gate Area High-K Dielectrics with Trap-Assisted Tunneling and Random Telegraph Noise

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***Abstract*—If the trap density is 10^{12}cm^{-2}, then there are only one trap in 10nm × 10nm on average. Accordingly, three-dimensional simulation that is sensitive to the movement of sole electron is indispensable for carefully investigating the reliability issues related to local traps in future nano-electron devices. As a demonstration, we investigate Random Telegraph Noise (RTN) and Trap-Assisted Tunneling (TAT) at the same moment in 5nm×5nm gate area high-K dielectrics (EOT= 0.8nm to 0.47nm). The simulation is carried out with respect to various gate biases, physical thickness of high-K, interlayer suboxide thickness, and dielectric constant of high-K. It is suggested that thinner suboxide and higher permittivity can suppress the increase of the leakage current which is caused by TAT.**

Keywords-single-electron; simulation; random telegraph noise; trap-assisted tunneling; high-K dielectrics; interlayer suboxide

I. Introduction

Aggressive device scaling has encouraged the careful study of high-K gate dielectric for reducing the gate leakage current. Among the literature, Random Telegraph Noise (RTN) and Trap-Assisted Tunneling (TAT) in high-K gate stack is discussed in [1]-[4]. The basic idea is to model RTN by using the ratio of capture time and emission time via trap with regard to gate voltage (V_g). This ratio is determined by the tunneling from/to trap; which is sensitive to the location of trap, the trap level, and the gate stacks structure as well as V_g. Firstly, an electron tunnels from Si substrate to a local trap inside gate stack. Next, this electron, generally, has three opportunities: 1) Tunneling back to Si. 2) Tunneling to gate. 3) Staying at the trap. The RTN is caused by 1). The trap-assisted tunneling is caused by 2). The fixed charge is caused by 3). The TAT should be avoided in order to reduce the gate leakage current. It is convenient to distinguish these processes 1), 2), 3), at given condition characterized by V_g, the dielectric constant of high-K film (K), the interlayer (IL) suboxide thickness (t_{SBO}), and the equivalent oxide thickness (EOT).

II. Simulation

Note here that trap is “located” at a position inside gate stack, as illustrated in Figure 1 (Left). If one-dimensional (1D) simulation is adopted, the trap would be regarded as a sheet, as illustrated in Figure 1 (Right). These are quite different as long as gate area is very small (e.g., less than 100nm^2). If gate area is large enough, then we can regard many local traps as extensively distributed in plane; which can validate 1D simulation model illustrated in Figure 1 (Right). This cannot, however, represent “local” trap in deca-nanoscale device structure; via which electrons can be captured (trapped) and emitted (detrapped) repeatedly. Thereby, electron’s tunneling from/to trap should be calculated in three-dimensional (3D) simulation. It should be noted that the emission/capture rate of electrons via local trap is sensitive to the trap level; which can rise by more than 100 mV while an electron is stored in trap [5], [6]. According to the International Technology Roadmap for Semiconductors (ITRS) [7], the equivalent oxide thickness (EOT) for high-performance devices will reach 0.8 nm, 0.62 nm and 0.47 nm in 2015, 2020, and 2025 respectively. In lower power branch, the EOTs are 0.9 nm, 0.7 nm, and 0.57 nm in 2015, 2020, and 2025, respectively. In this work, we use the simulation samples of EOT = 0.8nm, 0.62nm, and 0.47nm with K being from 9 to 60, respectively, as shown in Figure 2. The thickness of high-K films (t_{HK}) is determined by the following equation:

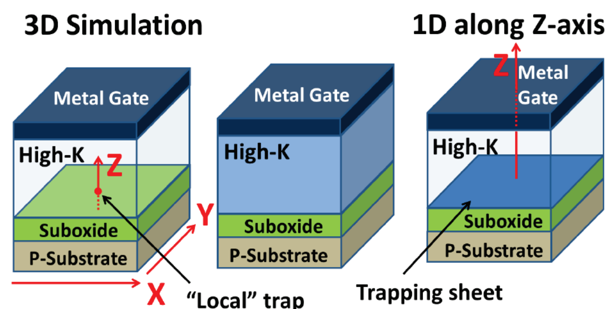

Figure 1: Difference between 3D simulation and 1D simulation for a local trap in the high-K gate stack of P-Si substrate, interlayer (IL) suboxide, high-K film, and Al metal gate.

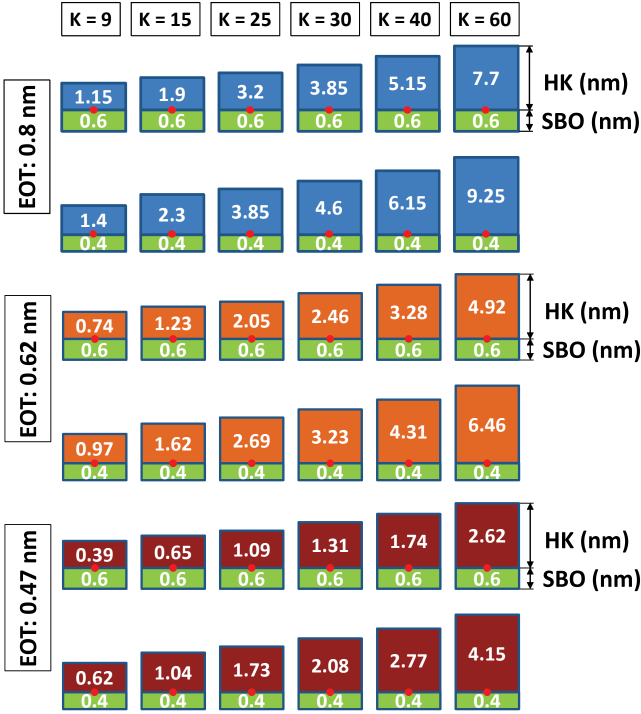

Figure 2: Gate stack structure of high-K (HK) dielectrics, interlayer suboxide thickness (SBO) and a trap located (depicted by dot) on the boundary between interlayer suboxide and high-K film

$$t_{HK} = K \times \left(\frac{EOT}{K_{OX}} - \frac{t_{SBO}}{K_{SBO}} \right) \quad (1)$$

where K_{OX} is the dielectric constant of SiO_2, and K_{SBO} is the dielectric constant of IL suboxide. The K_{OX} is 3.9 and K_{SBO} is the average of K_{OX} and K. We simulate two cases of t_{SBO} which are 0.4 nm and 0.6 nm. By way of example, we may consider an acceptor type single level trap; which can be occupied by at most two electrons owing to spin freedom. The charge states should be −2q, −q, and zero with respect to the number of trapped electrons, where q is the elementary charge. The trap level rises by the decrease of potential of local trap while an electron is stored in trap. The calculated 3D potential profiles with two electrons, one electron, and no electron in trap, are shown in Figures 3-5. We can find the potential drop at trap is about 330 mV (250mV+80mV) when one electron tunnels into a neutral trap and is about 140 mV (−80mV+220mV) when another electron tunnels into the same trap. The right of Figure 6 illustrates the band structure of high-K gate stacks, which is necessary to calculate the tunneling rate. The barrier height (ϕ_B) and electron affinity (EA) are determined according to [5] and [8]. Firstly, we can determine the barrier height between metal

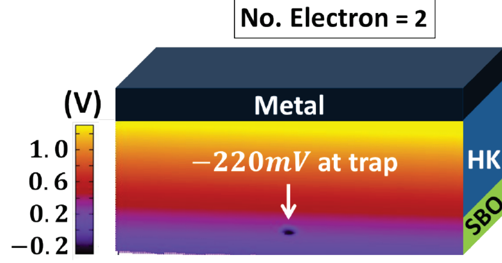

Figure 3: Potential profile at the cross section where a trap is located with K=60 and V_g=1.3 V and occupied by two electrons.

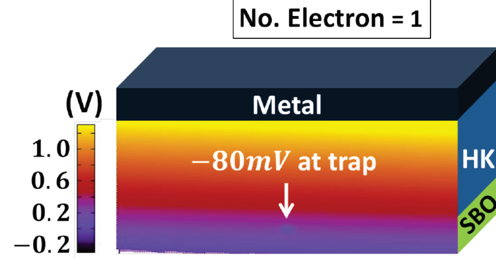

Figure 4: Potential profile at the cross section where a trap is located with K=60 and V_g=1.3 V and occupied by one electron.

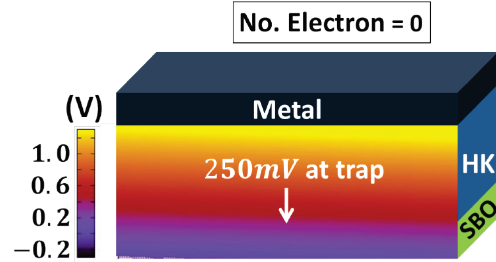

Figure 5: Potential profile at the cross section where a trap is located with K=60 and V_g=1.3 V and occupied by no electron.

gate and the high-K material by the difference of metal work function (4.06eV for Al) and high-K's electron affinity. At equilibrium condition, the Fermi level is flat from metal gate to Si substrate. The barrier height between high-K and P-substrate is $\phi_B(K)$. The parameters used in the simulation are listed in table 1. The tunneling current formula used here is same as [5], [6]. Firstly, we search for tunnel paths; along which electrons tunnel with the tunneling probability (T) being calculated by using the WKB approximation as follows:

$$\ln(T) = -\frac{4}{3\hbar}\sqrt{2m^*}\,\frac{t^*}{\phi_2 - \phi_1}\left[(\phi_2 - E)^{3/2} - (\phi_1 - E)^{3/2}\right] \quad (2)$$

where ϕ_1 is the barrier height at the start of the tunneling path, ϕ_2 is the barrier height at the end of the tunneling path, E is the energy of the tunneling electron, m^* is set to $0.85m_0$ [9] where m_0 is the electron rest mass, and t^* is the length of the tunnel path. If an electron is captured by trap as a result of tunneling from Si to trap, the trap level rises by more than 100 mV. This potential difference substantially affects the direction of the subsequent tunneling from the trap. As illustrated in the left of Figure 6, RTN is a repeated process of electron's tunneling from Si to trap and from trap to Si. The TAT is a sequential tunneling of electron from Si to trap and then trap to gate. If V_g is made higher, the tunneling from trap to gate is enhanced; then TAT may be prior to RTN. If K is made higher, the electric field across high-K film is weakened and physical thickness of gate stack is increased at same EOT; then RTN may be prior to TAT at given EOT. We then perform 3D simulations with three different EOTs, which are 0.8 nm, 0.62 nm, and 0.47 nm. The results are shown in Figures 7-9, respectively. The label R^1 represents RTN process during which the number of electrons in trap varies like: $0 \rightarrow 1 \rightarrow 0$ and R^2 represents RTN process during which the number of electrons in trap varies like $1 \rightarrow 2 \rightarrow 1$. The labels T^1 and T^2 represent TAT process during which the number of electrons in trap varies like: $0 \rightarrow 1 \rightarrow 0$ and $1 \rightarrow 2 \rightarrow 1$, respectively. For example, let us look at the case of EOT=0.62nm, SBO = 0.6nm, K = 40, and V_g = 1.1V in Figure 8. An electron firstly tunnels into the trap; and then we calculate the emission time to gate (9.52 fs) and the emission time back to substrate (7.59 fs). Therefore, RTN (R^1) is prior to TAT. As V_g is increased from 1.1 V to 1.3 V, the emission times of tunneling to gate and back to substrate become 9.56 fs and 10.83 fs, respectively. Then, TAT (T^1) prevails. By this way, we can obtain a chart map to distinguish the boundary between RTN and TAT, as shown in Figures 7-9. Here note that RTN and TAT cannot occur at the same moment. We can also find that for low gate bias and large EOT/SBO ratio, only T^1 or R^1 occurs, but when the voltage becomes higher and EOT/SBO ratio becomes smaller, T^2 starts to occur. This is determined by the energy levels of trap and substrate. We note that when the first electron tunnels from the substrate into the trap, the trap level is increased about 0.3eV. In the low gate bias and large EOT/SBO ratio condition, the voltage drop across the SBO region is small and the trap level will become higher than the energy level of the substrate when one electron tunnels into the trap. Therefore the next tunneling from substrate is impeded and the trapped electron will tunnel out to the gate or back to the substrate; and then causing the T^1 or R^1 case. On the other hand, for the high gate bias and small EOT/SBO ratio condition, the voltage drop across the SBO region is large; therefore the one electron trap level will still be lower than the energy level of the substrate, then the next tunneling to trap is possible; which may cause T^2 or R^2. It is also noted that when the inversion layer is made at the surface, the second tunneling from substrate to trap is likely to be dominant because of more tunneling electrons under the high gate bias and small EOT/SBO ratio condition.

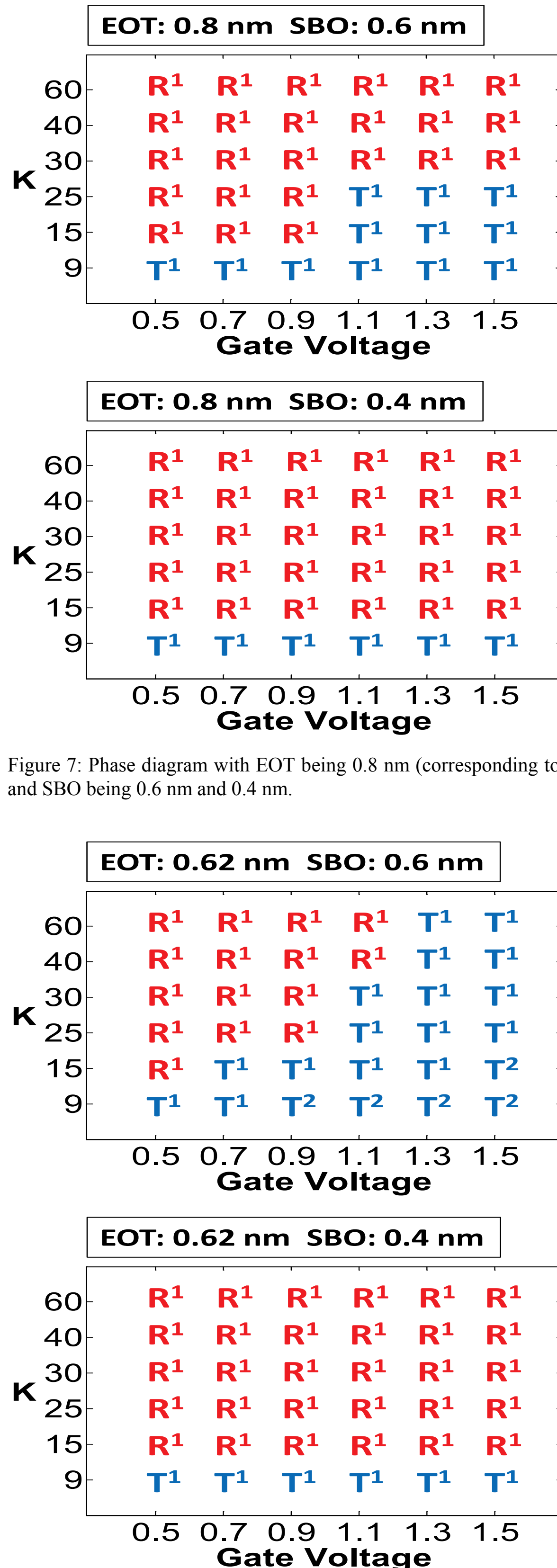

Figure 7: Phase diagram with EOT being 0.8 nm (corresponding to 2015) and SBO being 0.6 nm and 0.4 nm.

Figure 8: Phase diagram with EOT being 0.62 nm (corresponding to 2020) and SBO being0.6 nm and 0.4 nm.

Table 1 Parameter list for various high-K materials.

	Permittivity	*Gap (eV)*	*EA (eV)*
TiO_2	20-80	3.05	3.9
La_2O_3	30	6	2
HfO_2	25	6	2.5
Y_2O_3	15	6	2
Al_2O_3	9	8.8	1

$$\phi_B(K) = exp(-0.053K + 1.42) \text{ (eV) [5]}$$

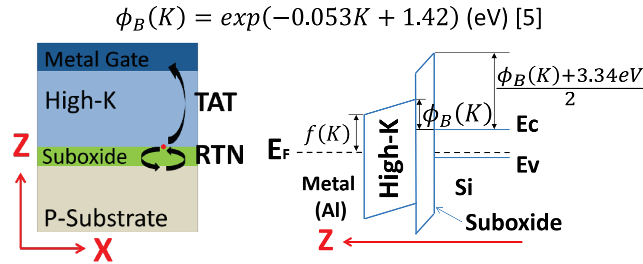

Figure 6: The Z-X cross-section illustrating TAT and RTN via local trap (depicted by dot) in the left hand side and the corresponding energy band diagram along Z-axis in the right hand side. The *f*(K) is the difference between Al's work function (4.06 eV) and high-K's electron affinity. The dielectric constant in interlayer suboxide is (K + 11.7)/2, where 11.7 is Si's dielectric constant. The 3.34 eV is the oxide barrier height [5].

III. SUMMARY

Trap-related phenomena are discussed by taking into account trap level fluctuation by sole electron movement via trap inside high-K gate stack. As a result, we obtained a chart map to distinguish which prevails, --- RTN or TAT, with regard to various K, Vg, and SBO. To avoid TAT, it is preferable to reduce the interlayer suboxide thickness. In particular, when EOT is 0.47 nm (2025 in ITRS), TAT can be suppressed even at K=30 and Vg=1V, as long as the interlayer suboxide thickness is less than 0.4nm. Otherwise, it is difficult to suppress TAT even though K is larger than 60. This is because the physical thickness of high-K film is decreased when EOT becomes smaller. Additionally, the trap level rises by more than 100 mV if an electron is stored in trap; which substantially increases the tunneling rate to gate.

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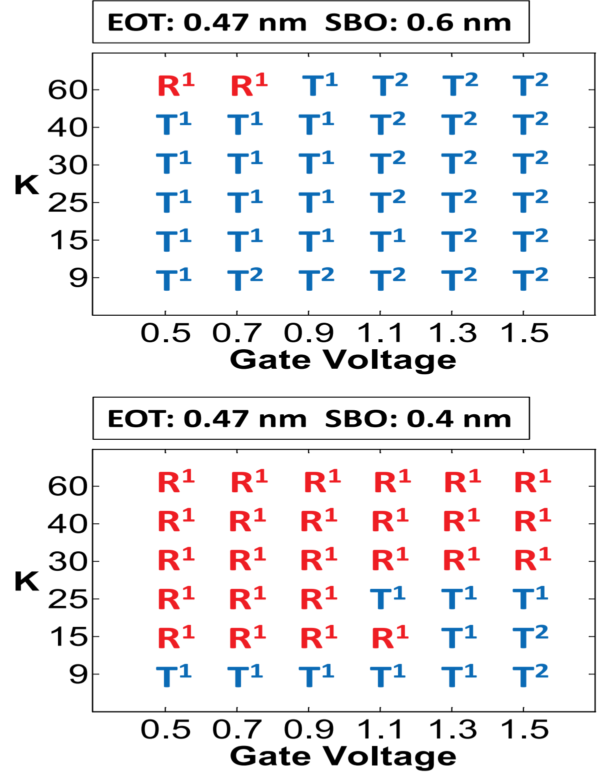

Figure 9: Phase diagram with EOT being 0.47 nm (corresponding to 2025) and SBO being 0.6 nm and 0.4 nm.

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