Optimization of Si MOS transistors for THz detection using TCAD simulation

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***Abstract*—We present a TCAD simulation study for Silicon MOSFET terahertz detectors. The impact of transistor doping profile optimization on detector performance is analyzed. Time-domain simulations are used to extract the DC response to THz excitations and to explore the impact of different device parasitics. It is shown that the DC response can be improved by (1) minimizing the source-side parasitic resistance (2) maximizing the drain-side parasitic resistance and (3) minimizing the drain-to-body and channel-to-body capacitances.**

I. Introduction

Operating frequencies of transistors are generally considered to be limited by the their transit frequency f_T and their maximum frequency for power amplification f_{max}. However, active research in recent years has established that Si MOS transistors can be used as power detectors for electromagnetic waves up to frequencies in the THz range, i. e. far beyond their f_T and f_{max} . The detection is based on self-mixing of THz signals in the transistor channel resulting in a photoresponse in the form of a DC voltage proportional to the power of incident radiation [1]. Based on this principle, a 1k pixel video camera for 0.7- 1.1 THz imaging application has been recently realised using 65 nm CMOS technology [2].

The transistor operation in THz power detectors differs fundamentally from the operation in typical digital and analog circuits. Therefore, it should be expected that the optimum transistor design for THz detectors is different from that of the standard CMOS transistors. Device simulations to study the impact of transistor geometries and doping profiles on the performance of THz detectors can be very useful and such analysis can be used to suggest improvements in transistor design.

In this work, we have done detailed TCAD simulations to study of the impact of NMOS transistor design and doping distribution on detector performance. Extensive time-domain simulations have been used to obtain the THz response and the impact of different device parasitics on this response has been analyzed. This paper is organised in five sections. Carrier dynamics for THz detection is discussed in Section II. The simulation procedure is outlined in Section III. Simulation results and analysis are presented in Section IV followed by conclusions in Section V.

II. Carrier Dynamics

Mixing of THz waves in a transistor channel is generally described with the help of 1D Euler equation for carrier dynamics and current continuity [3] given as,

$$\frac{\partial v}{\partial t} + v\frac{\partial v}{\partial x} + \frac{q}{m}\frac{\partial U}{\partial x} + \frac{v}{\tau} = 0 \tag{1}$$

$$\frac{\partial n}{\partial t} - \frac{1}{q}\frac{\partial j_n}{\partial x} = 0 \tag{2}$$

where U, $\partial U/\partial x$ and v are the local potential, local electric field and electron velocity in the channel respectively, q and m are the electron charge and effective mass, τ is the momentum relaxation time, n is the electron concentration and j_n is the current density due to electrons. These equations differ from the system of drift-diffusion equations typically used in device simulations by the appearance of the first two terms in equation (1). The term $\partial v/\partial t$ accounts for the force of inertia and $v\,\partial v/\partial x$ refers to convection current.

The critical parameter controlling the relative importance of the first two terms in equation (1) is the product of the excitation frequency ω and the momentum relaxation time τ. When the momentum relaxation time of electrons is much smaller than the fundamental time period of incident radiation, i.e. $\omega\tau \ll 1$, the first two terms in equation (1) become negligible [4], [5]. In this scenario, equation (1) reduces to the drift equation

$$\mu\frac{\partial U}{\partial x} + v = 0 \tag{3}$$

with the mobility defined as $\mu = q\tau/m$. In silicon transistors, τ is in the order of $10^{-14}\,s$ and the condition $\omega\tau \ll 1$ holds up to several THz. Therefore, we use here the Drift-Diffusion (DD) transport model for the simulation of THz detection.

III. Simulation Procedure

Figure 1(a) shows the biasing scheme for the device optimization study presented here. The RF signal from the antenna is coupled to the gate terminal and modeled as a sinusoidal AC voltage source with amplitude V_{RF} and frequency ω. V_{RF} is 10 mV for all simulations unless otherwise stated. A DC gate bias V_g is also provided. Source and substrate terminals are grounded and the drain voltage (V_d) is measured with zero drain current boundary condition (open drain). Note that experimentally studied detectors have also used alternative circuit topologies [2]. For differential detector circuits such as those investigated in [2], the optimum transistor design could differ from the one presented here.

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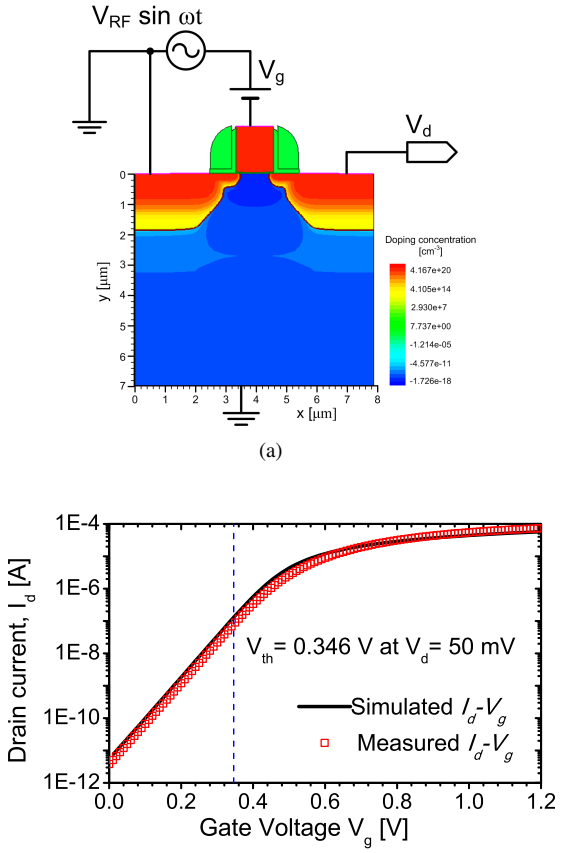


Fig. 1. (Color online) Simulation setup: (a) Biasing scheme. IHP $0.13\mu m$ NMOS is defined using process simulation. THz excitation is modeled as a sinusoidal voltage source with gate coupling. Response is measured at open-drain boundary conditions. V_{RF} = 10 mV for all measurements. (b) Transfer characteristics for simulated versus real device at V_d = 50 mV. Threshold voltage V_{th} is 0.346 V.

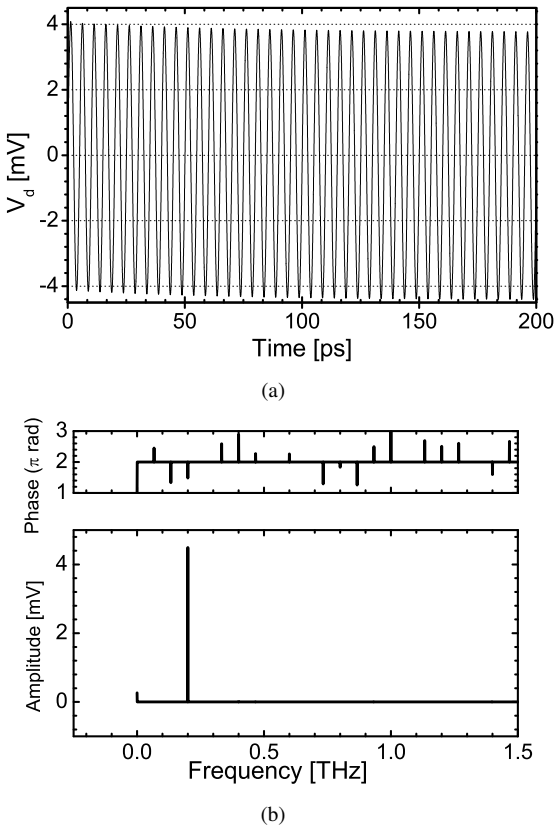


Fig. 2. Quasi-continuous time domain simulation results: (a) Open drain response for 0.2 THz excitation at V_g = 0.4 V. A settling time of about 130 ps can be noticed. (b) Fourier transform for steady state response with both amplitude and phase information. Fundamental harmonic as well as DC photoresponse can be observed.

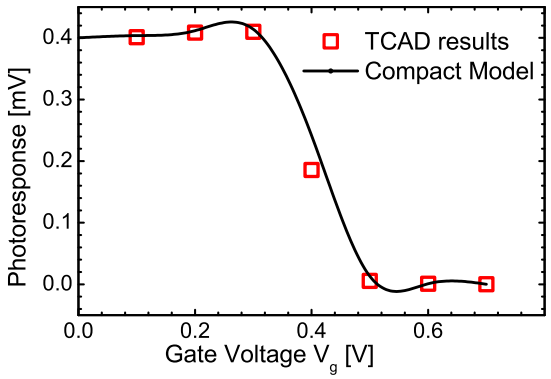


Fig. 3. Comparison of DC photoresponse obtained from TCAD and circuit simulations for different gate bias for an RF signal of 2 GHz. A PSP based RF compact model is used for circuit simulations.

The NMOS transistor from IHP's $0.13\mu m$ BiCMOS technology [6] is used for the present investigation. Doping profiles are derived from the process simulation. Simulated versus measured DC transfer characteristics are shown in figure 1(b). The calculated threshold voltage (constant current method) is 0.346 V.

Detailed quasi-continuous time domain simulations are performed to analyze THz mixing in the MOSFET channel. Figure 2(a) plots the time evolution of the drain voltage for a 0.2 THz excitation at a gate bias of 0.4 V. A distinct response settling time can be noticed. Note that the drain output is composed of harmonics as well as a DC offset because of frequency mixing. For this, the settled response is analyzed using Fourier transform. Figure 2(b) shows the drain output in frequency domain. An obvious fundamental tone of 0.2 THz can be observed along with a noticeable DC component.

To validate our simulation methodology, TCAD results are compared to those obtained from circuit simulation with a PSP based RF compact model. The comparison is performed at 2 GHz because of two reasons: (a) accurate compact models are not yet available for very high frequencies, and (b) A large channel resistance of MOSFET in subthreshold exponentially increases the response settling time and much longer device simulations are required for higher frequencies. Figure 3 shows the TCAD and circuit simulation results at 2 GHz. As shown, they are in close agreement and this verifies our scheme.

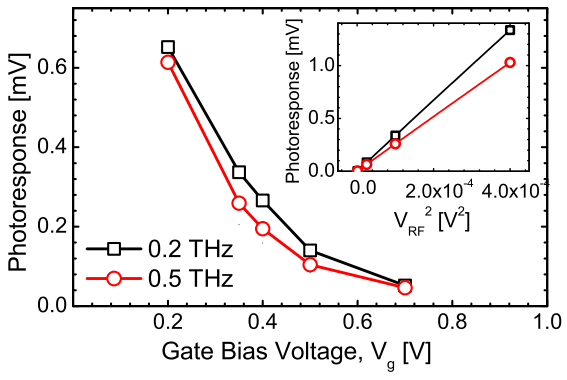


Fig. 4. Photoresponse for 0.2 THz and 0.5 THz excitation with gate bias. V_{RF} is 10 mV for both. (Inset) Square-law dependence of response on RF signal amplitude at V_g= 0.35 V.

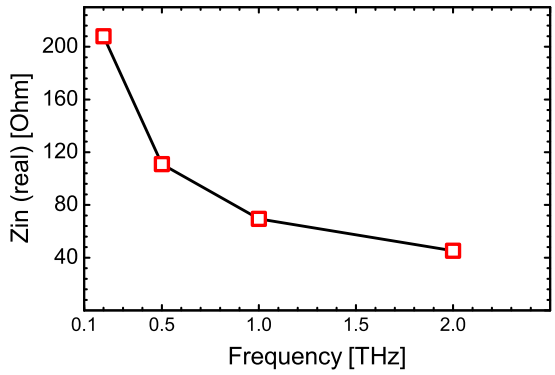


Fig. 6. Reduction in real input impedance of NMOS with frequency due to increase in injection current. V_g is 0.4 V. Impedance values are calculated using small signal AC simulations in TCAD.

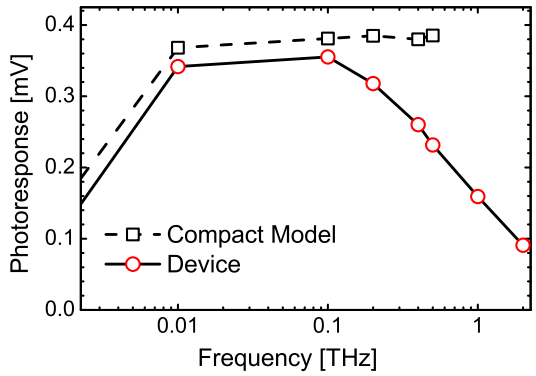


Fig. 5. Response roll-off with frequency at V_g= 0.4 V. At low frequencies (<10 GHz) the photo-response increases due to increased capacitive coupling of the RF signal to the drain. The dashed curve is from circuit simulation and is invalid after 0.1 THz because of uncalibrated compact model.

IV. Results and Analysis

Figure 4 shows the photoresponse obtained for 0.2 THz and 0.5 THz excitations plotted as a function of gate bias. As observed, the response reduces with increase in V_g for the linear region. It is maximum in the subthreshold region. The inset figure also confirms the linear relation between DC output and normalized input radiation power (V_{RF}^2).

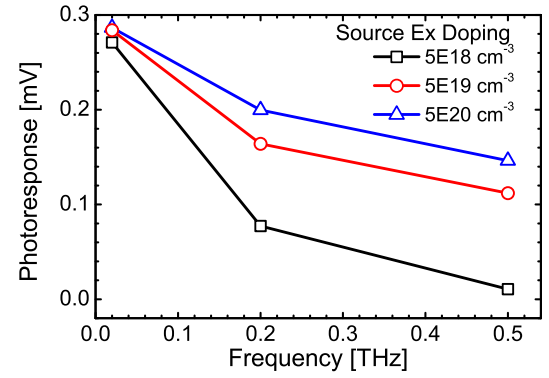
A close examination of figure 4 yields an interesting observation. The DC response reduces with increase in frequency from 0.2 THz to 0.5 THz. Figure 5 further explores this frequency roll-off. Here the photoresponse is plotted as a function of frequency for a 0.4 V gate bias. A significant response reduction can be seen which is not predicted by previous theory developed for FET THz detectors [3], [5]. Figure 5 also plots the data from circuit simulation (using *Agilent ADS*). As expected, circuit simulation data follows TCAD results till 100 GHz but becomes inaccurate after this frequency because of uncalibrated compact model.

A reason behind this observed roll-off of photoresponse can be the source-side parasitic resistance as indicated in [7]. This can be further explained as follows. THz radiation causes electron density oscillations inside the FET channel. With increase in frequency, the charges in the channel flow more rapidly and the rate of this charge flow- *Injection current*- becomes larger. Therefore the effective input impedance Z_{in} of the device reduces with frequency. Figure 6 plots the real part of Z_{in} versus frequency calculated using small signal AC analysis in TCAD which holds our argument. The potential drop over the parasitic resistance due to this injection current thus increases at higher frequencies. The useful signal available at the channel therefore reduces and results in a response roll-off.

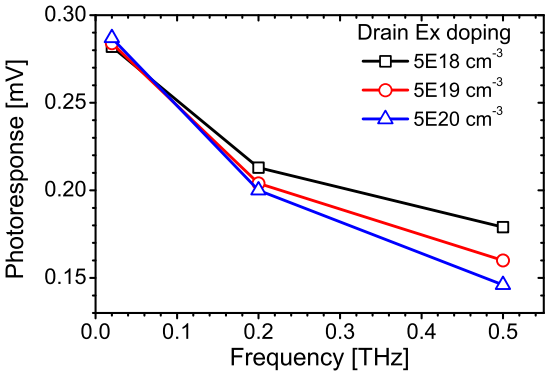
This theory can be further verified by altering the source and drain doping profiles and examining their effect on DC drain output. Since the channel is in immediate contact with source and drain extensions, we change the extension peak doping levels while keeping the same extension depth. Figure 7(a) shows the result of source side extension doping on photoresponse characteristics. The drain doping is the same in all three cases. As expected, the response is increased and the roll-off is reduced with higher extension doping because of lower source resistance. A 10x improvement is obtained at 0.5 THz with a two order increase in doping value. Note that the source resistance also controls the frequency roll-off slope. A lower source resistance is also desired to reduce the thermal noise.

Drain extension doping variation presents a different picture. Figure 7(b) shows the results. While the change in response is not as appreciable as in the case of source doping, the DC photoresponse reduces with increase in drain side doping or reduction in drain parasitic resistance. This observation can be ascribed to improvement in the device asymmetry. Radiation coupling to the drain end reduces for a higher drain resistance which improves the response.

Since the drain is not grounded, charge injection from the drain side is also affected by the drain-to-body capacitance C_{db}. This capacitance must be reduced to reduce the radiation coupling at drain end. We investigate this by varying the p-well doping profile. Reduced deep p-well doping for reduced C_{db} resulted in an improved photoresponse (Fig. 8(a)). Changing the top p-well doping results in change of channel-to-body

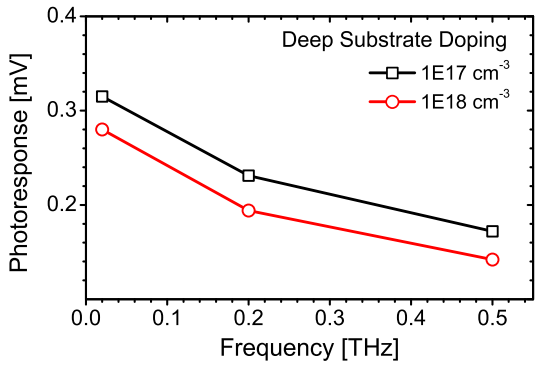


(a)

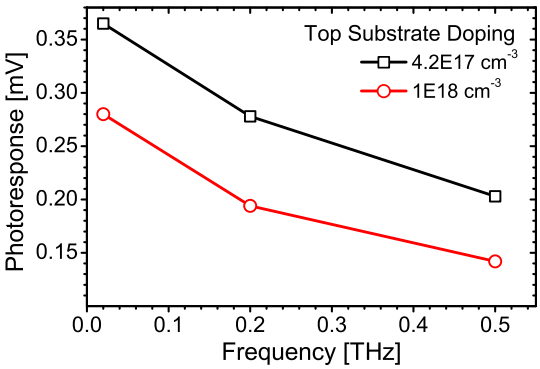


(b)

Fig. 7. Effect of source and drain extension doping on frequency response roll-off. (a) Only source extension peak doping is varied while drain doping is fixed (b) Only drain extension peak doping is varied with fixed source side doping. All results are obtained for a DC bias of V_g = 0.4 V.



(a)



(b)

Fig. 8. Effect of p-well profile on response roll-off at V_g= 0.4 V. (a) Deeper p-well concentration is changed, to change drain-to-body junction capacitance (b) Top p-well doping is changed to change channel-to-body capacitance. Gate voltage was adjusted to maintain the same overdrive.

capacitance $C_{ch,b}$ which contributes to signal loss to the substrate body. A reduction in top doping level is thus helpful in reducing $C_{ch,b}$ to improve the response. Fig. 8(b) shows the simulation results for various top p-well doping values. The gate voltage is adjusted to maintain the same overdrive when the the top substrate doping is altered.

V. Conclusion

In summary, we have analyzed the effects of device parasitics on the operation of CMOS FET THz detectors. Time-domain TCAD simulations have been used. It is found that the photoresponse for THz detection can be improved by: (1) minimizing the source-side resistance, (2) increasing the drain-side resistance, and (3) reducing the drain-to-body and channel-to-body capacitances. Based on these results, we propose an asymmetric transistor layout for optimized THz detection in the considered $0.13\mu m$ technology. It consists of (a) heavily-doped source extensions using the extensions of the 1.2V logic devices, (b) lightly-doped drain extensions using the extensions of the 3.3V I/O devices, and (c) a restriction of the p-well implantation to the source side of the FET.

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