Optimization of Program and Erase Characteristics of Two Bit Flash Memory P-Channel Cell Structure using TCAD

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***Abstract*—**This paper presents the optimization of the two bit flash memory P-channel cell structure using efficient 2D write and erase model. Our proposed cell structure stores charge at either Source and/or Drain sides of the gate in an SiN film and is based on method of programming by DAHE and erasing by FN tunneling. It is found that expansion of cell window and the improvement of erase characteristic depend on the optimization of the gate-film overlap under gate of the SiN film.

Keywords—Flash Memory; SONOS; Two-Bit; P-Channel; TCAD; (key words)

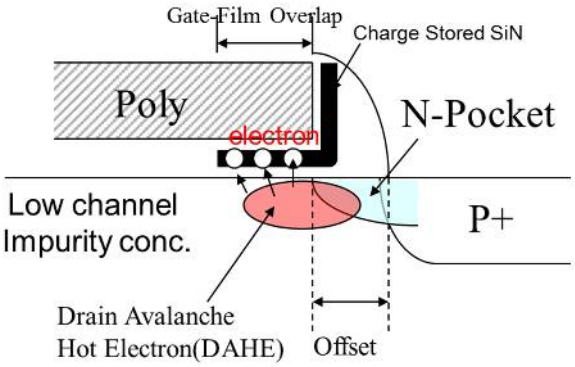
I. Introduction

For most nonvolatile memory SONOS (Semiconductor-Oxide-Nitride-Oxide-Semiconductor), a programming method by Channel Hot carrier Electron (CHE) using the N-channel cell structure with high-speed operation has been mainstream [1]. However, with the miniaturization of the cell, the short channel effect becomes stronger, and to maintain the programming voltage by the CHE method becomes difficult. Therefore, memory cell structure with the P-channel (Pcell) has been proposed [2]. In this paper, optimization of two bit flash memory P-channel cell which is based on the method of programming by Drain Avalanche Hot Carrier (DAHC) and erasing by Fowler-Nordheim (FN) tunneling using TCAD is reported.

II. Cell Structure and Program/Erase Mechanism

Figure 1 shows cell structure under study. Our proposed cell structure has the charge stored in the SiN film on both sides of the SD region. DAHC which can inject electron on SiN film efficiently in low Vg to reduce the increase of the cell current is adopted as programming method. In addition, low channel impurity concentration is used for mobility improvement, and the pocket profile and offset length are constructed for the control of the short channel effect. By the optimization of the program and erase characteristics, gate-film overlap of SiN film under gate is adjusted.

Figure 2 shows an illustration of cell window. In a Pcell, when electrons are injected into the SiN film, current conduction is enhanced (ON state). When electrons are removed from the SiN film, majority carrier current conduction



Fig,1 Cell structure in right half side under study. Electron is injected into SiN film by DAHE, and is removed from SiN film by FN tunneling.

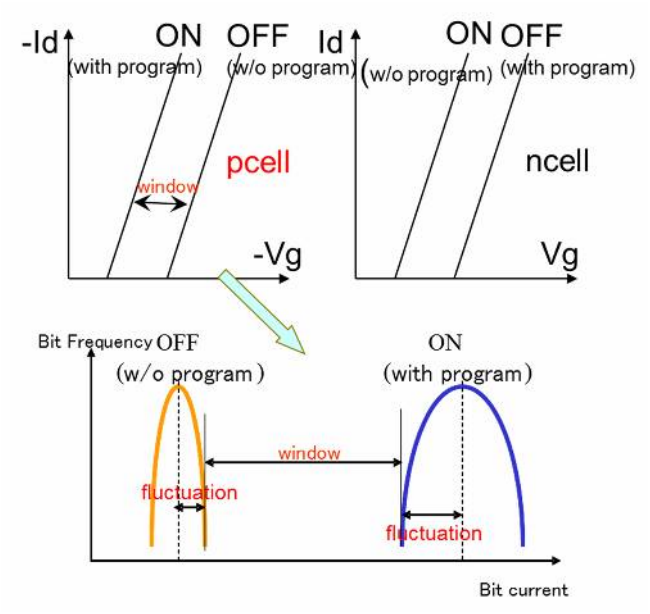


Fig.2 Conceptual diagram of cell window. The window is the current difference between "ON" and "OFF" state. The actual window becomes small by considering of fluctuation.

(holes) is inhibited (OFF state). This relationship is the reverse for the Ncell. The current difference between "ON" and "OFF" state is the operating window, the actual window size is decreased by fluctuations.

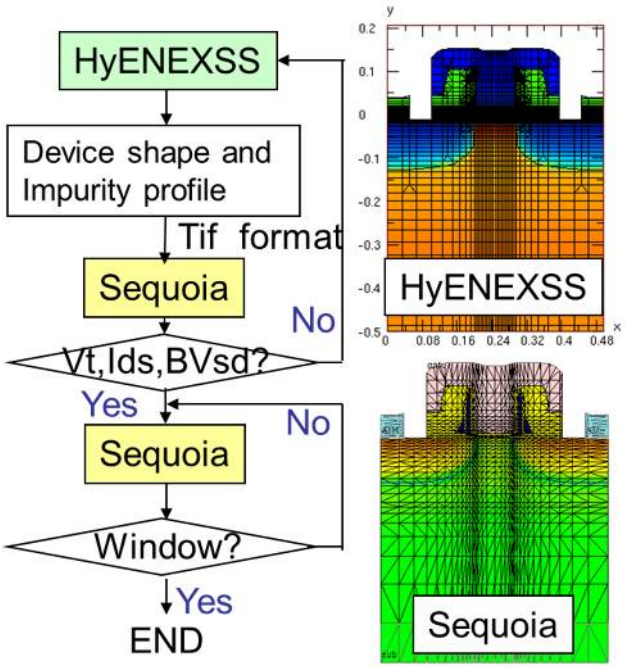


Fig.3 Calibration method of cell window estimation. Some model parameters and channel width are adjusted.

III. Simulation Strategy

Figure 3 shows the flow of the cell window calculation. We use HyENEXSS [3] for a device shape and impurities profile extractions, and Sequoia tool [4] for window calculation including program and erase characteristics, respectively. To ensure simulation accuracy, diffusion and segregation coefficients for impurity are adjusted as Vt, Ids and BVsd fit to experiment data. TIF format is used for the interface of two tools. The cell window is calibrated by considering some model parameters and an effective channel width. The main model parameters relate to magnitude and extension of electron injection amount into SiN film with hot carrier injection model [5] for program characteristics, and coefficients of pre-exponential and exponential term in Fowler-Nordheim tunneling model [6] for erase characteristics.

IV. Optimization of Program and Erase Characteristics using TCAD

The film thicknesses and dimensions of the cell structure which used for the calibration of the model parameter are listed in Table I. Figure 4 shows a comparison between experimental data and simulation of basic characteristics. In spite of 2D analysis, simulation reproduces experiment data well. It may mean that the 3D effect is small in the p-channel cell with channel impurity of arsenic.

Table I. Film thicknesses and dimensions of cell structure

Dimensions	Value
Gate Length	94nm
Gate Width	90nm
Gate Oxidation	80Å
Gate–Film Overlap	200Å
Bottom Oxidation	65Å

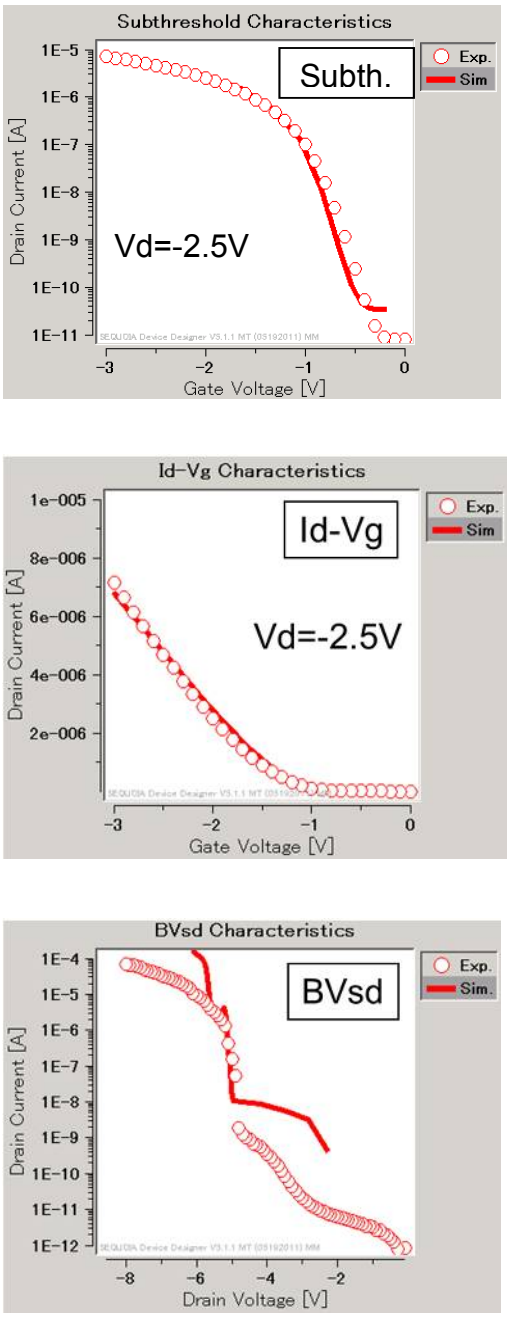
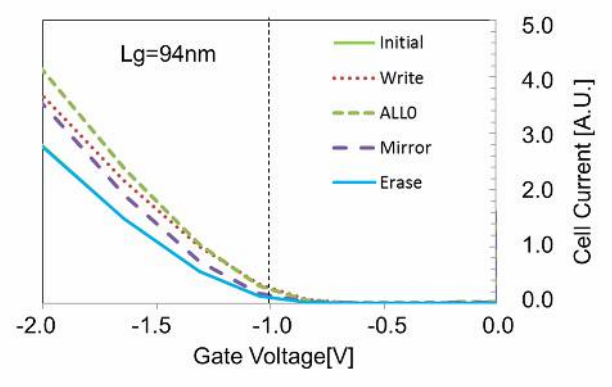
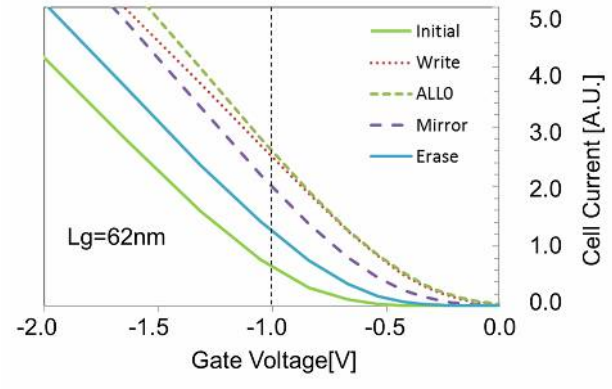


Fig.4 Comparison between experimental data and simulation of subthreshold, Id-Vg, and BVsd characteristics before window calculation.



(a)



(b)

Fig.5 Simulated cell current in terms of gate voltage in each process step of (a)Lg=94nm and (b)Lg=62nm. Bias condition is Vd= -2.5V and Vb=Vs=0V. The dashed line of Vg=-1V is read condition. “Erase” in Lg=94nm almost overlaps with “Initial”.

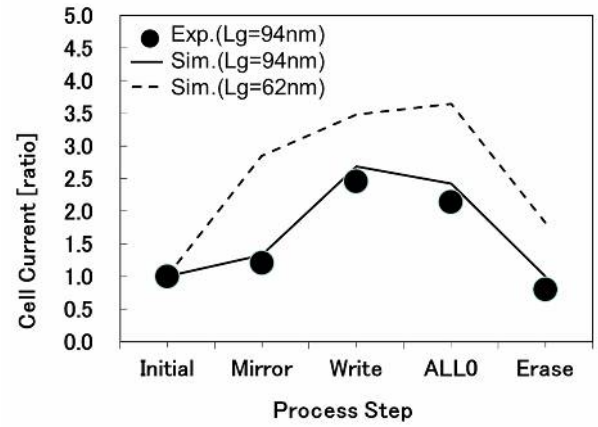
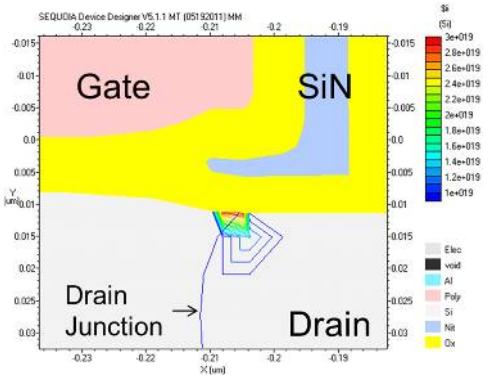


Fig.6 Ratio of initial current for current at read condition in each process step. Read condition is given by Vg= -1.0V, Vd=-2.5V, and Vb=Vs=0V.

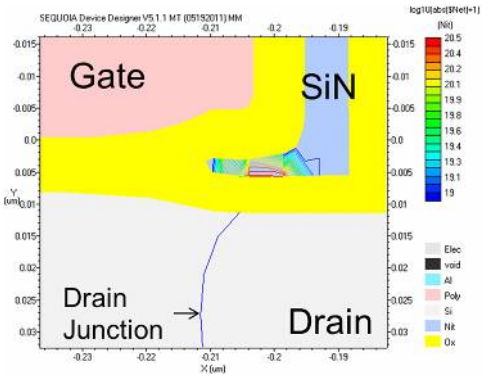
Figure 5 and 6 show the simulated cell current with gate voltage dependence and the ratio of initial current for current at read condition in each process step. "Mirror", "Write" and "ALL0" represent programming in drain side, source side and both, respectively. In each process, simulation reproduces tendency of experiment data well. The increase in effective cell window as difference between "Mirror" and "Write" is a key to improve the performance of the cell.

Figure 7 shows distributions of impact ionization and electron injection to SiN film in program process. It is effective to increase gate-film overlap so that "Mirror" does not increase to minimize the distance between a peak position of the impact ionization and the SiN film for improvement of the programming efficiency.

Figure 8 shows electric field distribution of Lg=94nm and Lg=62nm in erase process. The electric field used for the erase process by FN tunneling weakens for shorter gate lengths because the effective gate oxide thickens. Optimization of the gate-film overlap to improve "Erase" and "Mirror" is necessary for the miniaturization of the cell. In addition, the optimization of the cell structure using our approach can largely reduce calculation cost in comparison with a full 3D analysis and is effective for the actual development that QTAT is required.

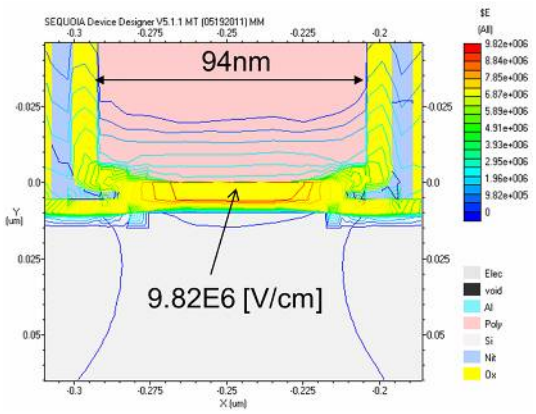


(a)

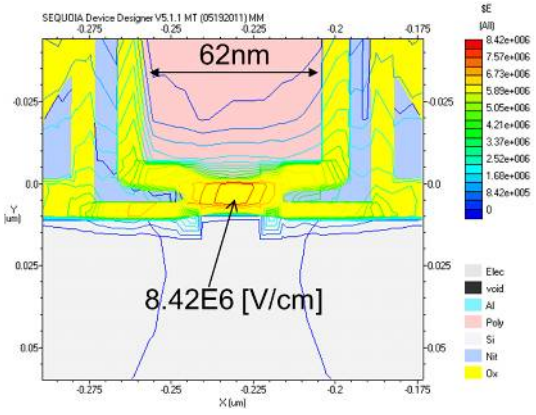


(b)

Fig.7 Distributions of (a) impact ionization and (b) electron injection to SiN film in program process. Program condition is based on Vg=-1.0V, Vd=-6.0V and Vb=Vs=0V for Lg=94nm.



(a)



(b)

Fig.8 Electric field distribution of (a) Lg=94nm and (b) Lg=62nm in erase process. Erase condition for two different gate lengths is same as Vg=-6.0V and Vd=Vs=Vd=+6.0V.

V. Conclusions

Optimization of the cell structure using our approach can substantially reduce calculation cost and engineering effort in comparison with a full 3D analysis and is effective for development under QTAT requirements using an easy-to-use and cost-effective 2D model. Although our model is 2D, it reproduces actual program and erase characteristic well, and it is found that the optimization of the gate-film overlap in the SiN film is important. Our approach is effective for memory device design under QTAT constraints.

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