Extraction of Quasi-Ballistic Transport Parameters in Si Double-Gate MOSFETs Based on Monte Carlo Method

Ryoma Ishida[1], Shunsuke Koba[1], Hideaki Tsuchiya[1,2], Yoshinari Kamakura[2,3], Nobuya Mori[2,3], Shigeyasu Uno[2,4], and Matsuto Ogawa[1]

[1]Department of Electrical and Electronic Engineering, Graduate School of Engineering, Kobe University, Kobe, Japan
Email:137t204t@stu.kobe-u.ac.jp

[2]Japan Science and Technology Agency, CREST, Chiyoda, Japan

[3]Division of Electrical, Electronic and Information Engineering, Graduate School of Engineering, Osaka University, Suita, Japan

[4]Department of Electrical and Electronic Engineering, Ritsumeikan University, Kyoto, Japan

***Abstract*—In this study, we have developed an evaluation tool of quasi-ballistic transport parameters in realistic devices, to clarify practical benefits of downscaling MOSFETs into ultimate physical scaling limit. It is found that ballistic transport in double-gate (DG) MOSFETs is enhanced due to the channel length (L_{ch}) scaling until L_{ch} = 10 nm, but when L_{ch} is further scaled to less than 10 nm using $T_{Si} = L_{ch} / 3$ scaling rule, where T_{Si} is the channel thickness, surface roughness scattering intensified by spatial fluctuation of quantized subbands drastically degrades ballistic transport. Furthermore, on-current increase or decrease of ultra-scaled DG MOSFETs is found to be basically determined by a backscattering coefficient R. Gate and drain bias voltage dependencies of ballisticity are also evaluated.**

Keywords—quasi-ballistic transport; backscattering coefficient; Monte Carlo simulation; scaling; surface roughness scattering

I. Introduction

Ballistic transport has been expected to boost device performance of MOSFETs. In particular, silicon-on-insulator (SOI) or double-gate (DG) MOSFETs with an intrinsic channel are considered to have an advantage to achieve ballistic transport, because impurity scattering is absent in those channel region [1]. However, such ultrathin channel devices suffer from a non-traditional surface roughness (SR) scattering caused by spatial fluctuation of quantized subbands [2]. Therefore, clarification of practical benefits of downscaling MOSFETs into ultimate physical scaling limit is highly required.

In the meantime, concepts such as mobility and saturation velocity, which have formed the basic foundation for developing conventional drift-diffusion transport models, are considered not to be applied anymore in the quasi-ballistic transport regime. Hence, a new transport model describing carrier's quasi-ballistic transport at the atomic level is needed. According to [3], drain current in the quasi-ballistic transport regime is expressed using an injection velocity v_{inj} and a backscattering coefficient R. Thus, it is indispensable to develop an evaluation tool of those quasi-ballistic transport parameters in realistic devices, in order to clarify practical benefits of further downscaling Si MOSFETs. In this study, we have developed such evaluation tool based on Monte Carlo (MC) simulation techniques, and have provided knowledge regarding the role of the non-traditional SR scattering on the quasi-ballistic transport in Si-DG MOSFETs [4]. We have also discussed gate and drain bias voltage dependencies of R, in order to demonstrate that the channel length dependency of R is not altered by the bias conditions.

II. Simulation Methods

A. Multi-subband MC approach

We have employed the self-consistent multi-subband MC approach, in which Schrödinger-Poisson solver and MC simulator are self-consistently solved. Scattering processes considered in this study are acoustic phonon, optical phonon, ionized impurity and SR scatterings. Here, it should be emphasized that the non-traditional SR scattering caused by spatial fluctuation of quantized subbands, which is owing to channel thickness variation in ultrathin channel devices, is also considered by using so-called Prange-Nee terms [5]. Nonparabolicity of the conduction band is taken into account in all scattering rates. In addition, the number of subbands considered in the simulation was chosen to be large enough, i.e., subbands with quantized energy less than 0.5 eV were considered, because V_D = 0.5 V was used in this study.

B. Quasi-Ballistic tarnsport parameters

A schematic diagram representing the quasi-ballistic transport picture is shown in Fig. 1. v_{inj} is defined as an average velocity for carriers passing through the bottleneck point from source to channel. When scattering occurs in the channel, an average carrier velocity at the bottleneck point, v_s, is expressed by [1]

$$v_s = v_{inj} \times \frac{1-R}{1+R(v_{inj} / v_{back})} \tag{1}$$

where v_{back} is a backward carrier velocity and R a backscattering coefficient defined as a flux ratio given by $R = Q_b v_{back} / Q_f v_{inj}$, where Q_f and Q_b are the forward and backward

978-1-4799-5288-5/14/$31.00 © 2014 IEEE

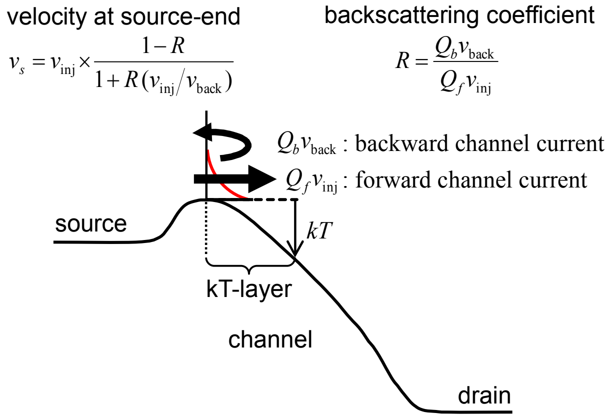

Fig. 1 Definitions of quasi-ballistic transport parameters in a MOSFET. Backscattering coefficient R is defined as a ratio of backward and forward channel currents.

channel charge densities, respectively. In the ballistic limit (R = 0), $v_s = v_{inj}$. By taking advantage of MC techniques, we have carefully monitored particle trajectories crossing over the bottleneck point from source to channel and vice versa, and then we could extract the average carrier velocities, v_{inj} and v_{back}, and R. In other words, we have succeeded in evaluating the quasi-ballistic transport parameters directly from the carrier dynamics in MOSFETs [4].

III. Simulation Results

A. Channel length dependencies of R and I_{on}

Fig. 2 shows the device structure of DG MOSFET used in this study. Note that the channel length L_{ch} was varied from 30 to 6 nm, whereas the channel thickness T_{Si} was chosen by following an empirical rule of $T_{Si} = L_{ch}/3$, which is often used as a guideline to suppress short-channel effects. In fact, we confirmed that threshold voltage (V_{th}) lowering due to L_{ch} scaling can be successfully suppressed by introducing this T_{Si} scaling as shown in Fig. 3, where the results obtained by using $T_{Si} = L_{ch}/2$ scaling and fixed T_{Si} (=3 nm) are also plotted for comparison. As clearly shown in this figure, the $T_{Si} = L_{ch}/3$ scaling almost completely suppresses the V_{th} lowering until L_{ch} = 6 nm.

Fig. 4 shows the simulated R as a function of the channel

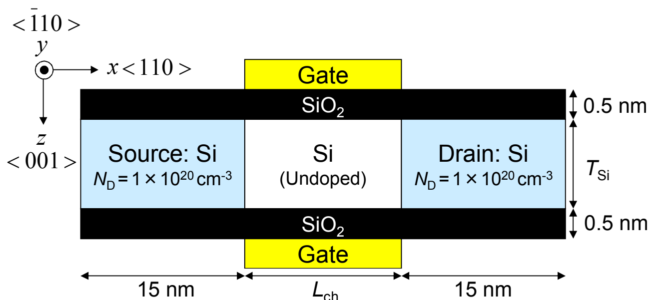

Fig. 2 Device structure of DG MOSFET. Note that the channel length L_{ch} was varied from 30 to 6 nm, whereas the channel thickness T_{Si} was chosen by following an empirical rule of $T_{Si} = L_{ch}/3$, which is often used as a guideline to suppress short-channel effects. The channel is undoped and thus carrier backscattering in the channel is caused by phonon and SR scatterings.

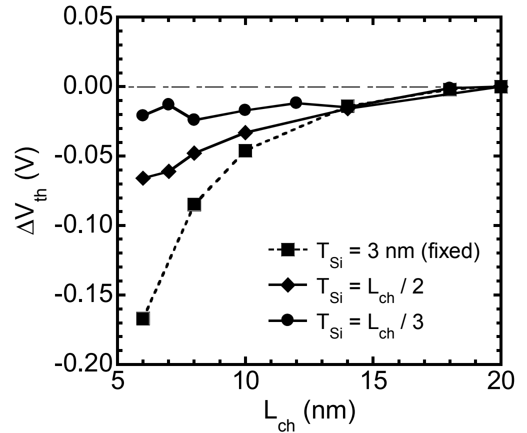

Fig. 3 Threshold voltage lowering ΔV_{th} computed as a function of the channel length, where the vertical axis represents variations in V_{th} measured from the values at L_{ch} = 20 nm, i.e., $\Delta V_{th} = V_{th}(L_{ch}) - V_{th}(20\,nm)$. The dashed line with squares represents the fixed T_{Si} (= 3 nm), the solid line with diamonds $T_{Si} = L_{ch}/2$, and the solid line with circles $T_{Si} = L_{ch}/3$. Note that the $T_{Si} = L_{ch}/3$ scaling almost completely suppresses the V_{th} lowering until L_{ch} = 6nm. Therefore, we adopted the $T_{Si} = L_{ch}/3$ scaling rule in this study.

length, where our previous results in [6] are also plotted. Note that the lower and upper horizontal axes represent L_{ch} and T_{Si}, respectively. R decreases with reducing L_{ch} until L_{ch} = 10 nm in both the present and previous results. This means that ballistic transport is enhanced due to the channel length scaling down to 10 nm. However, for L_{ch} < 10 nm, the present results exhibit the drastic increase in R, whereas the previous result exhibits the monotonous decrease in R. Since our previous result ignored SR scattering, the discrepancy in the sub-10 nm regime is due to the SR scattering [4]. Fig. 5 shows the channel length dependency of on-current, I_{ON}, simulated using the MC simulator. It is found that I_{ON} increases with reducing L_{ch} until L_{ch} = 10 nm, and then, it sharply decreases in the sub-10 nm regime. Namely, on-current increase or decrease of ultra-scaled DG MOSFETs is found to be basically determined by a quasi-ballistic transport parameter R, shown in Fig. 4. Accordingly, the on-current degradation in the sub-10 nm

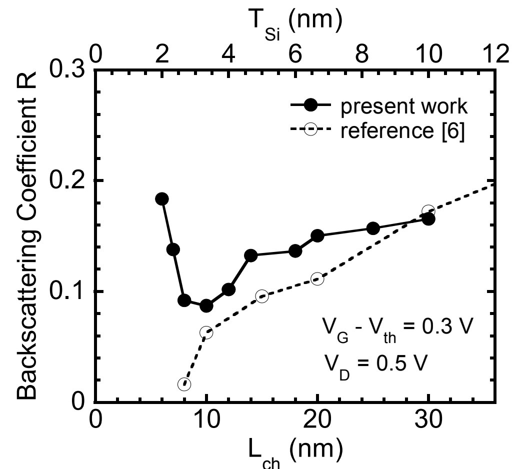

Fig. 4 Simulated R as a function of the channel length, where the lower and upper horizontal axes represent L_{ch} and T_{Si}, respectively. The dashed line represents our previous results in [6]. The discrepancy in the sub-10nm regime is due to the SR scattering.

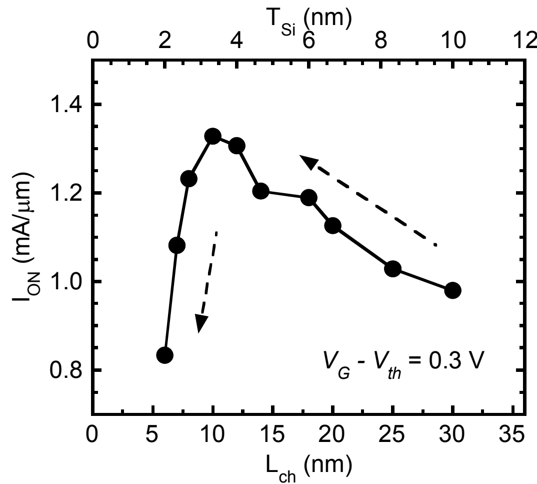

Fig. 5 Channel length dependency of I_{ON}. It was calculated at $V_G - V_{th}$ = 0.3V. V_{th} is defined as the gate voltage which corresponds to I_D = 0.01mA/μm. I_{ON} increases with reducing L_{ch} until L_{ch} = 10 nm, and then, it sharply decreases in the sub-10 nm regime. This tendency is coincident with that in an inverse of R shown in Fig. 4.

regime is confirmed due to the SR scattering intensified by spatial fluctuation of quantized subbands. Hence, significant improvement in the quality of gate oxide interfaces is indispensable to receive the benefits of ballistic transport in the sub-10 nm DG/SOI MOSFETs.

B. Gate and drain bias voltage dependencies of R

Since the scattering rates depend on electron kinetic energy, R may be functions of the gate and drain bias voltages. Then, to demonstrate that the channel length dependency of R found in Fig. 4 is unaltered by the bias conditions, we further examined the gate and drain bias voltage dependencies of R, using the MC simulator. Fig. 6 shows the gate voltage dependencies of R calculated for L_{ch} = 6, 10, and 20 nm. It is found that R increases with the gate voltage for all the channel lengths. To explain the reason, we plotted the variations due to the gate voltage in the lowest subband energy profile and in the average electron kinetic energy profile in Fig. 7 (a) and (b), respectively, for L_{ch}

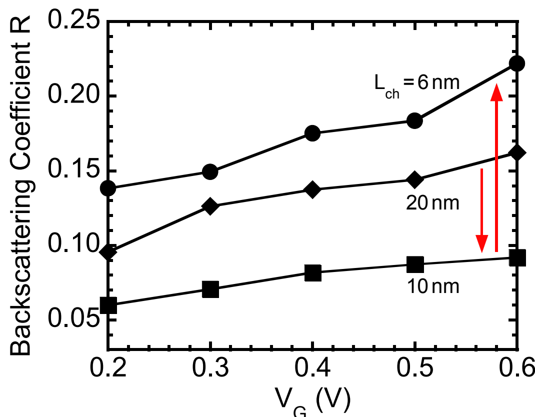

Fig. 6 Gate voltage dependencies of R calculated for L_{ch} = 6, 10, and 20nm. V_D = 0.5 V. R increases with the gate voltage for all the channel lengths.

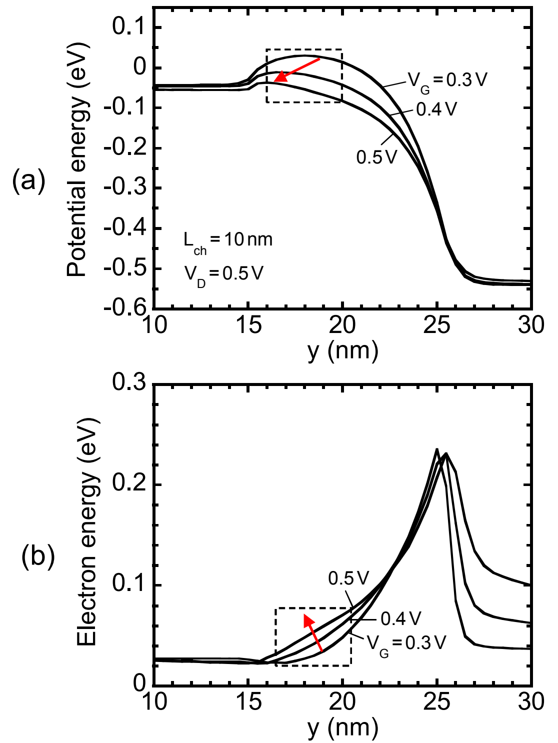

Fig. 7 Variations due to gate voltage in (a) the lowest subband energy profile and in (b) the average electron kinetic energy profile, where L_{ch} = 10nm and V_D = 0.5 V. Note that the electron kinetic energy increases in the left side of the channel as the channel potential is decreased by the gate voltage increase, which leads to the increased R with the gate voltage.

= 10 nm and V_D = 0.5 V. Note that the electron kinetic energy increases in the left side of the channel as the channel potential is decreased by the gate voltage increase. As a result of the increased kinetic energy, phonon scattering increases at the source-end of the channel with the gate voltage. SR scattering also increases with the gate voltage. Both of them lead to the increased R with the gate voltage as shown in Fig. 6. However, for L_{ch} = 6 nm, SR scattering becomes dominant over acoustic phonon scattering [4], and then R more swiftly increases with the gate voltage in the case of L_{ch} = 6 nm. According to the above results, the channel length dependency of R in Fig. 4 is found to be unaltered by the gate bias condition in the present DG MOSFETs.

Next, Fig. 8 shows (a) I_D – V_D characteristics and (b) the drain voltage dependencies of R, calculated for L_{ch} = 10 nm and V_G = 0.2, 0.4 and 0.6 V. At V_D = 0 V, R = 1 was obtained for all gate voltages, which verifies the validity of our extraction method of R. Here, note that R is almost constant with the drain voltage in the saturation region, which of course corresponds to the saturation of the drain current. This can also be understood using the variations in the lowest subband energy profile and in the average electron kinetic energy profile as shown in Fig. 9 (a) and (b), respectively. First, the electron kinetic energy slightly increases in the left side of the channel with the drain voltage, as shown in Fig. 9 (b). Next, the width of the potential bottleneck barrier, i.e. kT-layer length [1], reduces with the drain voltage as shown in Fig. 9 (a). This is because as the drain voltage increases, the potential energy around the drain-side of

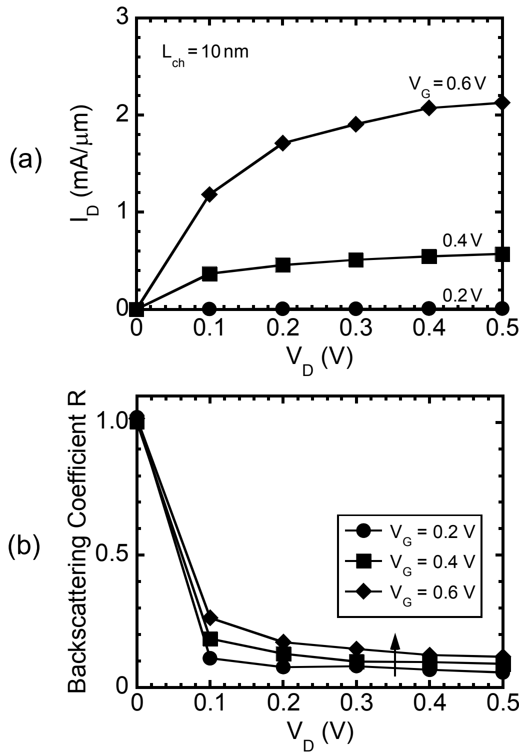

Fig. 8 (a) $I_D - V_D$ characteristics and (b) drain voltage dependencies of R, calculated for L_{ch} = 10 nm and V_G = 0.2, 0.4 and 0.6 V. At V_D = 0 V, R = 1 was obtained for all gate voltages. Here, note that R is almost constant with the drain voltage in the saturation region, which of course corresponds to the saturation of the drain current.

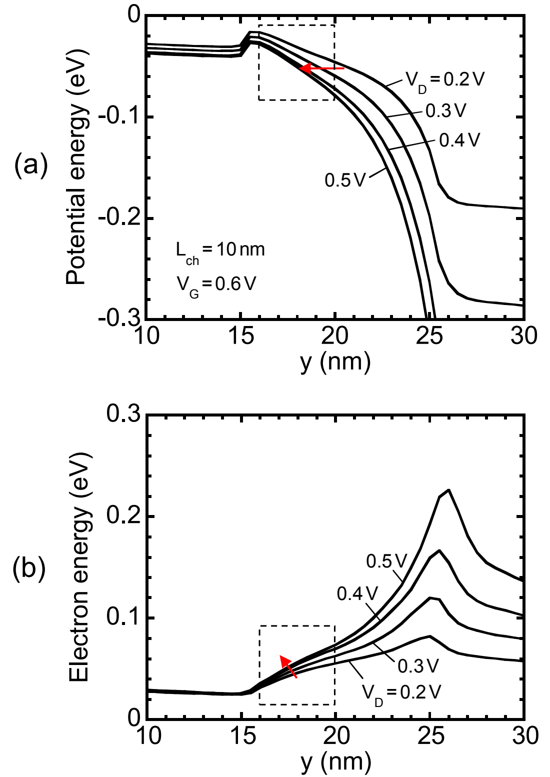

Fig. 9 Variations due to drain voltage in (a) the lowest subband energy profile and in (b) the average electron kinetic energy profile, where L_{ch} = 10nm and V_G = 0.6 V. The electron kinetic energy slightly increases in the left side of the channel with the drain voltage as seen in (b). On the other hand, the width of the potential bottleneck barrier, i.e. kT-layer length, reduces with the drain voltage as seen in (a). The reduction of the kT-layer length offsets the increase in phonon scattering due to the increased electron kinetic energy.

the channel is significantly lowered, and it distinctly reduces the kT-layer length. Since the reduction of the kT-layer length offsets the increase in phonon scattering due to the increased electron kinetic energy, R eventually becomes almost constant with respect to the drain voltage. Consequently, the drain bias condition is also found not to alter the channel length dependency of R in Fig. 4.

IV. Conclusion

In this study, we have developed an evaluation tool of the quasi-ballistic transport parameters based on MC techniques, and have presented the backscattering coefficients evaluated as a function of the channel length, the gate and the drain bias voltages. As a result, it is found that ballistic transport in DG MOSFETs is enhanced due to L_{ch} scaling until L_{ch} = 10 nm, but when L_{ch} is further scaled to less than 10 nm using the $T_{Si} = L_{ch}$ / 3 scaling rule, SR scattering intensified by spatial fluctuation of quantized subbands drastically degrades ballistic transport. On-current behavior of ultra-scaled DG MOSFETs has been confirmed to be basically determined by R, and thus the quality of gate oxide interfaces must be improved to avoid the drastic increase of R due to SR scattering, and to improve the device performance in the sub-10 nm regime. It is also found that R increases with the gate voltage, whereas it is almost constant with the drain voltage in the saturation region. Therefore, the channel length dependency of R was confirmed to be unaltered by the gate and drain bias conditions in the on-state. The knowledge obtained in the present simulation would be useful to develop a compact model for quasi-ballistic MOSFETs.

References

[1] K. Natori, "Scalling limit of the MOS transistor -A ballistic MOSFET-,'' IEICE Trans. Electron., vol. E84-C, no. 8, pp. 1029-1036, August 2001.

[2] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5 nm,'' Technical Digest of International Electron Devices Meeting (IEDM), pp. 47-50, December 2002.

[3] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," IEEE Electron Device Lett., vol. 18, no. 7, pp. 361–363, July 1997.

[4] S. Koba, R. Ishida, Y. Kubota, H. Tsuchiya, Y. Kamakura, N. Mori, and M. Ogawa, "The impact of increased deformation potential at MOS interface on quasi-ballistic transport in ultrathin channel MOSFETs scaled down to sub-10nm channel length," Technical Digest of International Electron Devices Meeting (IEDM), pp. 312-315 December 2013.

[5] R. E. Prange and T.-W. Nee, "Quantum spectroscopy of the low-field oscillations in the surface impedance," Phys. Rev., vol. 168, no. 3, pp. 779–786, April 1968.

[6] H. Tsuchiya, K. Fujii, T. Mori, and T. Miyoshi, "A quantum-corrected Monte Carlo study on quasi-ballistic transport in nanoscale MOSFETs," IEEE Trans. Electron Devices, vol. 53, no. 12, pp. 2965–2971, December 2006.