Investigation of Retention Behavior for 3D Charge Trapping NAND Flash Memory by 2D Self-Consistent Simulation

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***Abstract*—This paper presents a comprehensive investigation on retention behavior for three-dimensional charge trapping NAND flash memory by two-dimensional self-consistent simulation. Major physical mechanisms, including tunneling, charge trapping and de-trapping process as well as drift-diffusion have been incorporated into the simulator. The developed simulator is able to describe the charge transport along the bitline and in vertical direction in the memory structure. This work aims to help to design and optimize three-dimensional stackable CT-NAND architectures.**

Keywords—retention; charge trapping; NAND flash; two-dimensional simulation

I. INTRODUCTION

3D stackable Charge-Trapping (CT) NAND flash is forecasted to continue the scaling of NAND flash below 15nm node. [1] Various types of 3D stacked NAND architecture have been proposed and implemented to provide excellent scaling ability [2-5]. With scaling down of the 3D NAND flash memory, the bit line (BL) is continuously reduced, thus the spreading of charge along BL and the correlation between memory cells under different operations are no longer negligible. Hence, accurate 2D simulation of the charge behavior along the BL and in the gate stack is significant to design and optimize the 3D stackable CT-NAND flash. However, previous research of CT memory mainly focuses on the gate stack one-dimensionally in one memory cell [6, 7] and lacks the detailed descriptions of charge transport and trapping mechanism in the storage layer [8]. In this work, a 2D self-consistent simulator of CT-NAND is developed with the incorporation of physical models including tunneling, charge trapping and de-trapping process as well as drift and diffusion mechanism to explore the charge transport mechanism both along BL and in vertical directions in the storage layer. The retention behavior of 3D NAND flash is simulated and the charge loss mechanism is analyzed. The results can help to design and optimize 3D NAND memory.

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II. PHYSICAL MODEL AND SIMULATION METHOD

A. Physical Model

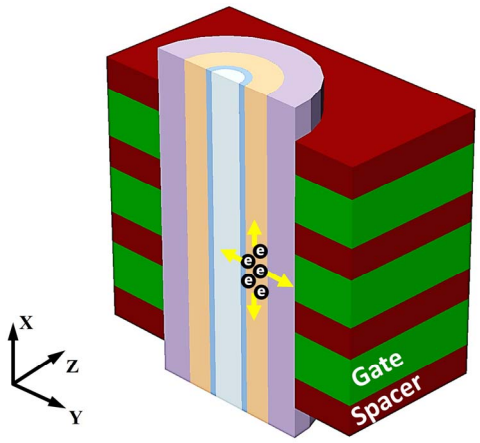
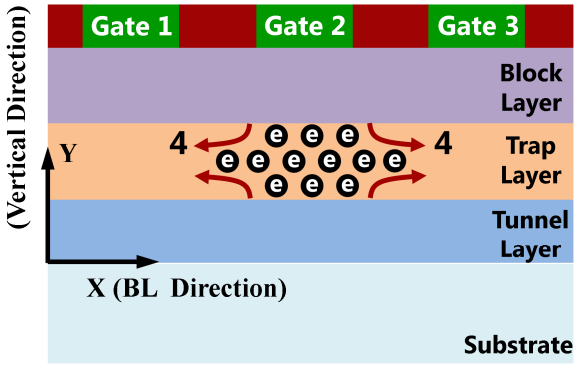
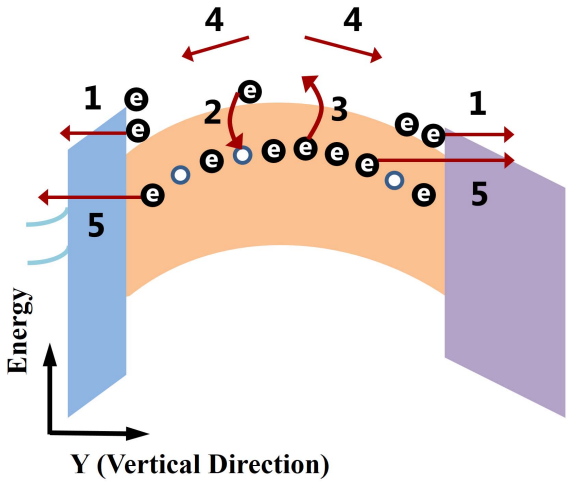


Fig. 1. Simulated 3D CT-NAND structure, charge loss along BL and vertical direction is also shown.

Fig. 1 demonstrates the simulated regions of 3D NAND flash structure. In order to consider charge transport along both BL and in vertical direction in the trapping layer and the interference of the neighboring cells and without lack of generality, the simulation region consists of three cells. The involved physical mechanisms accounting for charge evolution along BL and vertical direction in the 3D-type memory cell are illustrated in Fig. 2(a) and Fig. 2(b) respectively. A set of 2D non-linear partial differential equations is solved self-consistently in the simulator, comprising Poisson equation, carrier continuity equation and trapped charge conservation equation. [9] Charge transport in the conduction band of the charge trapping layer is described based on the drift-diffusion transport scheme.



(a)



(b)

Fig. 2. Dominant physical mechanisms along (a) BL and (b) in vertical direction: 1-DT/FN Tunneling, 2&3-carrier capture and emission, 4-drift and diffusion transport, 5-TB Tunneling.

B. Simulation Method

The interaction between free carriers and trapped carriers is governed by carrier capture phenomenon calculated by Shockley-Read-Hall (SRH) theory and carrier emission contributed by thermal and Poole-Frenkel effect. Besides, Band-to-Trap (BT) tunneling and Trap-to-Band emission is taken into account as the additional charge capture and loss mechanisms. Tunneling current across oxide and the above-mentioned BT and TB rate are computed using Wentzel-Kramers-Brillouin approximation.

Fig. 3 shows the reproduction of experimental data extracted from [10], referring to a 4/8.7/11.5 nm TANOS device. The parameters used are listed in Table I.

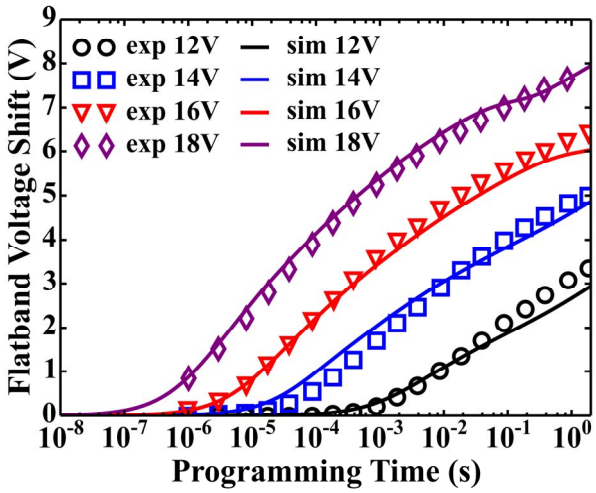


Fig. 3. Calibration of the simulator using device with $SiO_2/Si_3N_4/Al_2O_3$ (4/8.7/11.5 nm) gate stack.

TABLE I. MAIN PARAMETERS USED IN THE SIMULATION

Parameter	Value
Si_3N_4 trap cross-section	2×10^{-14} cm^{-2}
Si_3N_4 trap energy	1.7 eV
Si_3N_4 electron mobility	0.01 $cm^2/V/s$
Si_3N_4 TBT frequency	1×10^6Hz [7]
Si_3N_4 PF frequency	2×10^{11}Hz [7]

III. RESULTS AND DISCUSSION

Fig. 4 demonstrates the potential distribution of the gate stack and trapped electron distribution in the trapping layer of the structure for calibration in the final programming state. To manifest the charge spreading along BL, the simulation of a TANOS device with gate stack of 6/8/12 nm (thick tunneling oxide) is performed.

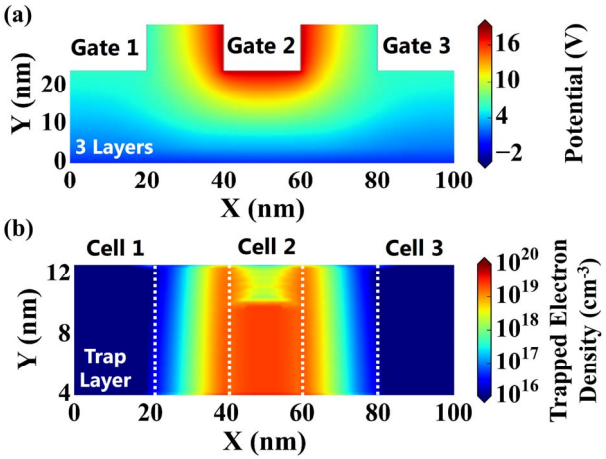


Fig. 4. (a) Potential of the structure (b) trapped electron distribution in the trapping layer for the structure used for calibration.

Fig. 5 shows the trapped and conduction band (CB) electron density of this structure during retention at 10^6s under 350K. It can be concluded that the electrons are transported to the tunneling oxide interface and blocking oxide interface on both sides of cell 2. This results from the spreading of electrons along BL and the flatter tunneling-out barrier under isolation regions compared with that under gate region. Fig. 6(a) plots the band diagram of three cuts indicated in Fig. 5. In addition, Fig. 6(b) and (c) reveals the corresponding trapped electrons and CB electrons profile.

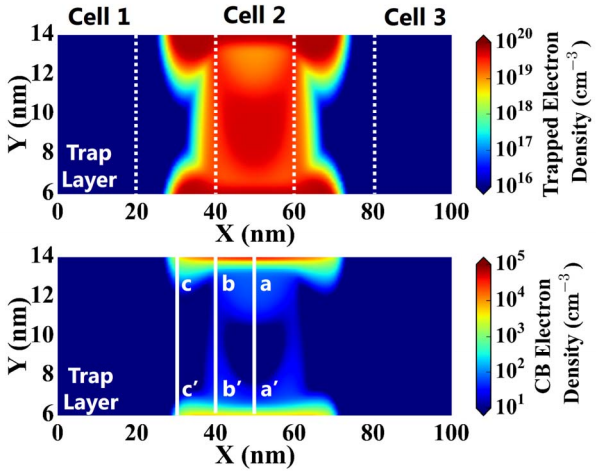


Fig. 5. Trapped electron density and CB electron density of a 6/8/12 nm TANOS device at 10^6s under 350K.

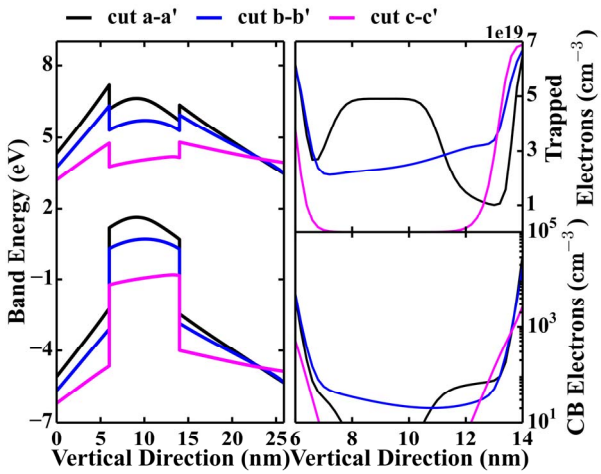


Fig. 6. Band diagram (a), trapped electrons density (b) and CB electron density(c) along three cuts along vertical direction indicated in Fig. 5.

Fig 7 plots the time-dependent evolution of trapped electrons along BL at tunneling oxide interface, through the middle of the trapping layer and at blocking oxide interface. Fig 8(a) and (b) illustrates the time-dependent evolution of trapped and CB electron density in vertical direction at the middle of trapping layer.

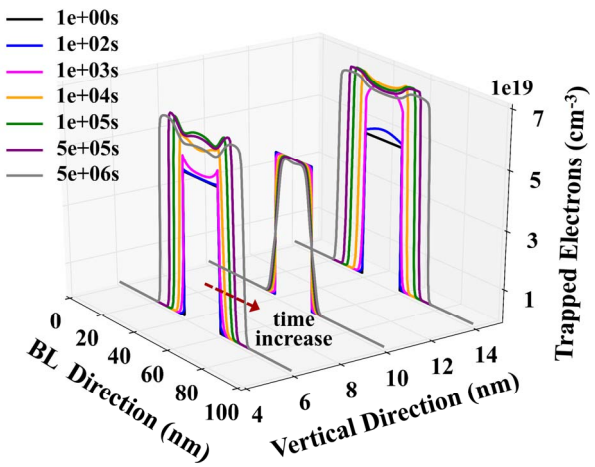


Fig. 7. Trapped charge distribution at different retention time along BL direction near tunnel oxide interface, in the middle of trapping layer and near block oxide interface.

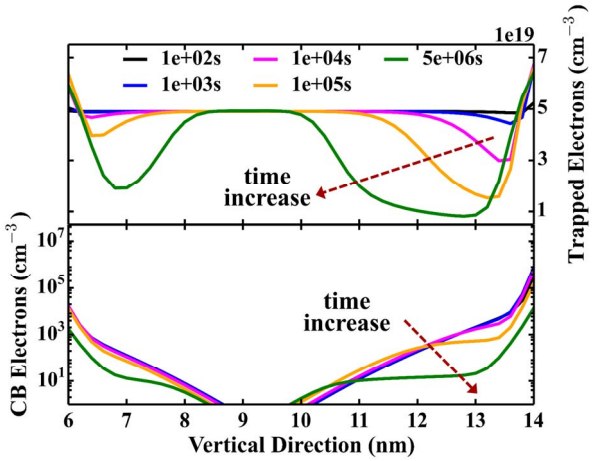


Fig. 8. Time evolution of (a) trapped electron and (b) CB free carrier density along vertical direction at the middle of trap layer during retention.

Fig 9 compares the final trapped electron distribution at 10^6s of TANOS devices with 4/8/12 nm gate stack under different retention temperature, which further elucidates that TB tunneling through thin oxide (4nm) is the primary cause of charge loss at room temperature (300K) and electron spreading along BL governs the retention characteristics at high temperature (350K). The electron distribution at high temperature is a consequence of electron spreading along BL and BT tunneling through tunneling oxide in vertical direction of cell 2. The shift of threshold voltage for the 4/8/12 nm and 6/8/12 nm devices under different retention temperature is shown in Fig. 10.

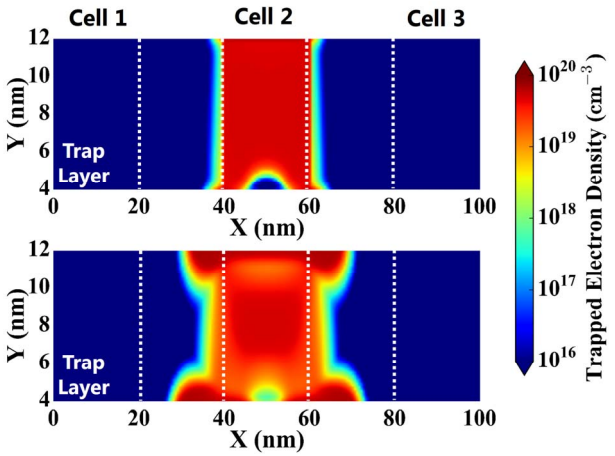


Fig. 9. Trapped electron density at 10^6s for a 4/ 8/12 nm TANOS device under different retention temperatures (top: 300K, bottom: 350K).

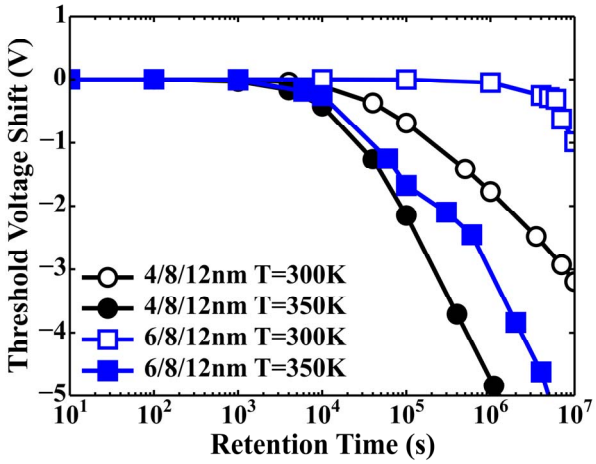


Fig. 10. Threshold voltage shift of devices with different tunnel oxide thickness under 300K and 350K retention temperature.

IV. Conclusion

A 2D self-consistent numerical simulation approach with drift-diffusion transport scheme for CT-NAND is presented in this paper, able to describe the charge transport both along BL and in vertical direction in memory structure to explore the retention behavior. This work can help to design and optimize 3D stackable CT-NAND architectures.

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