Simulation of Light-Illuminated STM Measurements

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***Abstract*— A three dimensional simulation system for light-illuminated STM measurements is proposed for the first time combining semiconductor process and device simulators with an FDTD solver. Photo-generation rates estimated from light intensity obtained from the FDTD solver are incorporated into a semiconductor device simulation of a device structure including a semiconductor sample and an STM probe tip. Tunneling currents between the STM probe and the sample are solved consistently with current continuity equations in the semiconductor sample. The usefulness of the proposed method is demonstrated through a case of UV-laser-illuminated STM measurement of a silicon nanowire.**

Keywords—scanning tunneling microscopy STM; semiconductor device simulation; light-illuminated STM; tunneling currents; finite-difference time-domain FDTD;

I. INTRODUCTION

Scanning tunneling microscopy (STM) is a powerful metrology in investigating microscopic physical quantity distributions in semiconductor devices. Tunneling currents between an STM probe tip and a semiconductor sample include information at or near the sample surface, such as surface topology, potential, energy band, and carrier concentration. By scanning the sample surface, such physical quantities can be obtained with good spatial resolution [1]. The importance of the measurement of such quantities in nanometer scale resolution is increasing.

One of the problems of the STM measurements of semiconductor samples is that the STM probe tip potential affects the sample surface and change the surface potential, band energy, and carrier concentration. This effect called tip induced band bending can be considered by the three-dimensional potential based simulator developed by the authors [2]. Another problem is the effect of electric currents flowing in the semiconductor sample. This effect also changes the surface physical quantities and affects the measurement results. To consider this effect, current continuity equations are required to be solved in the simulation. Such an STM simulator has also been developed by the authors [3].

However, when the STM measurement is applied to the samples of novel and thin semiconductor devices such as FinFETs and nanowires, there occurs a situation in which carriers in the semiconductor sample is depleted. In such a case, it may occur that the STM cannot measure the tunneling current corresponding to electrons in the valence band or in the conduction band of the semiconductor sample. Therefore an idea to supply sufficient carriers is required to measure such thin devices.

II. LIGHT ILLUMINATED STM MEASUREMENTS

In the case of thin semiconductor devices such as fins or nanowires, carriers are required to be supplied in order to measure tunnel currents corresponding to valence or conduction electrons of the semiconductor sample. The light-illuminated STM metrology [4] [5] or the laser-combined STM [6] is a powerful solution generating carriers in the thin semiconductor samples by photo-generations. (Fig.1)

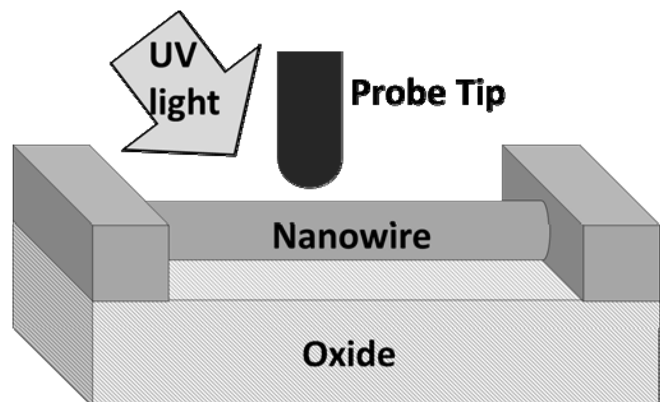

Fig. 1. Illustration of the light-illuminated STM measurement. The light creates phogo-generated carriers in the nanowire and enhance tunneling currents between the sample and the probe tip.

In the illuminated STM measurements, both electrons and holes in the thin semiconductor structure are supplied by photo-generation, and generated electrons can be tunneled into the STM probe tip. For such purposes, ultra-violet (UV) light with very short absorption length in semiconductors is often used to generate many carriers effectively in the thin layer. The problem of this method is that the generated carriers change the physical quantities such as electro-static potential and carrier concentration in the semiconductor sample. To investigate this effect precisely, a computer simulation for this measurement method is required.

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III. Simulation of the Light-Illuminated STM

The light-illuminated STM metrology is physically simulated by semiconductor process and device simulators combined with an FDTD solver. The process simulator is used to create simulation structure including the semiconductor sample and the STM probe tip. Light intensity distribution caused by the illumination is calculated by the FDTD solver. Finally tunneling currents including photo-generated carriers consistently with current continuity equations in the semiconductor sample is solved by the device simulator. The concept of the proposed simulation system is shown in Fig. 2.

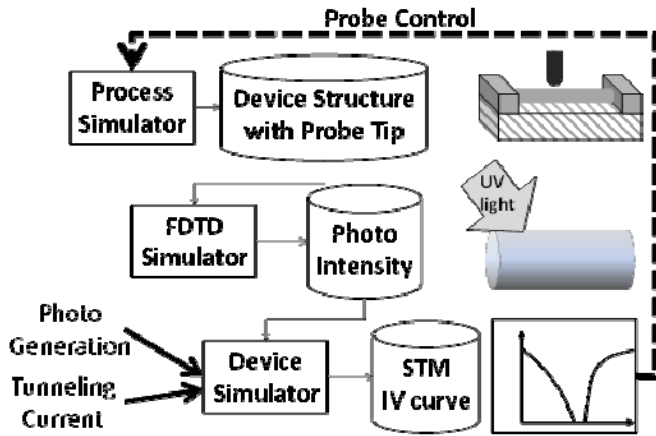

Fig. 2. The proposed simulation system for the light-illuminated STM measurements. The system is composed of a process simulator, an FDTD solver, and a device simulator. All simulators are three-dimensional ones.

For process and device simulations, 3D TCAD system HyENEXSS [7] is used. Device structures are created by the process simulator, including the tungsten STM probe tip as the part of the device sample structure as shown in Fig. 3. In the process simulator, complex shapes such as nanowires and STM probe tips can be represented by unstructured meshes of HyENEXSS.

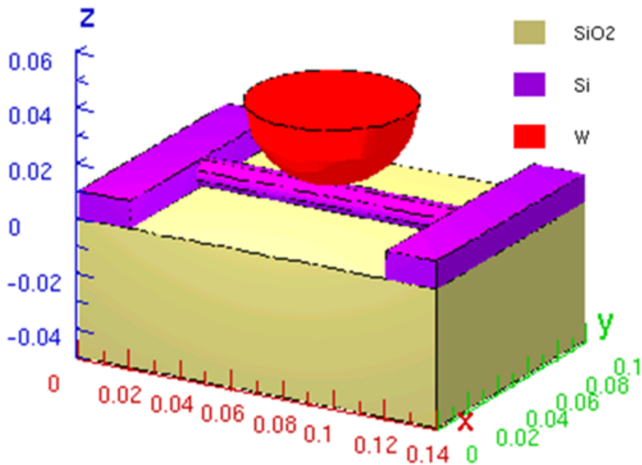

Fig. 3. Device structure created by the process simulator. This is an example of a silicon nanowire and a tungsten probe tip. The radius of the curvature of the probe tip and the tip-sample distance are controlled by the present STM simulation system.

Light intensity distribution caused by the light illumination is calculated as shown in Fig. 4 by the FDTD simulation code which is developed by the authors. The device structure created by the process simulator is converted into the input structure data for the FDTD simulator. Because orthogonal meshes are used to represent the device structure in the FDTD simulation, the complex structures created by the process simulator are approximated by rectangular solid. Therefore minute meshes are required to keep the accuracy of the device structure.

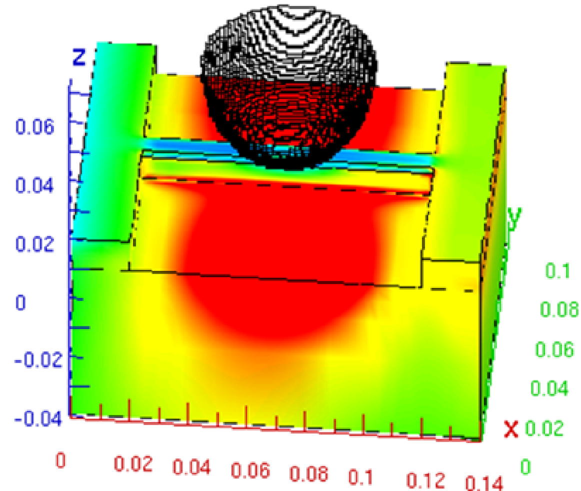

Fig. 4. Electric field intensity distributions calculated by the FDTD simulation. Device structure created by the process simulation is converted to the input structure file of the FDTD simulator.

Photo generation rates are estimated from the photo intensity as shown in Fig. 5, and are incorporated into device simulations. The device simulator calculates STM tunnel *I-V* curves consistently with the Poisson and the current continuity equations for semiconductors, and consistently with the photo-generated carriers. Because the device simulator uses unstructured meshes, the generation rates are calculated by interpolating the electric field values on the orthogonal mesh points of the FDTD solver into the unstructured meshes of the device simulator.

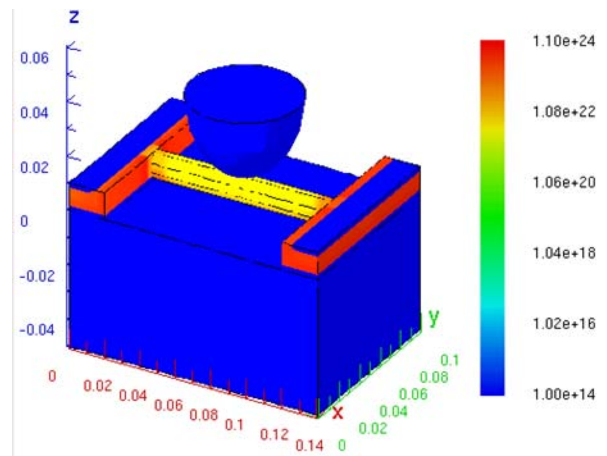

Fig. 5. Photo generation rates in the silicon nanowire estimated from the photo intensity. The unit of the generation rates is $cm^{-3}s^{-1}$.

IV. Simulation Results

Fig. 6 shows the *I-V* curves (a) with and (b) without illumination, assuming a Si nanowire of 10nm diameter and 100nm length, and STM probe tip with the radius of the curvature of 30nm. The source and the drain regions are 10^{20} cm^{-3} N-type, and the channel region (nanowire) is 10^{14} cm^{-3} P-type. The tunnel gap distance between the probe and the sample distance is 0.7nm. The work-function of the tungsten probe tip is assumed to be the same value as the mid gap of silicon. In the illuminated case, tunnel currents are observed in negative probe bias conditions, not observed in the case without illumination. The tunnel currents can be calculated separately for the valence and the conduction band of the semiconductor sample by the device simulator. In Fig. 6, tunnel currents corresponding to the conduction band are shown by closed circles, and those of the valence band are shown by closed triangles. The tunnel direction in the range of the probe bias $V_{PROBE} > 0$ is from the sample to the probe tip, and for $V_{PROBE} < 0$, from the probe tip to the sample.

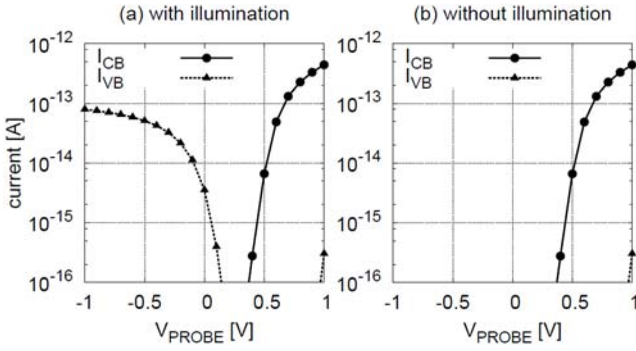

Fig. 6. Simulated *I-V* curves (a) with (left) and (b) without (right) illumination. Tunnel currents associated to the conduction band of the semiconductor is shown by closed circules, and those associated to the valence band by closed triangles.

Contrary to the discussions in the previous sections, the tunnel currents corresponding to electrons from the semiconductor sample to the probe tip are identical for the illuminated and not illuminated cases in the $V_{PROBE} > 0$ conditions. This is because the existence of the source and drain which supply electrons in sufficient speed into the conduction band of the inversion layer of the nanowire channel region.

On the other hand, tunnel currents I_{VB} in $V_{PROBE} < 0$ conditions which related to the valence band of the semiconductor appear drastically by the light illumination. The difference of the *I-V* curves are explained by the hole concentrations in the Si nanowire as shown in Fig. 7. In the illuminated case (a), the surface concentration below the probe tip center is the order of 10^{19} cm^{-3}, while in the case without illumination (b), 10^{12} cm^{-3}. High hole concentration in the illuminated case is caused by photo generations, and those holes behave as the target of electron tunneling from the probe tip to the valence band of Si. In the case without illumination, the amount of holes is lower by seven orders, which is the reason why tunneling currents cannot be observed in the negative probe bias conditions.

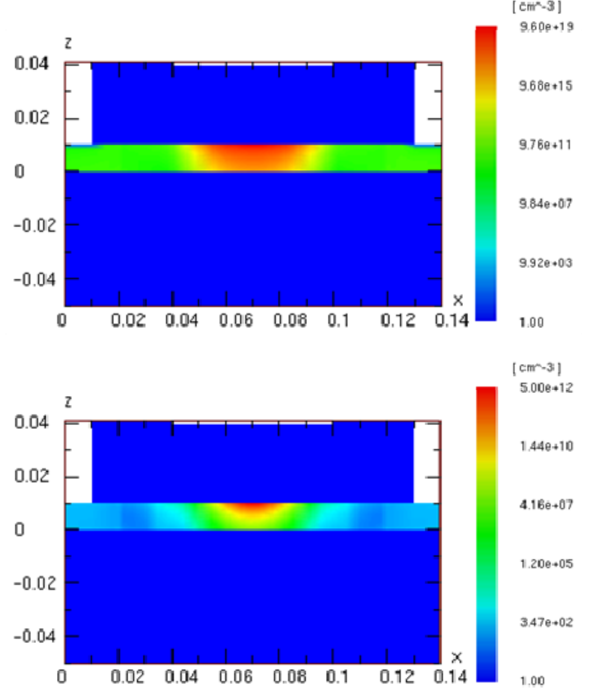

Fig. 7. (a) (upper) Hole concentrations at *V*probe=-1V with illumination. (b) (lower) Hole concentrations at *V*probe=-1V without illumination.

Before the simulation such a situation is not supposed by the authors that the *I-V* curves differ in $V_{PROBE} < 0$ not in $V_{PROBE} > 0$. This implies the importance of carrier supply speeds quantitatively predicted by the simulation. The tunneled electrons from the probe tip to the valence band of the silicon nanowire recombine with holes, and decreased holes are only supplied by slow Shockley-Read-Hall mechanisms. Thus the tunneling from the probe tip to the valence band is prohibited in the not illuminated case.

The simulation calculation CPU time strongly depends on the numbers and sizes of meshes. In the present case, CPU-time for the process simulation consists of 31949 mesh points is 30 sec., for the FDTD solver consists of 42228 mesh points is 3 min., and for the device simulation consists of 31949 mesh points is 3.5 hours. Without illumination, the device simulation CPU time is 1.2 hours.

V. Conclusions

A simulation system for illuminated STM measurements is developed and applied to the case of Si nanowire measurements. The simulation clarifies the effect of photo-generation and predicts the STM *I-V* curves. This implies that the present simulation optimizes the configurations of the illuminated STM measurements to measure thin semiconductor devices such as fin or nanowire transistors where carriers are not sufficiently supplied. The present simulation system enables the quantitative investigation of behaviors of photo-generated carriers in semiconductor devices during the STM measurements.

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