Semi-Classical Ensemble Monte Carlo Simulator Using Innovative Quantum Corrections for Nano-Scale n-Channel FinFETs

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***Abstract*—We present a three-dimensional semi-classical ensemble Monte Carlo device simulator with novel quantum corrections. The simulator includes a beyond-Fermi treatment of Pauli-Exclusion-blocked scattering, and a valley-dependent treatment of various quantum confinement effects. Quantum corrections to the potential are used not only to model redistribution of carriers in real space, but also to model altered energy valley offsets and associated redistribution of carriers in *k*-space, and quantum-confined scattering rates, including a new approach to model surface roughness scattering. We illustrate the capabilities of the simulator using different levels of modeling, with an emphasis on modeling nano-scale FinFETs with degenerate carrier populations, including III-V devices.**

Keywords—FinFET, Monte Carlo, quantum-confinement, surface roughness scattering, III-V, n-MOS, scaling, degenerate semiconductors, device modeling.

I. INTRODUCTION

Nonconventional geometries and materials are being explored as options for complementary metal oxide semiconductor (CMOS) device scaling [1-4]. FinFETs (Fin-shaped field effect transistors) increase gate control for improved transconductance, subthreshold slope and reduced short-channel effects [4,5]. Such gate control has been motivation enough for industry leaders to overcome the significant fabrication challenges posed by FinFETs [6]. Already incorporated at the 22 nm technology node, FinFETs are likely to drive scaling in future nodes [7]. Moreover, high-mobility III-Vs are also being considered.

As FinFETs shrink, predictive simulation becomes increasingly important for exploring the complex design space. Toward this end, we have developed a semi-classical ensemble Monte Carlo simulator to efficiently model transport in three-dimensional (3D) nano-scale n-channel FinFETs, while capturing multiple quantum-mechanical effects. A beyond-Fermi treatment of Pauli-Exclusion-blocked scattering is provided. Various effects of confinement are accounted for, including not only redistribution of carriers in real space, but also redistribution of carriers among energy valleys, and quantum-confined scattering, including a new approach to modeling surface roughness scattering. The simulator is illustrated through modeling $In_{0.53}Ga_{0.47}As$ and reference Si tri-gate semiconductor-on-insulator (SOI) ultra-scaled FinFETs.

II. MODEL

A. Monte Carlo in the Bulk Limit

We first verified our simulation approach in bulk. We calculate bulk electron phonon scattering rates according to the Golden Rule as standard [8, 9]. Our simulator includes acoustic phonon scattering, intervalley optical phonon scattering, polar optical phonon scattering in III-Vs, and degenerate ionized impurity scattering using Thomas-Fermi screening [10].

We include non-parabolic band structures and multiple valleys per material: six Δ-valleys in Si; and one Γ-, four L-, and three X-valleys in III-Vs. We follow Fischetti [11] for material-specific effective masses, band non-parabolicities, and deformation potentials. For III-V ternary alloys, we employ a virtual crystal approximation, including bowing parameters for effective masses and intervalley separations [12], and associated alloy scattering [13].

We have generated carrier drift-velocity vs. electric field curves for $In_{0.53}Ga_{0.47}As$ and Si to verify bulk transport, providing excellent agreement with experimental data [9,14,15] requiring only small tuning of various deformation potentials.

B. Quantum Corrections for Degeneracy

Modern CMOS devices incorporate massive doping densities to reduce the parasitic source/drain resistance, and have ultra-low effective oxide thicknesses (EOTs), leading to degenerate carrier populations in the source, drain and, above threshold, in the channel. Under these conditions, Pauli-Exclusion-Principle based blocking (Pauli-blocking, or PB) of scattering must be considered, and carrier populations can be forced well into the bands, particularly for electrons in III-Vs.

PB is achieved by considering the occupation probability f of the final (f) states f_f in the Golden Rule transition rate S from initial (i) to the various final states, as

$$S_{\mathrm{i}\to\mathrm{f}} = \frac{2\pi}{\hbar}|\langle\mathrm{i}|V|\mathrm{f}\rangle|^2\delta(E_\mathrm{i} - E_\mathrm{f} + \Delta E)[1 - f_\mathrm{f}]. \quad (1)$$

When considered in Monte Carlo *device* (vs. bulk) simulation, f typically is approximated as a Fermi distribution locally, with position dependent Fermi energy (chemical potential) and temperature consistent with the carrier population and average energy [16-18]. However, this assumption for f_f cannot be justified in far-from-equilibrium conditions in nano-scale devices approaching the ballistic limit of performance.

We avoid *a priori* assumptions about the form of f. Instead, we calculate f self-consistently as a function of position $\mathbf{r}$, discretized energy E_l, energy valley g, and (currently) forward or backward direction of propagation $\pm$. This basic approach (with more **k**-space refinement) has been used in bulk simulations before [8,9]. Here, we extend this technique to 3D devices. To gather sufficient statistics, we average over nearest neighbor grid sites, and over time periods Δt (here 120 fs) that are small compared to normal switching transients. Specifically, we calculate f as,

$$f(\mathbf{r}, E_l, g, \pm) = \frac{N(\mathbf{r}, E_l, g, \pm)}{\Delta t \cdot D(E_l, g)/2} \quad (2)$$

where $N(\mathbf{r}, E_l, g, \pm)$ is the number of electrons with parameters $\mathbf{r}, E_l, g, \pm$ over the time period Δt, and $D(E_l, g)/2$ is the average density of states within the energy range ΔE about E_l, for valley g and either propagation direction. Recently, we have incorporated the use of *sub-carriers*, or fractional carriers, to avoid artifacts of classical molecular dynamic carrier-carrier scattering, which intrinsically neglects PB of final state pairs. In the process, we have further improved the statistics for calculating the PB itself.

Under equilibrium conditions the thus-calculated occupation probabilities should and do reduce to a Fermi distribution, as illustrated in Fig. 1 for the Γ-valley of $In_{0.53}Ga_{0.47}As$. Both low-electron densities with no PB and associated classical (Boltzmann) distributions, and highly degenerate electron concentrations of $n = 5\times10^{19}$ cm^{-3} (with inelastic scattering self-consistently limited by f_f) were simulated. The difference in the electronic distributions with and without PB will inform our illustrative device results later.

C. 3D FinFET Structure

We create a 3D cubic mesh with a 1 nm resolution. The grid-mesh couples to the charge distribution and potential/force profile via a nearest-grid point assignment to avoid self-forces.

A representative simulated FinFET structure is shown in Fig. 2. In this work, the fin channel sits above a 5 nm thick buried oxide (BOX) layer. The source and drain reservoirs and extensions are doped while the channel is left undoped. The source/drain height T_{SD} is 25 nm, while its length L_{SD} is 10 nm. The source/drain extension length L_{EXT} is 6 nm. The width of the fin W_{FIN} is 6 nm, while the height of the fin T_{FIN} is 20 nm. The length of the gate L_G is also 20 nm. The physical gate oxide thickness T_{OX} is 5 nm of hi-k hafnium-oxide, giving an effective oxide thickness (EOT) of ~0.9 nm. The channel orientation is [100] in the direction of transport, ideal for n-channel Si devices if not for Si CMOS as a whole.

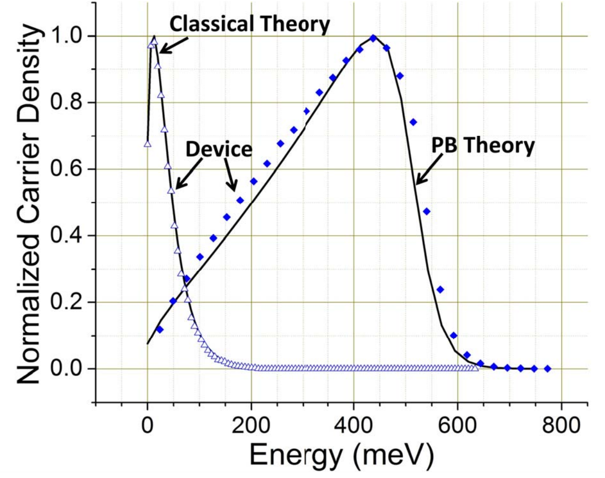

Fig. 1 Peak-normalized Monte Carlo simulated electron distributions in the Γ-valley of $In_{0.53}Ga_{0.47}As$ under equilibrium, for low electron densities in which Pauli-blocking is negligible (classical), and for a highly-degenerate electron concentration of n=5×10^{19} cm^{-3} with self-consistently calculated PB of inelastic scattering. The product of the density of states per unit energy and the Fermi distribution are provided for reference as precise theoretical results.

D. Quantum Corrections for Confinement

We add quantum corrections to account for confinement effects in deeply scaled FinFET devices. This approach has been adapted to 3D from earlier 2D work [19,20], and further extended to address surface roughness (SR) scattering within complex 2D confinement profiles.

As in [19] for 2D structures, we solve an effective-mass Schrödinger Equation in 2D slices i transverse to the transport direction as a function of position along the channel *and energy valley*, calculating the eigenstates of the confined geometry and a corresponding total thermal probability density ρ^{QM}. We also provide a non-parabolicity correction for these eigen-energies. We define the local quantum correction V_{OC} to produce a semi-classical charge distribution, ρ^{Cl}, matching the quantum-mechanical channel distribution,

$$\rho^{Cl}\left(V(x, y, z) + V_{QC}(y, z, g, i)\right) \equiv \rho^{QM}\left(V(y, z, i)\right), \quad (3)$$

where g again labels the energy valley. Here x is the transport direction, y is in the plane of the substrate normal to x, and z is normal to the substrate. The quantum correction modifies the electrostatic potential to produce the desired quantum-mechanical *space*-charge distribution *for each valley* through the application of classical forces and scattering. Fig. 3 illustrates this effect in an $In_{0.53}Ga_{0.47}As$ FinFET.

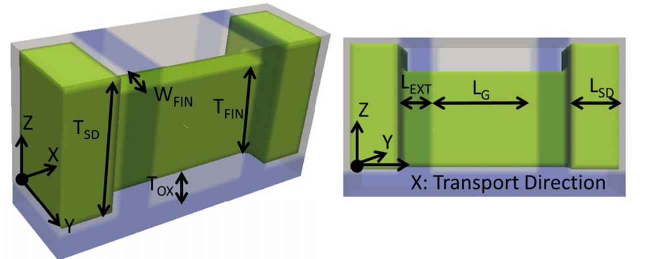

Fig. 2 Example FinFET device structure with relevant dimensions.

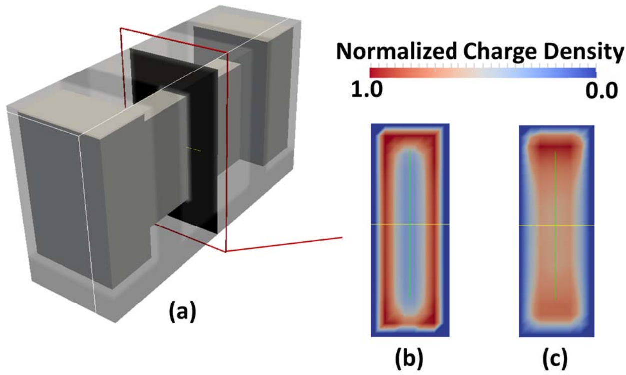

Fig. 3 $In_{0.53}Ga_{0.47}As$ FinFET (a) space-charge density across a cut transverse to the transport direction with (b) no quantum corrections and (c) with quantum corrections, where electrons are repelled from the interface.

The valley-dependent V_{OC} can also lead to redistribution of charges among energy valleys. In $In_{0.53}Ga_{0.47}As$ quantum wells, the light Γ-valley electrons experience stronger quantum confinement and, thus, a larger V_{OC} than the heavier peripheral L- and X-valley electrons. Thus, the energy separation between the Γ-valley and the peripheral valleys is reduced, allowing the latter to become more readily occupied, particularly with degenerate carrier populations as to be seen.

Scattering rates of quantum-confined carriers can be shown to oscillate about bulk scattering rates *when the energy is referenced to the expectation value of the position-dependent valley edge*. However, the minimum energy the quantum-confined carrier can have relative to this expected energy is greater than zero, and increases with increasing quantum confinement. In this way, it can be seen that quantum confinement can significantly increase minimum scattering rates for, particularly, randomizing/deformation potential phonon scattering. To model this effect, here as in [20], we use the final state energy *relative to the uncorrected classical potential V* to determine the scattering rates between *available* states above the quantum corrected potential $V + V_{QC}$.

Additionally, we now use V_{OC} to model surface-roughness (SR) scattering. In both triangular wells (Ando's Model) [21] and in narrow infinite square wells [22], SR rates follow the quantum confinement energy cubed. Thus, (although refinement is possible in the future) we use a rate

$$\tau_{SR}^{-1} = C V_{QC}^{3}, \qquad (4)$$

where C is a calibration coefficient. Thus, we reproduce these two limiting behaviors as well as necessarily limiting to an inverse-width dependence *on average* for wide square wells, while providing a simple mechanism for interpolating to more general confinement geometries. Here we have calibrated the SR scattering rate to that obtained previously for a Si/thermal SiO_2 interface (with quantum confined phonon scattering considered in both cases) [23].

III. Illustrative Device Simulation Results

We illustrate our simulator by showing drain current I_D vs. gate voltage V_G results in Fig. 4 with different levels of

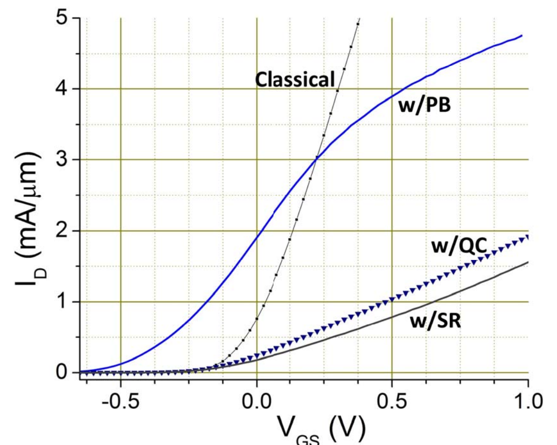

Fig. 4 $In_{0.53}Ga_{0.47}As$ FinFET I_D-V_G transfer characteristics for different levels of modeling, for W_{FIN} = 6 nm and source/drain doping $N_D = 5\times10^{19}$ cm^{-3}.

modeling for a FinFET of 6 nm fin width W_{FIN} and source and drain doping of $N_D = 5\times10^{19}$ cm^{-3}. Adding PB of scattering, along with contact injection from Fermi distributions, degrades the $In_{0.53}Ga_{0.47}As$ transconductance g_m compared to the classical limit, due to greatly reduced (worse) density-of-states capacitance initially, and for larger gate voltages by shifting carriers to the lower thermal velocity peripheral valleys, as seen in Fig. 5. The threshold voltage V_T is also reduced by raising the Fermi level E_f in the source (and drain), consistent with Fig. 1. Adding quantum confinement in the channel shifts the threshold voltage more positive by adding to the effective source-to-channel potential seen by incident carriers. However, it further reduces the transconductance largely by shifting now a sizable majority of carriers to the peripheral valleys above threshold. Finally, SR scattering further reduces the drive current. Incidentally, the shifting of light-mass carriers to the low quantum-confinement peripheral valleys actually helps minimize the relative impact of SR.

We provide comparisons to Si versions of otherwise identical FinFETs in Table I, except we choose a still-conservative-for-Si source/drain doping of $N_D = 2\times10^{20}$ cm^{-3}. Si

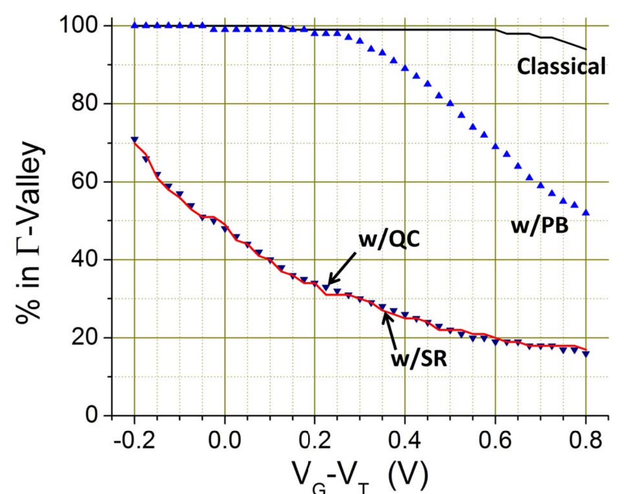

Fig. 5 Percent of electrons in the Γ-valley moving over the channel barrier in an $In_{0.53}Ga_{0.47}As$ FinFET given different levels of modeling. Quantum confinement scatters carriers into the higher-mass valleys.

TABLE I. MATERIAL COMPARISON FOR FINFET DEVICES

Material	$In_{0.53}Ga_{0.47}As$: 5×10^19 cm^-3				Si: 2×10^20 cm^-3			
Model	*Cl*	*PB*	*QC*	*SR*	*Cl*	*PB*	*QC*	*SR*
g_m (mS/μm)	12.1	4.9	1.7	1.4	3.6	4.2	3.6	3.0
V_T (V)	0.0	-0.4	-0.15	-0.15	-0.15	-0.2	0.0	0.0

TABLE II. TRANSCONDUCTANCE AS VARIED BY FIN WIDTH

Material	$In_{0.53}Ga_{0.47}As$: 5×10^19 cm^-3			Si: 2×10^20 cm^-3		
Width (nm)	*11*	*6*	*3*	*11*	*6*	*3*
without SR	2.6	1.7	0.81	4.0	3.6	2.5
with SR	2.3	1.4	0.56	3.4	3.0	1.7

is less sensitive to PB of scattering due to its larger density of states, and less sensitive to quantum confinement due to a larger confinement effective mass. Indeed, for the [100] channel orientation, confinement helps localize carriers to the optimal [010] (fin-normal) valleys. This relative insensitivity to degeneracy and confinement effects leads to better performance for the Si-FinFETs, despite larger thermal velocities and conductivities to be found in bulk $In_{0.53}Ga_{0.47}As$. (The greater available doping in Si also helps, but $N_D=5\times10^{19}$ cm^{-3} Si *also* outperforms the $In_{0.53}Ga_{0.47}As$ devices of the same doping, if by less, in simulations not shown.)

We also examined g_m as a function of fin width, as shown in Table II, in units of mS/μm. The lighter-mass $In_{0.53}Ga_{0.47}As$ system suffers more severe degradation with decreasing fin width due to its pronounced vulnerability to quantum effects.

IV. CONCLUSION

We have developed a 3D semi-classical ensemble Monte Carlo simulator with novel quantum corrections for PB of scattering and multiple confinement effects, including alteration of energy valley separations and a novel treatment of SR scattering. We have demonstrated the importance of the modeled effects through simulation of degenerately doped semiconductor $In_{0.53}Ga_{0.47}As$ and Si FinFETs. Detrimental effects thereof were found particularly in the former system.

ACKNOWLEDGMENT

We would like to thank Dr. John K. David for his prior work on this code. We thank GLOBAL FOUNDRIES INC. and the Semiconductor Research Corporation for their collaboration and financial support. We thank the Texas Advanced Computing Center for their generous allocation of remarkable supercomputing resources, and technical expertise. Dax M. Crum thanks the National Science Foundation for a graduate research fellowship (GRFP).

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