Experimental and theoretical investigation of the 'apparent' mobility degradation in Bulk and UTBB-FDSOI devices: a focus on the near-spacer-region resistance.

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This paper investigates the mobility 'apparent' channel length dependency in nanometric devices. Based on a series of current and capacitance measurements, we report clear $(V_G)^{-1}$ dependencies of the access resistance in Bulk but also in FDSOI devices. We show that the $\mu_{eff} - L_{eff}$ degradation observed at small L can be inferred from this gate-bias dependency. By means of numerical simulation, we show that in the near-spacer-region injection velocity saturation occurs and the spreading resistance exhibits a $(V_G)^{-1}$ dependency. A comparison between Bulk and FDSOI devices clearly shows that even in the absence of LDD-counter-doping (pocket), and channel doping, the near-spacer-region resistance is far to be negligible and can contribute up to ~30% of the total resistance ($R_{TOT} = V_D / I_{DS}$) of a ~22nm device.

I. Introduction

Several papers have investigated the 'apparent' channel length dependency of the mobility in nanometric devices [1-3]. By means of Monte Carlo simulations [1] it has been shown that the degradation observed at small L can be inferred from the additional 'ballistic' mobility adding a supplementary term in the Matthiessen mobility. However, some other research groups [2-3] have shown that the effect of this resistance alone is unable to quantitavely explain the experiments. The experimental mobility reduction must thus be partly due to either some other scattering mechanisms localized near the LDD (Light Doped Drain) junction or to systematic errors in the characterization procedures of the shortest devices.

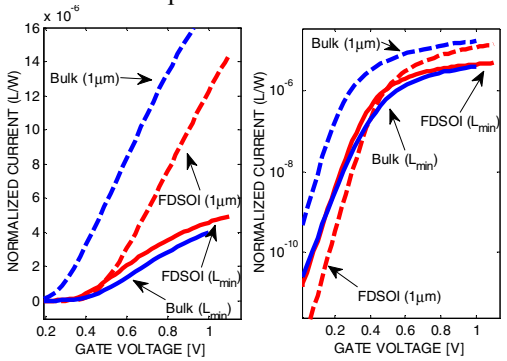

Figure 1: Long channel and short channel linear current (normalized by W/L) as a function of Gate voltage for bulk and NFDSOI NMOSFETs; V_{DS}=0.05V.

This paper highlights the impact of the near-LDD region on the apparent mobility degradation. It is shown that in this region a significant quasi-Fermi level drop occurs (leading to lateral fields exceeding 3x10^{4}V/cm, even at very low VD). From this observation one can infer that up to 30% of the total device resistance is spread in this region. A link with 'macroscopic' ballistic mobility models is also discussed.

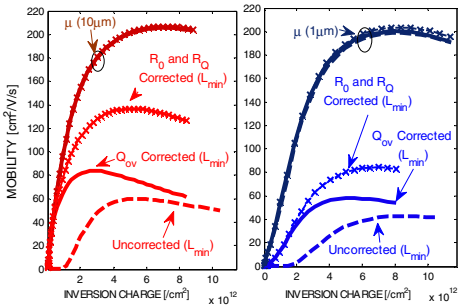

Figure 2: Split-CV NMOS mobility as a function of Q_{inv}. Overlap charge (Q_{ov}) [1] and R_0+R_Q correction (see text); R_0=50Ω.µm in FDSOI (left) and 40Ω.µm in Bulk (right).

II. Analysis of the Mobility Extraction Methods

We have performed a series of current (Fig. 1) and capacitance measurements in Metal Gate Bulk and FDSOI devices featuring 1.8nm High-K oxide on top of ~1.1 nm interfacial SiO_2 layer. The corresponding split-CV mobility, corrected from overlap capacitances, effective channel length (L_{eff}=L-ΔL) [4] and access resistance are shown in Fig. 2. The mobility vs. L_{eff} shown in Fig. 3 exhibits a strong degradation for the shortest devices that is more pronounced in the bulk devices. Also superimposed are the values obtained from the gain factor using the 'Y'-method [5].

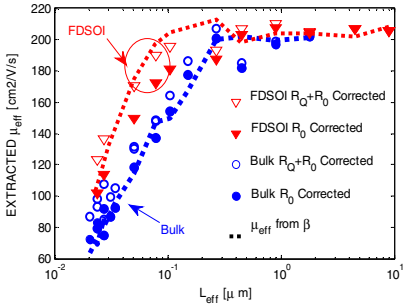

Figure 3: Split-CV NMOS mobility at Qinv=6e12/cm2 and mobility from 1/β. Impact of quantum resistance corrections. ΔL=-1.2nm in FDSOI and -1.4nm in Bulk.

We now discuss the validity of this extraction method [5] when the series resistance exhibits a pronounced $(V_G)^{-1}$ dependency. Such dependency is expected and comes from the resistance of the LDD-region [6]. To this, one can add the quantum (or ballistic) 'contact' resistance also exhibiting such dependency:

$$R_Q \approx \sqrt{2\pi \cdot \mathrm{m} \cdot \mathrm{kT}}/(q \cdot Cox \cdot (V_G - V_{TH})) = 2 \cdot \sigma_B \cdot (V_G - V_{TH})^{-1} \quad \text{(eq 1)}$$

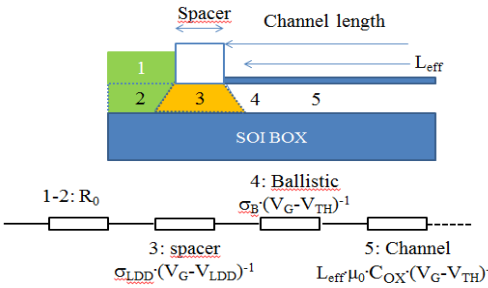

Figure 4: Resistor network with V_G and L dependencies. The equivalent threshold voltage V_{LDD} of the spacer resistance can be different from the transistor one V_{TH}. The mobility degradation is neglected (θ=0).

An equivalent 'macroscopic' resistor network is shown in fig. 4. For simplicity let's consider that the total series resistance accounting for both effects writes (using a single parameter σ):

$$R = 2 \cdot R_0 + 2 \cdot \sigma \cdot (V_G - V_{TH})^{-1} \quad \text{(eq 2)}$$

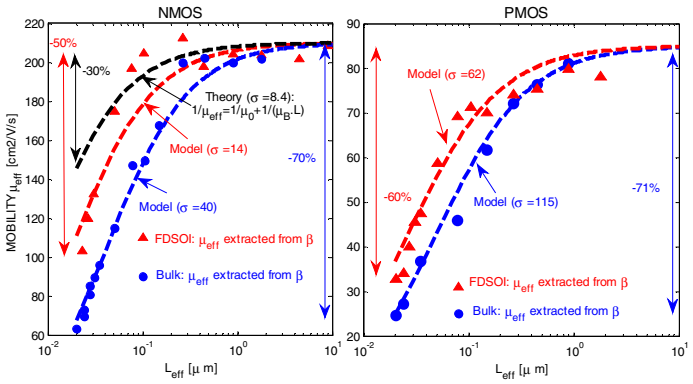

Figure 5: Experimental mobility compared to model Eq.3 with an 'effective' μ_B of 23.8 cm^2/(V.s.nm), 14.3cm^2/(V.s.nm), and 5cm^2/(V.s.nm) for NMOS (corresponding to σ =8.4, 14, and 40 Ω.µm.V). For PMOS, the 'effective' μ_B are 3.2 cm^2/(V.s.nm), and 1.7cm^2/(V.s.nm), which corresponds to σ =62, and 115 Ω.µm.V.

With some algebra, it can be proven that in that case, the gain factor $\beta_{eff} = \mu_{eff} C_{OX} W/L$ extracted from the slope of the Y-function [5] $Y = I_D/\sqrt{gm} \approx \sqrt{\beta_{eff} V_{DS}} \cdot (V_G - V_{TH})$ writes:

$$1/\beta_{eff} = L/\mu_0 C_{OX} W + 2\sigma/W, \quad \text{(eq. 3)}$$

where μ_0 is the long channel mobility.

This implies that the extracted effective mobility μ_{eff} becomes L-dependent as:

$$1/\mu_{eff} = 1/\mu_0 + 2 \cdot \sigma \cdot C_{OX}/L \cdot \quad \text{(eq. 3')}$$

Considering an 'apparent' ballistic mobility per unit length $\mu_B = (2 \cdot \sigma_B \cdot C_{OX})^{-1}$, eq. 3 can be re-written using a more familiar form [3-5]:

$$1/\mu_{eff} = 1/\mu_0 + 1/(L \cdot \mu_B) \quad \text{(eq. 3'')}$$

Our measurements in Fig. 5 (μ_B ~ *5 – 14* cm^2/(V.s.nm)) are in-line with other experimental results [1-3], but significantly lower than the theoretical ballistic mobility per unit length:

$$\mu_B \approx q/\sqrt{2\pi \cdot \mathrm{m} \cdot \mathrm{kT}} = 23.8\,\mathrm{cm}^2/(\mathrm{V.s.nm}) \quad \text{(eq 4)}$$

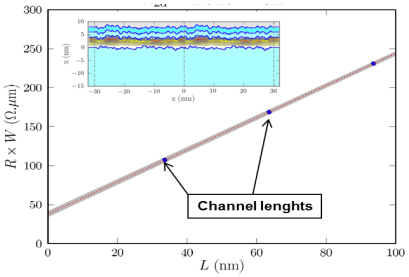

Figure 6: Resistance calculated with NEGF in an ideal channel-device where the length is doubled and tripled.

III. Quantum 'Contact' Resistance

The quantum or 'ballistic' resistance [2-7], which is due to the finite number of available sub-bands, puts a lower fundamental limit to the total channel resistance. Even in the absence of contact and spreading resistances, the intersect of the $R_{TOT}(L_{eff})$ plot for L_{eff}=*0* exhibits a finite value. This is depicted in Fig. 6, where R_{TOT} is calculated with NEGF [9-10] for an ideal channel-device where the length is doubled and tripled.

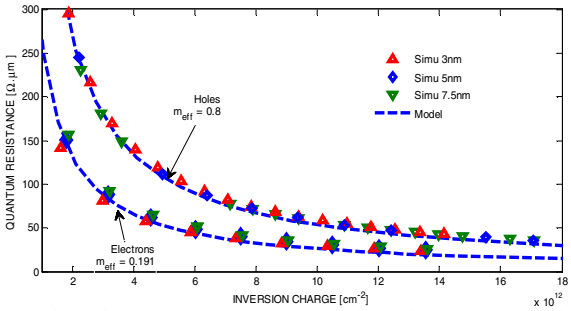

Figure 7: Holes and electrons quantum resistance calculated with a Poisson-Schrodinger for various channel thicknesses and eq. 1.

It is worth noticing that eq.1 neglect carrier degeneracy. It has been noted [3] that in strong inversion μ_B can be slightly lower (16.4 – 17.5 cm^2/(V.s.nm)) than the non-degenerate limit. However, it is clear that it is not sufficient to explain the observed 'apparent' ballistic mobility. Moreover the channel thickness in FDSOI devices does not significantly change the quantum resistance as confirmed by our calculations in Fig. 7.

In a device, featuring spacers and S/D regions, the impact of the quantum resistance along the channel is more subtle to localize. Fig. 8 shows the quasi-Fermi levels calculated from the NEGF density (supposing a heated Maxwellian carrier distribution). Despite some statistical oscillations originated from the random placement of the LDD dopant atoms and the surface roughness, a significant quasi-Fermi level drop in the

near-LDD region is observable. On the contrary, the channel operates in a diffusive regime as testified by the nearly linear voltage drop occurring in this region.

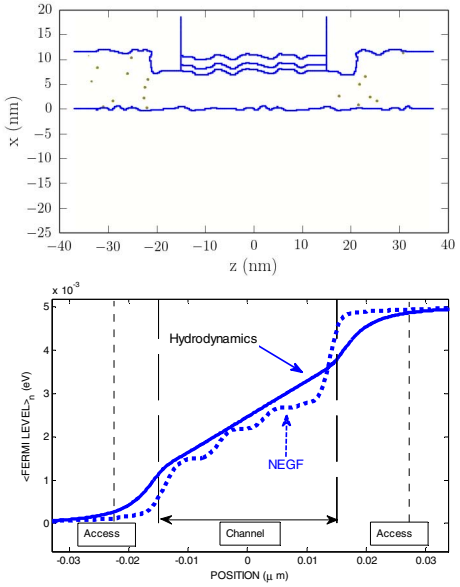

Figure 8 : FDSOI structure (top) featuring SiON/HfO2/Metal gate with remote coulomb interfacial charges (QHK=3e13/cm2), surface roughness and discrete LDD dopants (or continuum in Hydrodynamics). Quasi Fermi levels (bottom) calculated along the channel. NEGF (dashed) compared to density-gradient-corrected Hydrodynamics-based simulations (lines). Inversion charge 1.3e13/cm^2.

IV. Series Resistance

Series resistance extraction methods have been extensively discussed in literature (see e.g. [7]).

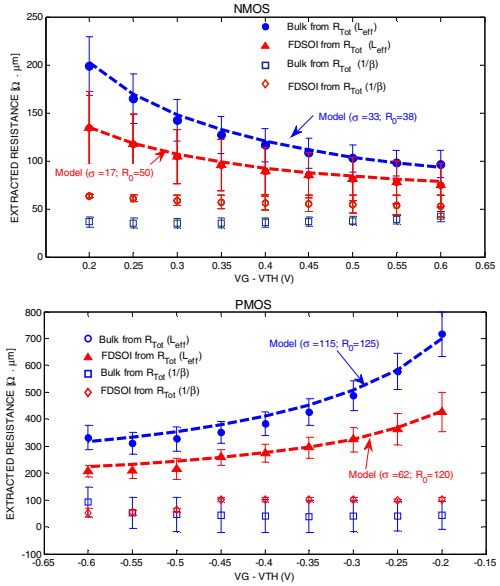

Figure 9 : NMOS (top) and PMOS (Bottom) extracted resistances using $R_{TOT}(L_{eff})$ and $R_{TOT}(1/\beta)$ methods (see text), and model Eq. 2. Error-bars show the uncertainty depending on the range of device lengths considered for the extraction [7].

Fig. 9 compares the values obtained by the intercept of the $R_{TOT}(L_{eff})$ and $R_{TOT}(1/\beta_{eff})$ plots [7]. Results obtained with the former method exhibits a clear $(V_G - V_{TH})^{-1}$ dependency which is not the case with the later one. With series resistance given by eq. 2 the '$R_{TOT}(1/\beta_{eff})$' method [2,6] partially cancels the V_G dependency and the extracted value is $R = 2 \cdot R_0 - 2 \cdot \theta \cdot \sigma$ (with θ the mobility degradation parameter). A similar behaviour is observed for both NMOS and PMOS devices. It is worth noting that the value of the parameter σ used in eq. 2 used to fit the Gate voltage dependency of the extracted access resistance using the intercept of $R_{TOT}(L_{eff})$, corresponds to the value used in eq. 3' to predict the mobility degradation vs L_{eff} shown in Fig. 5.

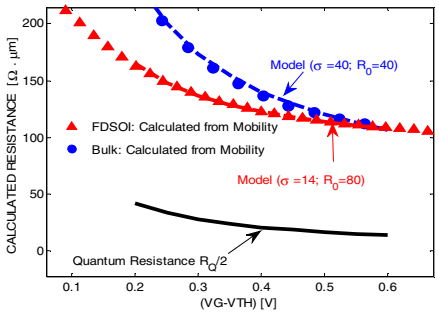

Figure 10 : Series resistance calculated to match the measured long and short channel normalized current.

Fig. 9 shows the series resistance $R_\mu(V_G)$ calculated to match long and short channel normalized current using:

$$I_D \cdot (L/W) = \mu_{Long} \cdot Q_{inv} \cdot V_D / (1 + \mu_{Long} \cdot Q_{inv} \cdot 2 \cdot R_\mu) \cdot$$

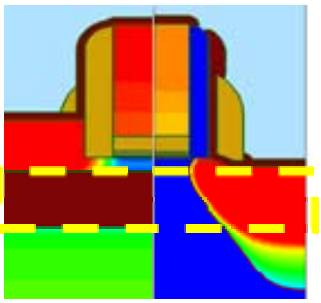

Figure 11 : Doping level by means of process simulation for short FDSOI and Bulk MOSFETs of Fig. 1.

V. The Near-Spacer-Region Resistance

To gain more insight into the $\sigma \cdot (VG - V_{TH})^{-1}$ dependency of the series resistance let us performed realistic process (Fig. 11) and device simulations using well calibrated density-gradient-corrected Hydrodynamics-based simulations [10-12]. In a Hydrodynamics (or Drift diffusion) simulation it is possible to capture (at least qualitatively) the effect of ballistic carrier velocity by means of the usual velocity saturation model [11]. A direct comparison with NEGF simulations of Fig. 8 shows a reasonable agreement using the default 'bulk' silicon value of V_{sat}=1.04x10^{7}cm/s. This can be compared to the slightly larger injection ballistic velocity values (V_{inj}=1.23x10^{7}cm/s in non-degenerated silicon). Even if the apparent saturation of the carrier velocity can be different from that of velocity saturation (the rate of energy gain from the lateral field is equal to the rate of energy loss to the surrounding by phonon

scattering), and originated by the finite number of quantum states available, the effect on carrier transport (at a given temperature) is similar (see Fig. 8). Fig. 12 shows spreading resistance obtained by averaging the pseudo-Fermi level voltage drop across a section normal to the current density direction.

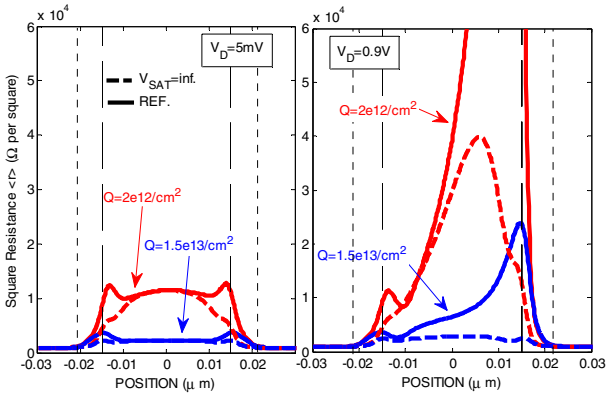

Figure 12: NFDSOI square resistance along current path for two inversion charge densities, in the linear and saturated regime. Structure of Fig.8; vertical lines correspond to the edges of the spacers and the channel.

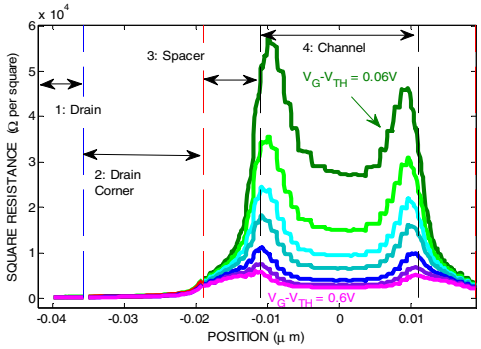

Figure 13: NFDSOI square resistance along current path for V_G-V_{TH}=0.06V up to V_G-V_{TH}=0.6V; V_{DS}=0.05V.

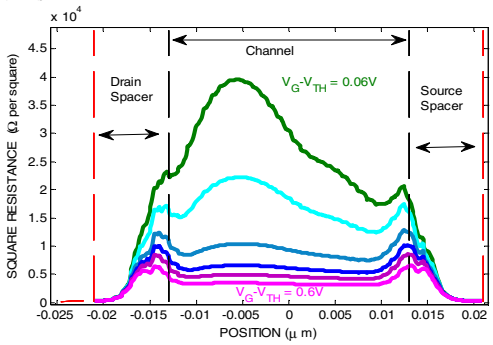

Figure 14: Same as Fig. 13 but for Bulk NMOSFET

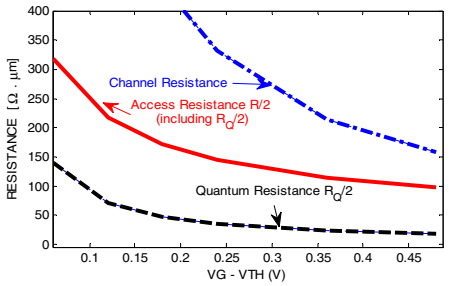

Figure 15: Simulated resistance as a function of VG-VTH in a 22nm FDSOI device (corresponding to the experimental data in fig.9).

The impact of the velocity saturation on the linear regime is fairly localized in the spacer/LDD-region while in the saturated regime the entire channel is impacted.

The spreading resistance along the current path for the two devices of Fig.1 are shown in Figs. 13 and 14. One can distinguish; 1/ the vertical raised S/D region, 2/ the curved corner region, 3/ the spacer region, and 4/ the channel region. It can be clearly noticed that below the spacer and at the entrance of the channel, the resistance exhibits a V_G-dependent peak. It is worth noticing that this highly resistive region is similar in the FDSOI device and the bulk device featuring LDD-pockets. One notes that it is precisely in this region that the previously mentioned velocity saturation occurs (even at very low V_D). In Fig. 15 the resistance of this spacer region is reported at a function of V_G. Fig. 16 shows that the near-spacer spreading resistance does not significantly change with channel length.

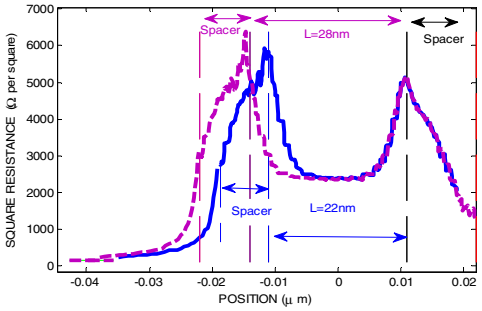

Figure 16: Square resistance along current path for two FDSOI devices with channel lengths of 22nm and 28nm. The near-spacer-region- resistance is identical in both devices; V_G-V_{TH}=0.6V.

VI. Conclusion

The near-spacer/LDD region exhibits a significant resistance that does not depend on L (in that sense it can be considered as a series resistance) but significantly changes with V_G. We found out that the 'apparent' mobility degradation observed in short device is consistent with the impact of this V_G-dependent resistance on the device current.

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