3D Atomistic Simulations of Bulk, FDSOI and Fin FETs Sensitivity to Oxide Reliability

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***Abstract*— New architectures introduction succeeded in reducing the device performances dispersion in scaled transistors, but as a consequence the relative importance of oxide reliability increased. In this work we present original results of charged interface traps impact on bulk, FDSOI and Fin FETs performances. Traps time constants are analyzed and recoverable and permanent degradation proportions are derived. Finally transistors parameters dispersion increase with time are simulated demonstrating our simulator ability to provide accurate reliability predictions for these three architectures.**

Keywords—Reliability; simulation; Bias Temperature Instabilities; FinFET; FDSOI.

I. INTRODUCTION

Statistical Variability (SV) arising from the discreetness of charge and granularity of matter increases with scaling [1] critically affecting circuit performance and shrinking design margins [2]. It motivates the introduction of low-doped channel transistor architectures like FinFETs and FDSOI MOSFETs since Random Dopant Fluctuations (RDF) is the dominant SV source for bulk MOSFETs. Recent studies for bulk transistors [3] proposed a comprehensive approach to oxide reliability, stating that several oxide degradation phenomena, such as Random Telegraph Noise, Bias Temperature Instabilities and Hot Carrier Injection (RTN, BTI and HCI) can be interpreted as discrete trapping events for which trap level and trap activation energy dispersions induce the trapping events dispersion in time, whereas a simple exponential distribution of threshold voltage shift for bulk devices can properly model traps electrostatic impact [4]. This is however not the case for low doped channel transistors nor for 3D architectures [5]. In this paper we investigate for the first time the impact of the trap level dispersion on BTI charge for the three transistor architectures. Time constants ratio is used to determinate trap average expression and to identify permanent and recoverable parts of the BTI degradation.

II. METHODOLOGY

A. Simulated Devices

Fig. 1 presents the three investigated devices from the 22 nm technology node, comparing classic bulk MOSFET with innovative architectures, namely Fully Depleted Silicon On Insulator (FDSOI) FET and FinFET. All of them feature 1.2 nm gate oxide thickness. The fin height is 25 nm, its width 10 nm and its buried oxide is 20 nm thick, whereas the FDSOI one is 10 nm under a 6 nm of silicon channel layer. Doping levels are detailed in [8]. Equivalent gate width for the Fin is 60 nm thus we have to consider the same width for planar devices in order to perform a fair comparison of variability and reliability impact.

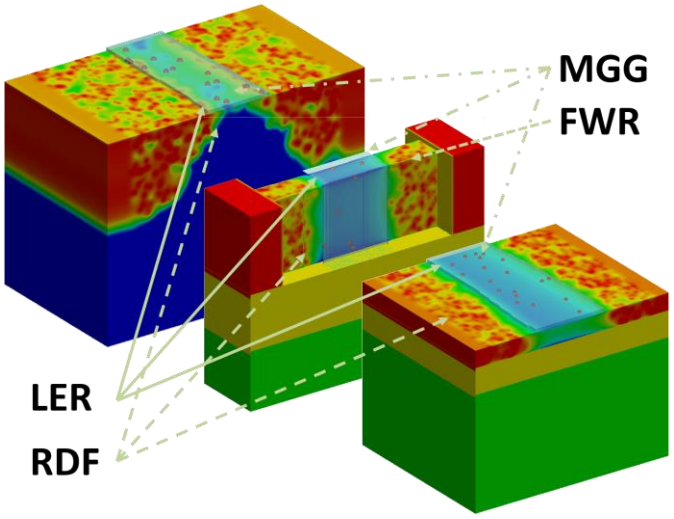

Fig. 1. Investigated bulk FDSOI and Fin FETs, all of them featuring a 60 nm wide effectife gate; considered SV sources are Random Dopants Fluctuations (RDF), Metal Gate Granularity (MGG), Line Edge Roughness (LER) and Fin Width Roughness (FWR).

These transistors are suffering from various SV sources: random discrete dopants are introduced through RDF, Metal Gate Granularity (MGG) is defined by two grains with an average diameter of 5 nm and respective work functions 4.021 and 4.221 eV. Lithography intrinsic limitations are taken into account with Line Edge Roughness (LER) and Fin Width Roughness (FER) with a roughness mean square of 3.8 nm and a 25 nm correlation length. Details on SV integration into GSS GARAND simulator can be found in [1, 6].

B. Simulation Methodology

Our unified reliability framework is used to drive the 3D atomistic simulator GARAND [1, 6] within a quantum

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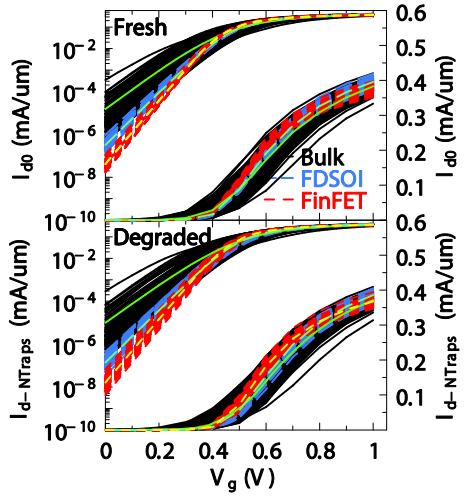

Fig. 2. 100 Id-Vg traces fof each investigated transistors before stress (up) and for all traps charged (down) at V_d=50 mV, with an average trap density of 10^{12} cm^{-2}; averages are plotted in lighter colors.

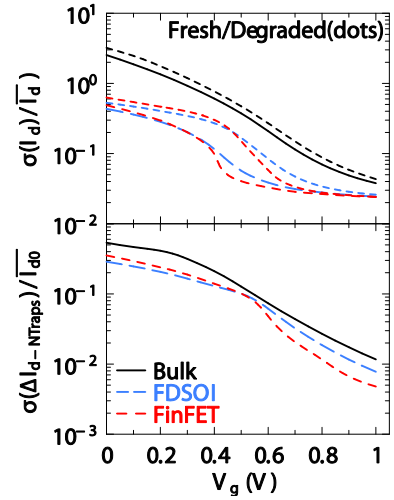

Fig. 3. Normalized standard deviation as a function of V^g for the current of fresh and degraded bulk, FDSOI and Fin FETs transistors (up) and for the drain current shift induced by the charge of all traps on the current (down) at V_d=50 mV.

corrected drift-diffusion approach [7]. Traps are uniformly distributed in the oxide with an average surface density of 10^{12} cm^{-2} and feature an average trap level Et equal to the Fermi level in the middle of the channel $E_{f\text{-}middle}$ and a cross-section $\sigma=10^{-14}$ cm-2. The activation energy E_a accounting for multi-phonon activated transitions is fixed in this work at 0.6 eV. Charge trapping time constants are computed as in [9], using the tunnelling rates and detrapping times are obtained through the detailed balance as in [9]. A state vector approach allows complex charging and discharging simulations of BTI and RTN degradations and accurate reliability predictions.

III. Results

Devices characteristics are illustrated in Fig. 2 in fresh and degraded conditions. Obviously the built-in variability is much more critical for bulk FETs because of the source to drain percolative behavior induced by RDF [1, 9]. This is worth noting that RDF is also impacting I_{on} current distributions for

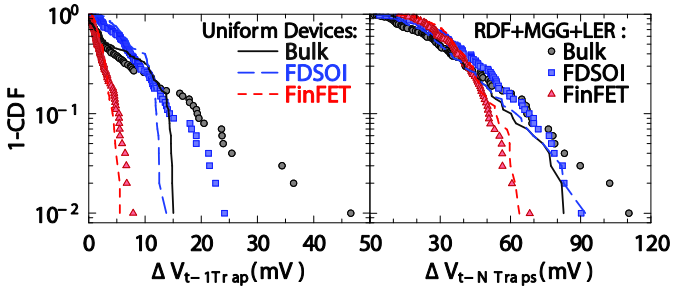

Fig. 4. Bulk, FDSOI and FinFET threshold voltage shift ΔVt induced by (left) a single trap (right) a poissonian number of traps averaged on 10^{12} cm^{-2} with (symbols) and without SV (lines). 22 nm square gate are considered for planar devices.

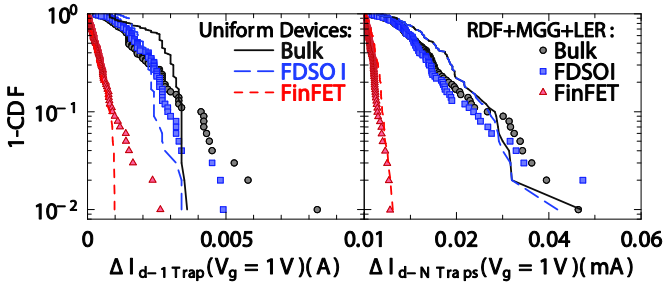

Fig. 5. Bulk, FDSOI and FinFET drain current shift ΔId induced by (left) a single trap (right) a poissonian number of traps averaged on 10^{12} cm^{-2} with (symbols) and without SV (lines).

channel dopants free architectures due to source and drain doping affecting access resistors in the ohmic regime [10]. The FDSOI MOSFETs and the FinFETs have better Ion/Ioff ratios and are also less affected by traps. Normalized standard deviations as a function of the gate voltage are given for the initial SV and in degraded transistors in Fig. 3 as well as the specific impact of charged traps. As the standard deviation are normalized, the FDSOI transistors show superior robustness towards variability and reliability in the subthreshold region, while FinFETs are superior above threshold. Gate bias increase leads first to the formation of the inversion layer, sensitive to SV and trapping. Once the inversion layer is formed the conduction regime changes and the final value of the dispersion for both FDOI and Fin FETs are only due to discrete dopants in the source and drain extensions. For bulk devices this plateau has not been reached and RDF is still playing a role in the current dispersion at Vg=1V. This is also the case for degraded devices with a Vg shift, since trapped charges are more and more screened with the increase of Vg as illustrated in lower Fig. 3.

A. *Traps Electrostatic Impact*

Fig. 4 and Fig. 5 illustrate the impact of single and multi-traps on the threshold voltage V_t and on the on current I_d at V_g=1 V respectively for uniform and atomistic devices suffering from SV, note that LER includes FWR for the FinFETs. The comparison between trap impact in uniform device, i.e. without SV, and atomistic devices demonstrates the relative importance of variability sources. Indeed the huge variation of a single trap impact on uniform and atomistic bulk transistors is due to the possibility for a single trap to totally block the source to drain percolative path at threshold voltage.

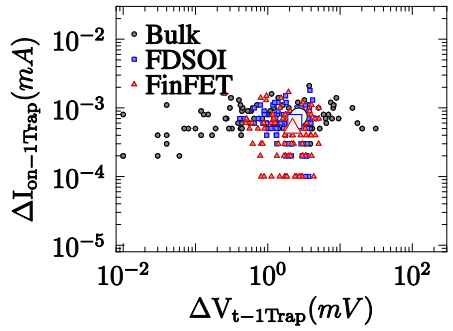

Fig. 6. Impact of a single trap on the on current vs impact of the same trap on the threshold voltage. Larger symbols represent the average impacts.

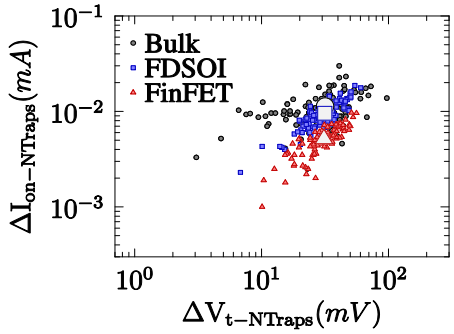

Fig. 7. Impact of a all traps charged on the on current vs impact of the same traps on the threshold voltage for a 10^{12} cm^{-2} trap density.

On the other hand for FDSOI FETs this difference is mainly due to MGG; different work functions in one or the other part of a device results in different thresholds voltage for those parts and therefore in traps impact dispersion. Once more the 3D inversion layer in FinFETs strongly reduces traps impact.

The impact of a single charged trap on the on current cannot be deduced from its impact on the threshold voltage at relatively low level of degradation since no correlations are observed in Fig. 6 between those two parameters. The corresponding correlation factors are 0.04, -0.10 and -0.03 for bulk, FDSOI and FinFETs respectively. On the contrary at higher trap density the correlations increase up to 0.43, 0.85 and 0.84. This high charge density is hence acting as a charged sheet, therefore impacting the whole device in every functioning regimes.

B. Traps Types Identification

Average time constant ratios allow to discriminate between preferentially uncharged, preferentially charged and RTN traps. Results are presented in Fig. 8; one can immediately notice that fixed trap level case is not realistic, for it is not rendering the measured time constants [11, 12]. In the variable trap level range case, the relative position of the trap level in respect to the Fermi level for a given bias determines the proportions between different trap types. At V_g=V_t bulk, FDSOI and FinFETs presents respectively 10.3, 11.8 and 8.6 % of RTN traps, whereas at V_g=1 V we obtain 9.3, 7.8 and 8.5 %. As the Fin time constants dispersion is much broader due to its architecture [8]. The proportion of preferentially charged traps in the FinFET does not change significantly with the gate bias

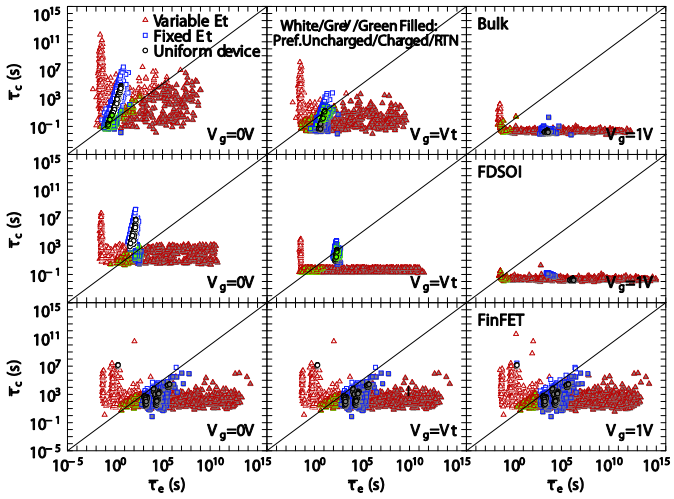

Fig. 8. Average capture time τ_c vs emission time τ_e for a fixed trap level E_t= $E_{f\text{-}middle}$ in uniform and atomistic devices and for a 1eV spread of E_t around $E_{f\text{-}middle}$. τ_c/τ_e ratio discriminates preferentially charged, uncharged and RTN traps.

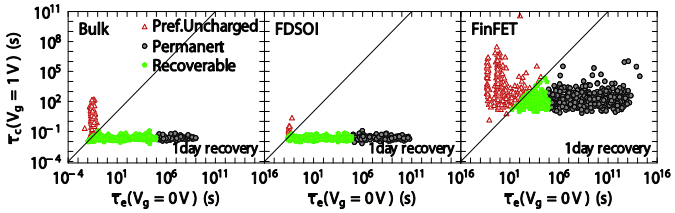

Fig. 9. Average capture time τ_c vs emission time τ_e for a 1eV spread of E_t around $E_{f\text{-}middle}$. τ_c/τ_e ratio discriminates permanent and recoverable parts.

staying close to 57%, whereas this proportion is doubling for the planar transistors reaching 72.3 and 89.6% for bulk and FDSOI at V_g=1 V.

C. Reliability Projections

Based on the same considerations but this time using the average emission times at low gate, to simulate a realistic discharge, Fig. 9 identifies the proportions of permanent and recoverable parts of the traps. Whereas 55.6 and 59.6% of the traps in respectively Bulk and FDSOI devices will discharge after one day of recovery, only 15.1% of the FinFETs traps are recoverable. These proportions do not include the preferentially uncharged traps and are based on average rates. However, the trapping is a stochastic phenomenon, so that several charging and discharging sequences are required for the same device to obtain realistic projections as in [9]. In this work we simply consider a single one, illustrated in Fig. 10 and we derive the average and standard deviation as a function of trap density in Fig. 11 showing that traps electrostatic impact are similar for FDSOI and FinFET [8] but traps dynamics are much more favorable to FinFETs as illustrated in Fig. 12. Those results can be used to calibrate a circuit level reliability interpolator in combination with GSS Mystic compact model extractor [9,].

IV. Conclusion

The electrostatic impact of single and multiple charges has been investigated for planar and 3D devices and the time

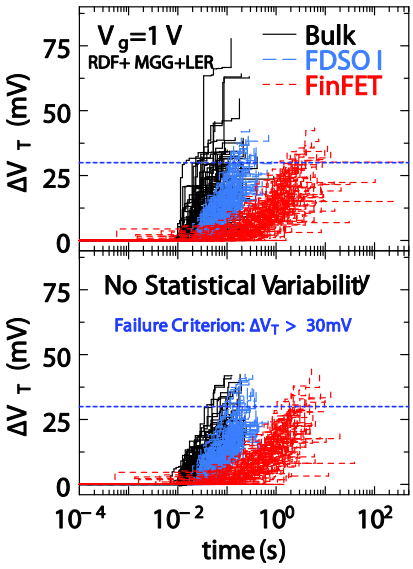

Fig. 10. BTI charge traces at V_g=1 V and V_d=50 mV for 100 atomistic transistors featuring a Poisson distribution averaged on $N_T=10^{12}$ cm^{-2}, for bulk, FDSOI and Fin FETs, with (up) and without (down) Statistical Variability (SV).

dependent added dispersion has been presented for an increasing gate bias. Trap level dispersion impact on time constants has been investigated. Their analysis has allowed to identify typical traps behavior; trap type's proportions have been extracted, allowing an estimation of the recoverable part of the traps. BTI charges have been simulated, demonstrating the increased robustness of FinFETs architecture, followed by FDSOI transistors. Finally devices performances dispersion increase with trap density and time have been analyzed, demonstrating the ability of our simulator to provide valuable reliability projections at device level. These results can be transferred up to circuit level, using GSS mystic compact model extractor and reliability interpolator. We are now extending the results to include crystal orientation of Fin walls and buried oxide trapping.

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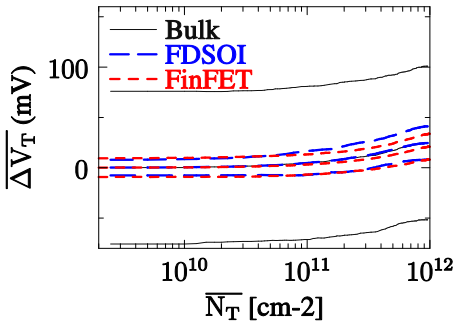

Fig. 11. Average V_t increases and standard deviations as a function of trap density.

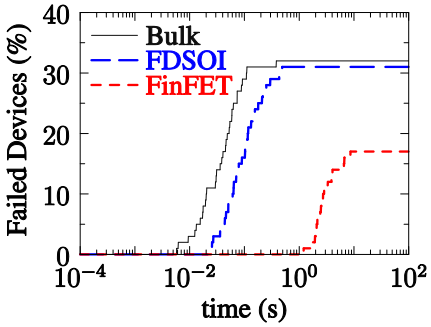

Fig. 12. Percentage of failed device, criterion being ΔV_t>30 mV.