

Time Dependent 3-D Statistical KMC Simulation of High-k Degradation Including Trap Generation and Electron Capture/Emission Dynamic

Yijiao Wang, Peng Huang, Xiaoyan Liu*, Gang Du, Jinfeng Kang*

Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics,
Peking University, Beijing 100871, China
E-mail: *xyliu@ime.pku.edu.cn, *kangjf@pku.edu.cn

Abstract—A comprehensive time dependent three dimensional simulation framework for high- k degradation is developed. In this framework, the models that account for trap generation in high- k , capture/emission dynamic, and statistical variability are incorporated in the simulation. The influence of the trap generation model on distribution of traps, threshold voltage, and the amount of trapped charge is investigated in detail, thereby lay a solid foundation for predicting more accurate design margins at circuit/system level in the future.

Keywords—high- k degradation; trap generation; time dependent; variability; capture/emission

I. INTRODUCTION

Recent studies have demonstrated that in modern nanometer devices the gate oxide degradation during the operational lifetime of MOSFET has become a major reliability threat to the continuation of CMOS scaling [1]-[3]. In particular, the bias temperature instability (BTI) plays the main role in determining the reliability performance of the gate oxide. Moreover, intrinsic statistical variability has been shown to dramatically influence the reliability of nanoscale MOSFET [4], [5], causing the prediction of gate oxide reliability, and the establishment of appropriate design margins at circuit/system level ever difficult. The interplay between the statistical variability and reliability in SiON gate oxide have been investigated by considering the capture/emission dynamic in [6], [7]. However, the interplay in HfO₂/SiO₂ gate oxide is different due to generation of traps in HfO₂ and is not yet well understood [8]. In this paper, by developing a gate oxide degradation (GD) model including trap generation and electron capture/emission dynamic, a 3D statistical simulation framework is presented for time-dependent simulation of high- k oxide degradation and statistical variability.

II. PHYSICAL MODEL AND SIMULATION METHOD

This work is based on a well-scaled 14 nm node n-channel SOI FinFET template as shown in Fig.1 with parameters listed in Table II. The three dimensional atomistic drift-diffusion solver is employed in this work. The quantum confinement effect is taken into account with density gradient corrections. Ideally, the channel is designed to be undoped. However, the

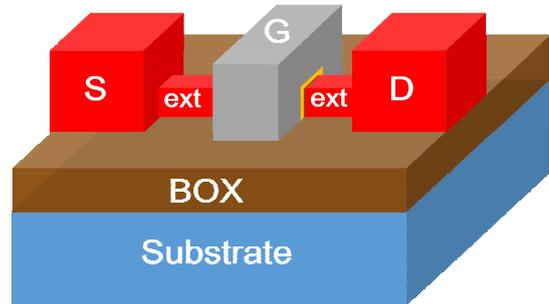


Fig.1 Structure of the simulated 14nm node n-channel SOI FinFET template.

dopants form a lateral distribution in the channel as a result of diffusion from the highly doped S/D extensions. The lateral doping profile in the channel is assumed to be exponential with

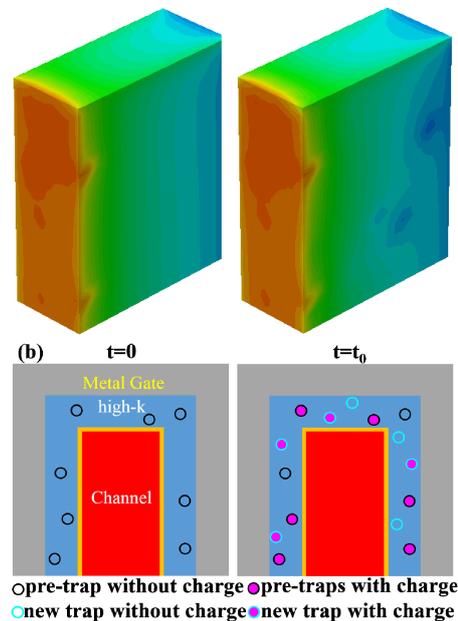


Fig.2 (a) Potential distribution of channel without (left) and with (right) charged trap in gate oxide; (b) Schematic of “GD” model, trap generation and electron capture/emission are taken into account.

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TABLE I. THE EQUATION OF “GD” MODEL

| Probability of traps generation | |
|---|-----|
| $P_G = ft \exp\left(-\frac{E_a - \alpha_a E_{loc}}{k_B T}\right)$ | (1) |
| Analytic model of capture/emission time | |
| $\tau_c = \tau_0 \exp(\mu_c / k_B T)$ | (2) |
| $\tau_e = \tau_0 \exp((\mu_c + \Delta\mu_e) / k_B T)$ | (3) |
| $\mu_c = \mu_{c0} + x\sigma_c - kE_{loc}$ | (4) |
| $\Delta\mu_e = \Delta\mu_{e0} + y\sigma_e + kE'_{loc}$ | (5) |
| * x and y are the normalized varieties | |

f is the attempt-to-escape frequency; E_a is the active energy of traps; $k_B T$ is the thermal energy; α_a is the enhancement factor of the electric field for the lowering of E_a ,

each decade of doping in the lateral extent of the junction fall off per 2nm. As in previous research report, the traps considered in HfO₂ gate oxide is oxygen vacancy which is shallow energy in the forbidden band of HfO₂ and readily capture/emit electron [9], [10]. As shown in Fig.2 (a), the charged traps in gate oxide can influence the potential distribution of channel. Therefore, the physical processes considered in “GD” model are trap generation (number increase) and electron capture/emission (charge modification) as shown in Fig.2 (b). The density of pre-existed traps is 10¹⁹ cm⁻³ with randomized positions. The trap generation is modeled as a random dynamic process with probability governed by equation (1) [11], [12]. The temperature-acceleration and bias-acceleration are both included in our model. The analytic model of capture/emission time presented in [13] is adopted for the electron capture and emission process. The distribution of capture/emission time can be described by equation (2)-(5). Based on our model, a simulator for the high-k degradation is developed as shown in Fig.3, which is divided into two parts. The TCAD part mainly creates random doping profile, assign charged traps, solves 3D Poisson equation, and evaluate the performance such as threshold voltage. Only random dopant fluctuation (RDF) is considered as it is the major intrinsic variation source which contributes to the deviation from the distribution of ΔV_t subject to gate dielectric degradation [7]. The GD model part is responsible for calculate the probability of trap generation and judge the capture/emission state. A kinetic Monte Carlo (KMC) engine is embedded in our simulator, which enables time domain simulation of the high-k degradation.

III. RESULTS AND DISCUSSION

The degradation in high-k gate oxide is simulated with two hundred different devices considering RDF. The devices are

TABLE II. THE PARAMETERS USED IN THIS WORK

| Parameters | VALUES |
|--|-----------------------|
| Gate Length | 20 nm |
| Channel Width | 8.6 nm |
| Channel Height | 24.8 nm |
| E _{OT} | 0.78 nm |
| HfO _x Thickness | 4.25 nm |
| V _O activation energy (E _a) | 2.0 eV |
| σ (E _a) | 0.2 eV |
| f | 5×10 ¹¹ Hz |
| α _a | 0.5 nm |
| τ ₀ | 10 ⁻¹⁰ s |
| μ _c | 1.2 eV |
| Δμ _e | 0.25 eV |
| k | 2 nm |
| σ _c | 0.2 eV |
| σ _e | 0.1 eV |

evaluated at 125 °C with S/D grounded and 2V stress on the metal gate. Fig.4 shows the time-evolution of trap generation and electron capture/emission at the time of 10⁻⁶s, 10⁻⁴s, 10⁻²s, 1s and 100s in the simulated high-k gate oxide of a single device. The electron capture/emission on each trap is tracked. The empty red cycles represent the discharged traps and the red circles filled with black are the charged traps. Simulated results indicate that the amount of the total traps and charged traps visibly increase after 100s stress. The capture/emission

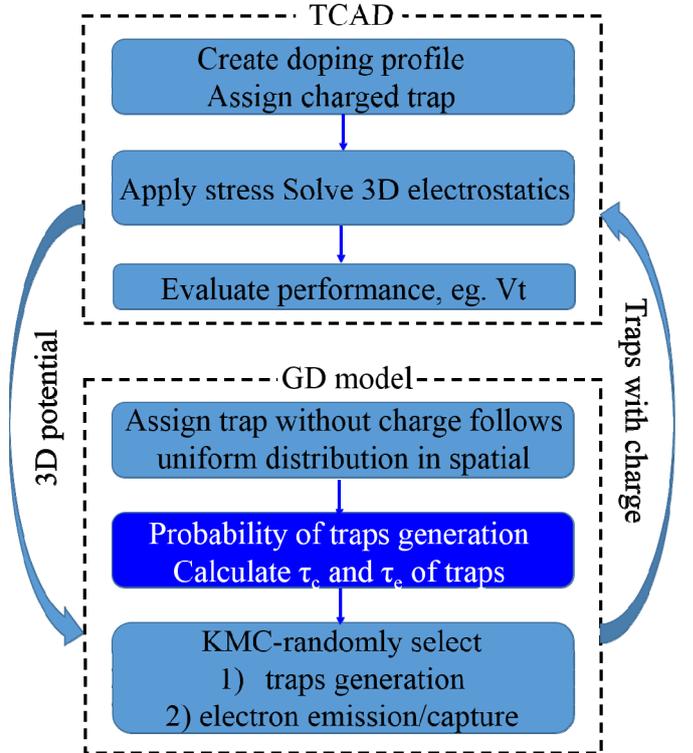


Fig.3 Block diagram of the simulator.

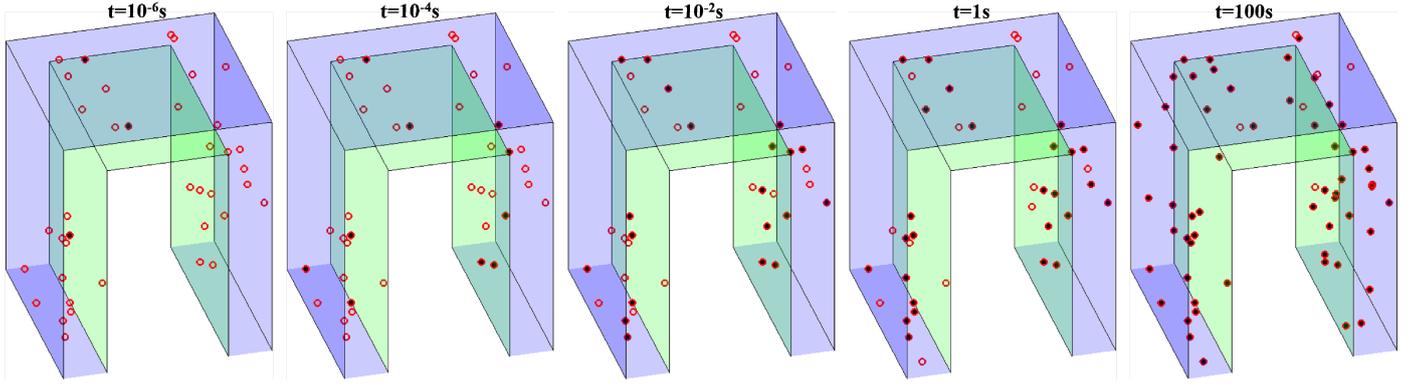


Fig. 4. Time-evolution of trap generation and electron capture/emission at the time of 10^{-6} s, 10^{-4} s, 10^{-2} s, 1s and 100s in the simulated high-k gate oxide of a single device, respectively. Simulated 3-D trap generation and electron capture/emission dynamic under 2V stress and 125 °C evaluated temperature. The empty red circles represent the discharged traps and the red circles filled with black are the charged traps.

transients for the case with and without trap generation are

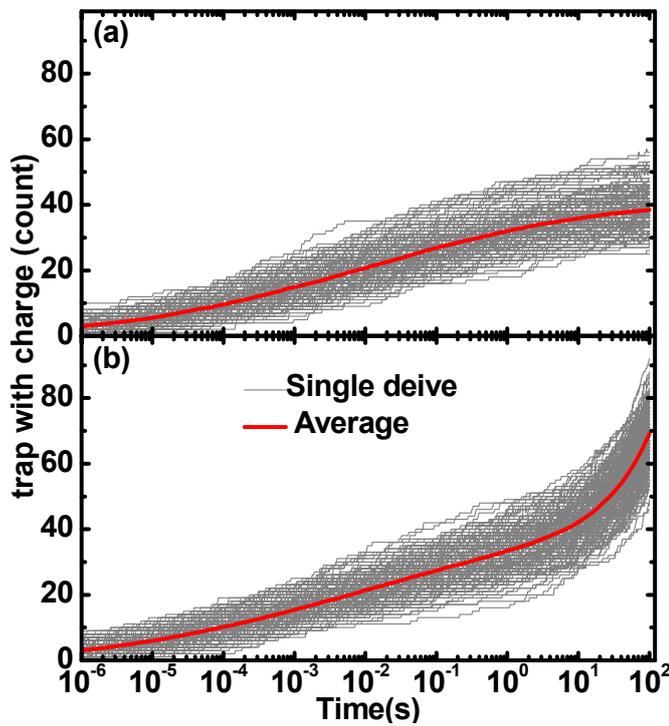


Fig. 5. Simulated capture/emission transients (a) without (b) with trap generation.

compared in Fig.5. The degradation in terms of charged traps lineally increases initially and then saturates when the trap generation is not considered, which is consistent with the simulation results in [14]. This is due to the decrease of the discharged trap. Therefore, the saturation can't be observed when the trap generation is included as shown in Fig.5 (b). The stochastic character of these dynamic and RDF lead to the variation of the charged trap amount as shown in the Fig.5. More importantly, it causes the variation in the ΔV_t at the same stress time as shown in the Fig.6. It should be noted that the relation between average ΔV_t and time deviates from linearity in log-log scale as shown in Fig.6 (a) when the trap generation

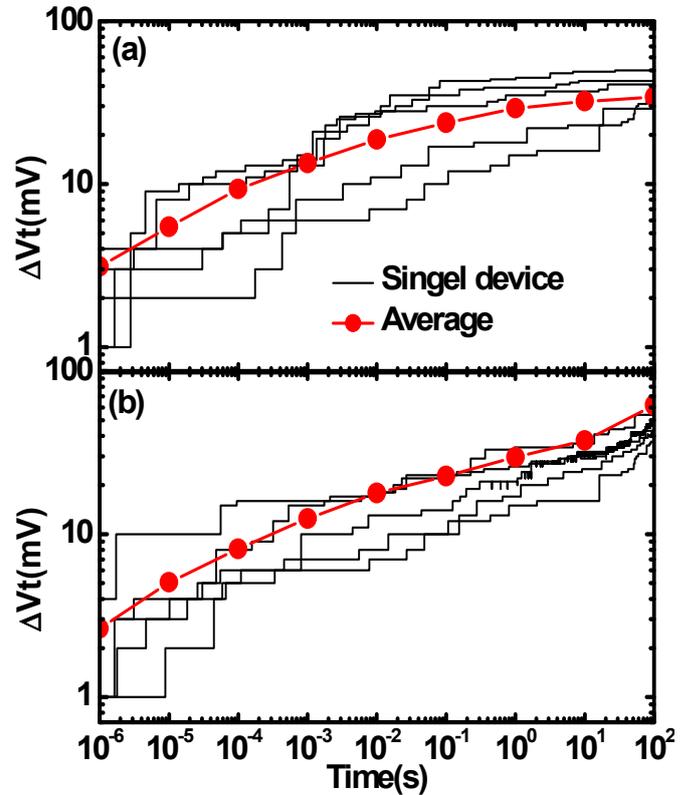


Fig. 6. Simulated threshold voltage shift resulting from electron capture/emission process (a) without (b) with trap generation.

is not considered. The power law time exponent extracted from Fig.6 (b) is 0.146, which is in excellent agreement with experimental measurements [15]. Thus it is necessary to consider the influence of trap generation in high-k gate oxide devices. The time dependent charged trap distribution is shown in Fig.7. It can be seen that with trap generation considered, the distribution of charged traps has wider range and are more Gaussian as time goes on, especially after 1s. Obtaining the distribution and location of charged trap sets the path to investigate the time-dependent interplay between the gate oxide degradation and RDF or other statistical variability.

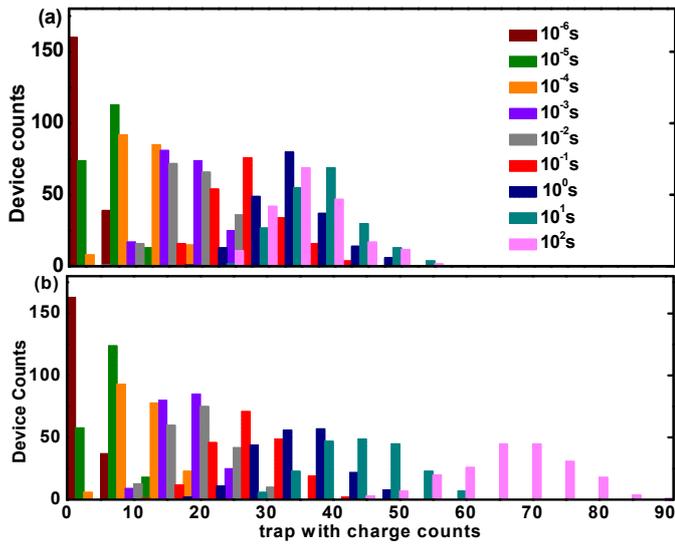


Fig. 7. Distribution of charged traps (a) without (b) with trap generation varies as time goes on.

IV. CONCLUSION

The presented simulation framework well captures the basic physical process, such as trap generation and electron capture/emission of traps, in high-k gate oxide degradation, thus the distribution and location of charged trap can be obtained at any time. More importantly, the three-dimensional, physics-based, time-dependent simulation of gate oxide degradation and the intrinsic statistical variability are integrated, which is a basic premise for predicting more accurate design margins at circuit-system level.

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