Efficient and Universal Method to Design Multiple Field Limiting Rings for Power Devices

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Abstract—For the first time, an efficient and universal method to design multiple field limiting rings (FLR) structure, which applicable to power devices with thin drift layer is proposed. Avalanche breakdown simulations of simplified structures are performed in each three area; the near main junction area, the outmost area, and the other. From simulation results, optimal spacing between each neighboring FLR is efficiently extracted. Phenomena related breakdown voltage determination in each area are also clarified. We demonstrate that the edge termination structures designed along our guidelines succeed to obtain the target blocking voltage in different 600 V class processes.

Keywords- FLR; power devices; thin drift layer; design optimization

I. INTRODUCTION

Ensuring blocking voltage of edge termination is a key factor of high voltage devices. Up to the present various edge termination structures have been proposed, including FLR [1], junction termination extension (JTE) [2], field plate (FP) [3], deep trench termination (DT2) [4], semi-insulating-poly-crystalline silicon (SIPOS) [5], reduced surface field (RESURF) [6], and recess junction termination (RJT) [7]. Among these techniques FLR is widely used in industry because of its proven reliability. Multiple-FLR has many floating region and is difficult to estimate breakdown voltage. Although TCAD is considered as a powerful approach, it is still hard to achieve optimal design in short time. There is a reported methodology in which the relationship between the ring voltage-blocking capability and its spacing to the next ring is estimated using simplified structure with two adjacent junctions [8]. However, until now it is under discussion how to choose a set of FLR spacing which avoids large potential drop. In actual devices FLR potential is determined by the coupling capacitance among all FLR and substrate. It is not easy to realize an expected potential distribution especially in thin drift layer condition. In this paper, we investigate FLR optimization methodology using process and device simulator, HyENEXSS [9], considering capacitance coupling.

II. SIMULATION STRUCTURE

When leakage current can be neglected, FLR potential is determined by coupling capacitance, which is inversely proportional to depletion layer width in rough approximation. Therefore coupling capacitance network about FLR and substrate can be illustrated as fig. 1 (a). Each FLR potential is expressed by equation (1),

$$V_i = \frac{C_{i-1}V_{i-1} + C_i V_{i+1} + Cs_i V_{dd}}{C_{i-1} + C_i + Cs_i} \qquad (1)$$

where C_i is capacitance between the ith and the $(i+1)$th FLR, Cs_i is capacitance between the ith FLR and substrate, V_i is the ith FLR potential and V_{dd} is drain voltage, respectively. Equation (1) means that the first and the second capacitances from the main junction C_0 and C_1 for thin drift layer devices should be large value not to be dragged by V_{dd}, since Cs_1 is relatively large due to depletion layer width limitation. Accordingly, narrow spacing is needed in the area next to the main junction. It is also important to set the outmost FLR spacing in taking account Cs_n, where n is the number of FLR, which increases because of its large junction area. If C_{n-1} is not enough large, V_n becomes high due to coupling with V_{dd}, and consequently difference between V_{n-1} becomes too large. Furthermore, considering coupling capacitance indicates that FLR spacing should be wider towards outer peripheral side. Figure 1 (b) ~ (e) show the simulation structures. Each of them has high resistance n-epi layer on n-type low resistance substrate connected to drain, and p-type FLR formed by boron ion implantation with patterning mask and high temperature drive-in process. Typical n-epi layer thickness is 40 μm. To analyze spacing dependence of breakdown voltage and potential variation originated with substrate bias in area (1) in fig. 1 (a), structures (b) and (c) are employed. Structure (d) for area (2) is almost same as (b), but the junction width is wide enough to avoid overestimation of electric field concentration by junction curvature effect. Structure (b) with n-epi layer 100 μm thick is also simulated to confirm effect of drift layer thickness. Phenomena in the outmost FLR, area (3), are focused in structure (e). Note that spacing includes depletion layer width in p-type region.

III. AVALANCHE BREAKDOWN SIMULATION

(1) Area next to the main junction

As shown in [8], there is a peak value in the FLR spacing dependence of breakdown voltage in the area next to the main junction. At narrower spacing than that gives maximum breakdown voltage, the surface has breakdown point, because depletion layer width becomes narrow and electric field increases. On the other hand, longer spacing makes the
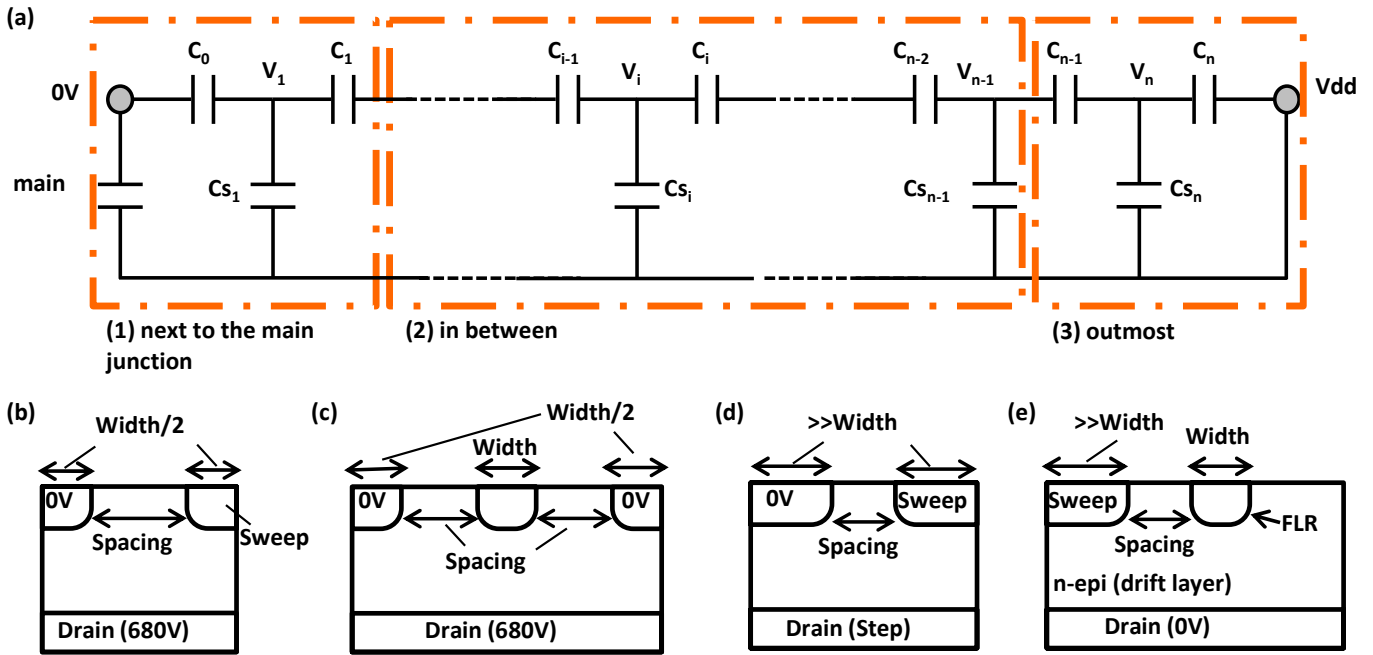
Fig. 1: (a) Schematic of FLR capacitance network and (b) ~ (e) simulation structures. Width = 6 µm in (b) and (c), width = 1 µm in (d) and (e), respectively.
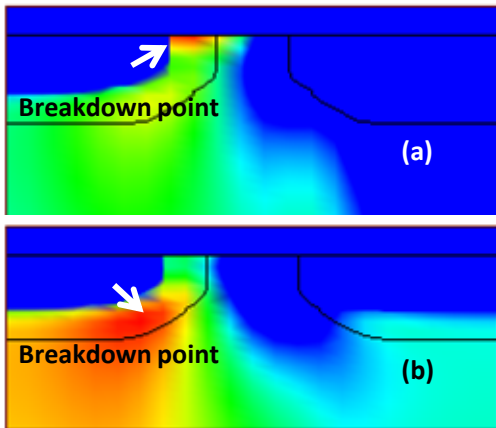

Fig. 2: Impact ionization rate distribution at breakdown voltage; (a) spacing = 3.5 µm and (b) spacing = 4.5 µm.
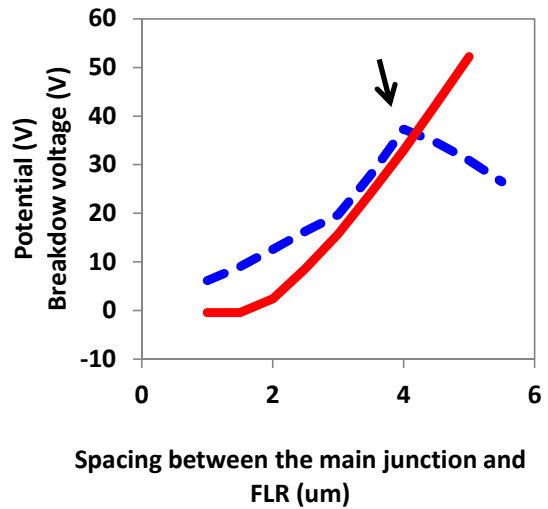

Fig. 3: Spacing dependence of floating FLR potential (solid) and breakdown voltage as same as fig. 2 (dashed).

potential at FLR spacing higher, and results in concentration of electric field and breakdown at junction bottom (fig. 2). FLR is an electrical floating region and potential of FLR is strongly affected with drain bias in device with thin drift layer. FLR couples with neighboring FLR and low resistance substrate with capacitance. The spacing change causes the coupling balance modification and FLR potential variation as shown in fig. 3, which is fig. 1 (c) simulation result. The potential of FLR next to the main junction should be lower than the breakdown voltage between neighboring FLR. The optimal spacing is the value when the breakdown voltage is the maximum in this case.

(2) FLR in between

Figures 4 and 5 show simulation results in structure (d), the drain voltage dependence of maximum breakdown voltage and spacing at that time. When drain voltage is under 300 V, the breakdown voltage and FLR spacing is almost the same without dependence on the drift layer thickness. In lager drain bias, breakdown voltage and FLR spacing in thin drift layer are lower than those in thick drift layer. The depletion layer cannot widen beyond the drift epi layer thickness. In device with thick drift layer, breakdown voltage is closer to 85 V which is gotten from the maximum depletion layer width determined by impurity profile. When a critical electric field is defined as "breakdown voltage / spacing", it varies with drain voltage and has a peak at 400 V in thin drift layer (fig. 6). It indicates that substrate voltage promotes lateral expansion of depletion layer
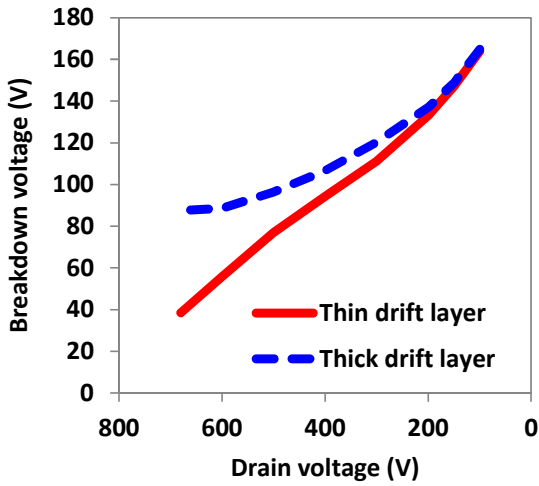
Fig. 4: Drain voltage dependence of maximum breakdown voltage in fig. 1 (d) of thin drift layer (solid) and thick drift layer (dashed).
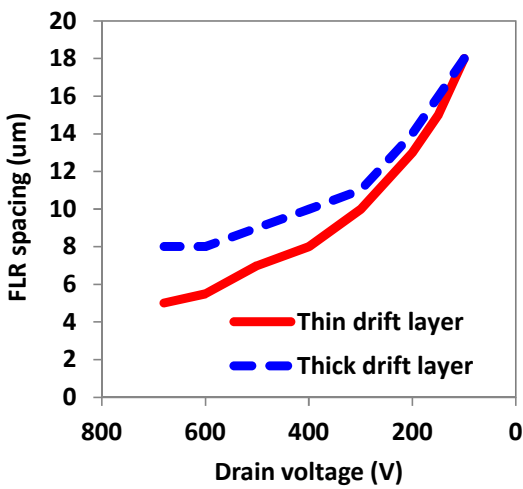

Fig. 5: Drain voltage dependence of FLR spacing when breakdown voltage is the maximum in fig. 1 (d), thin drift layer (solid) and thick drift layer (dashed).
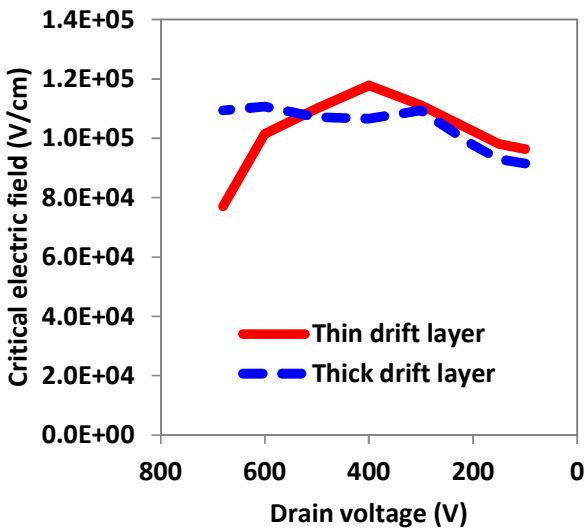

Fig. 6: Drain voltage dependence of critical electric field which defined by "breakdown voltage / spacing".

and the narrower spacing is suitable, when drain voltage is smaller than 400 V. For higher drain voltage, critical electric field decreases in thin drift layer, but it is almost same value in thick one.

(3) Outmost FLR

In the outmost area, spacing dependence of breakdown voltage has a peak value at 7 μm (fig. 7). With longer spacing, the depletion layer gets thinner rapidly and the breakdown point changes from outside of the outmost FLR to inner one, by the reason of too small coupling capacitance between these FLR (fig. 8).
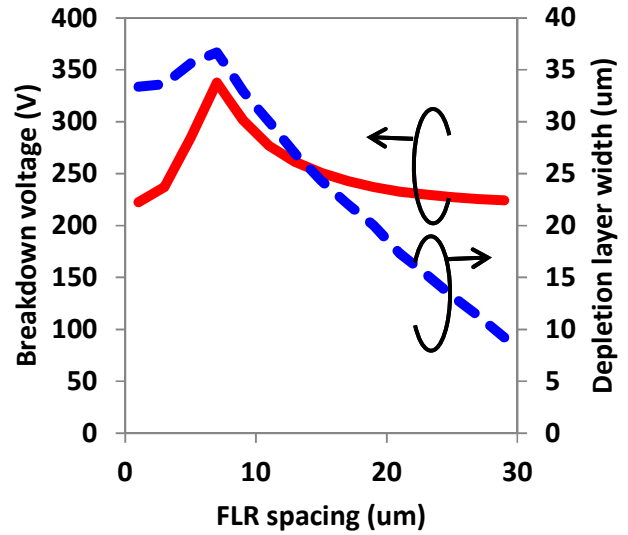

Fig. 7: FLR spacing dependence of breakdown voltage (solid) and width of depletion layer formed outside of the outmost FLR (dashed) in fig. 1 (e).
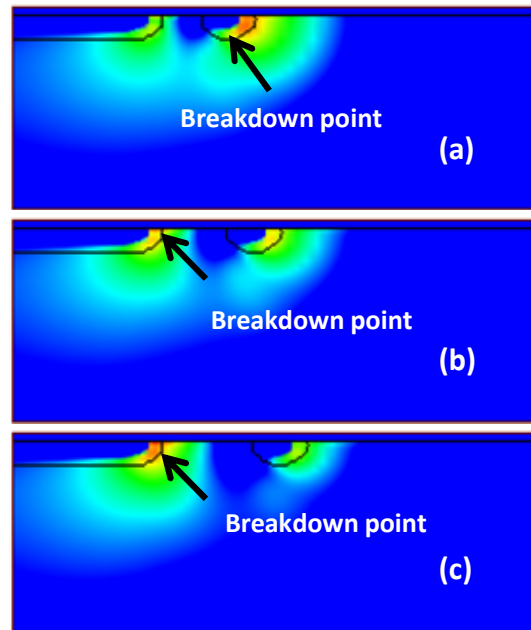

Fig. 8: Impact ionization rate distribution; (a) spacing = 5 μm; (b) spacing = 7 μm, (c) spacing = 9 μm.

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IV. BREAKDOWN VOLTAGE EVALUATION OF TEST STRUCTURE

We evaluate the blocking voltage of the edge termination area designed based on the above results in two 600 V class processes which drive-in time and temperature are different. Although the geometries of these FLR are quite different (fig. 9), we succeed to obtain the target blocking voltage in both processes (fig. 10). The potential difference between neighboring FLR divided by spacing, "local average electric field", against FLR potential is plotted in fig. 11. The breakdown point is the second from the outmost where its "local average electric field" is almost same as the critical electric field. It means that FLR spacing needs to be arranged so that the "local average electric field" is less than the critical one.

Our optimization strategy includes the influence not only between neighboring FLR but also from drain bias, by considering the capacitance coupling among FLR each other and substrate. Thus, the strategy is universally useful in device with any thickness of drift layer and with any process of forming FLR.

V. CONCLUSION

We investigate edge termination breakdown physics related to FLR spacing with simplified structures. Edge termination area is assumed to consist of three areas which are the FLR next to the main junction, the outmost and other. The simulations in these areas clarify the influence of drain voltage on the FLR potential in the FLR next to the main junction and the breakdown voltage between neighboring FLR. As a result, guidelines to choose FLR spacing are pointed out. Finally it is proven that the test structures designed along the guidelines successfully obtain the target blocking voltage.

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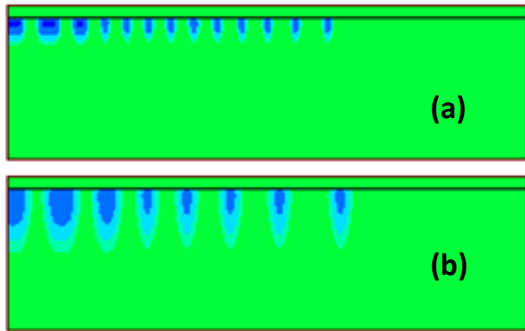[9] T. Wada and N. Kotani, IEICE Trans. Electron., E82-C, pp. 839-847, 1999.

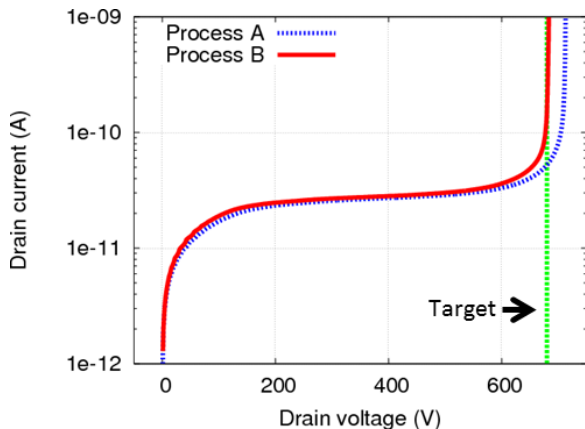Fig. 9: Doping profiles of designed FLR structure; (a) process A, (b) process B.

Fig. 10: Blocking characteristics of the designed FLR structures, process A (dashed) and process B (solid).
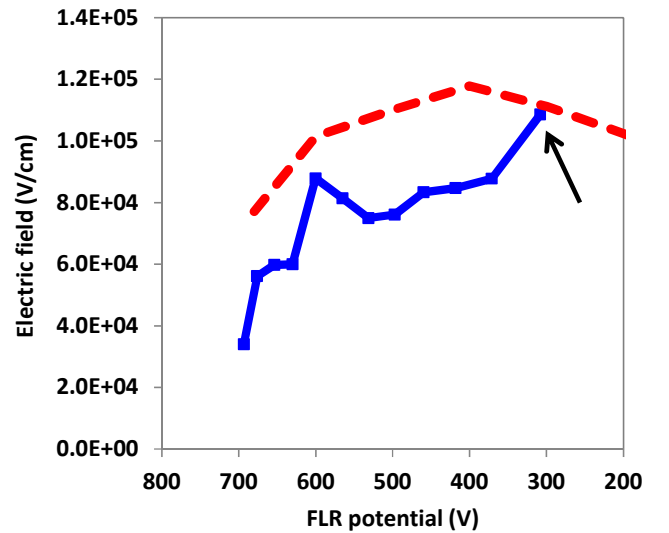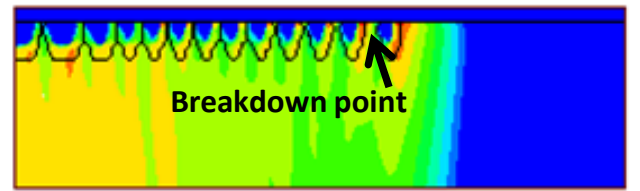

Fig. 11: Impact ionization rate distribution (top). "Local electric field" defined by "potential difference between neighboring FLR / spacing" against FLR potential (bottom).