A Novel Duality-based Modeling Methodology for Reverse Current-voltage Characteristics of SiC

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***Abstract*— This paper presents a novel methodology to design a compact but precise SPICE (Simulation Program with Integrated Circuit Emphasis) model which reproduces complete current-voltage (I-V) characteristics of Silicon Carbide (SiC) power devices. The methodology is based on duality relation between one function for the forward I-V characteristics and its inverse function for the reverse I-V characteristics. The simulated and the measured results of static characteristics of DioMOS (Diode integrated SiC MOSFET) have proved that the reverse I-V characteristics are reproduced by the inverse function of the forward I-V characteristics. Moreover, universal applicability of the proposed methodology is proved by other commercially supplied SiC power devices as well.**

Keywords—SiC MOSFET; channel diode; body diode; SPICE model; reverse currennt-voltage characteristics

I. INTRODUCTION

In design of power electronics applications, SPICE simulators play an important role to estimate their performance before prototyping [1]. Precise device models for the power devices contribute to the reliability of the simulated results. So far, the forward and the reverse I-V characteristics of the conventional power devices including internal diodes have been individually modeled by MOSFET and diode since the reverse I-V characteristics do not show the gate bias dependency [2, 3]. As for recent SiC MOSFETs, the forward voltage (V_f) of the common internal inverse diode is more than 2.5 V due to SiC pn junction. External anti-parallel diodes are always connected to decrease the conduction loss. Therefore, the internal diode model has not been focused in the simulation of SiC power circuits [4].

DioMOS is, however, a new concept power SiC MOS device with a unipolar channel diode integrated [5, 6]. The low V_f of the integrated diode contributes to the size, the production cost and the reliability of the inverter system. The reverse I-V characteristics of the DioMOS depend on the gate-source voltage (V_{gs}). At around V_f region, the conventional diode model does not precisely fit to the measured results of the DioMOS.

This paper presents a novel methodology to design a compact but precise model which reproduces the complete I-V characteristics of the SiC power devices. The methodology is based on duality relation between one function for the forward I-V characteristics and its inverse function for the reverse I-V characteristics. The reverse I-V characteristics dependent on the V_{gs} is not limited to the DioMOS. Other commercially supplied SiC power devices which have the vertical structure show the dependency and are reproduced by the proposed models as well.

II. ELECTRICAL PROPERTIES OF DIOMOS

Fig. 1 shows a schematic cross section of the DioMOS in which highly-doped n-type channel is formed underneath the SiO_2 gate dielectric. As a unipolar FET, the DioMOS has the forward I-V characteristics with low on-resistance and high blocking voltage. Fig. 2 shows increasing ratio of the on-resistance of the DioMOS at elevated temperature. It is smaller than that of typical Si MOSFETs.

As a unipolar channel diode, the DioMOS have the reverse I-V characteristics with low voltage drop. When enough reverse drain bias ($V_{ds} < 0$) is applied, electrons can overcome the potential barrier beneath the gate and flow into the source contact region. The flow of the electrons corresponds to the reverse current of the DioMOS. Fig. 3 shows the reverse recovery waveforms of the DioMOS. The duration while the reverse current flows is shorter than that of typical Si fast recovery diodes.

The potential barrier beneath the gate is changed by the gate bias. The reverse current characteristics of the DioMOS depend on the gate bias.

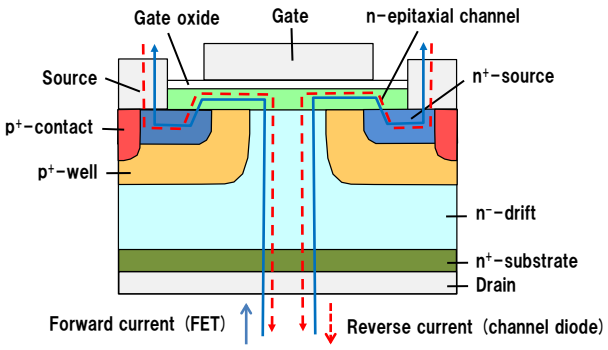

Fig. 1. Cross-sectional view of the DioMOS.

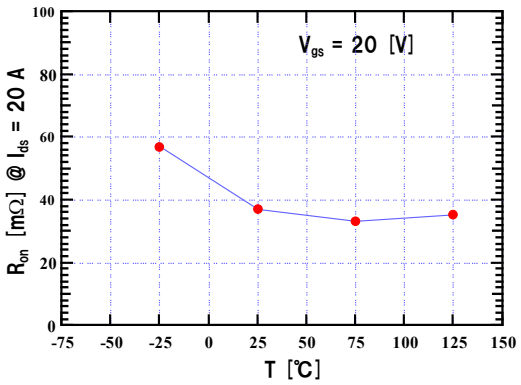

Fig. 2. Measured temperature dependence of the on-resistance of the FET of the DioMOS.

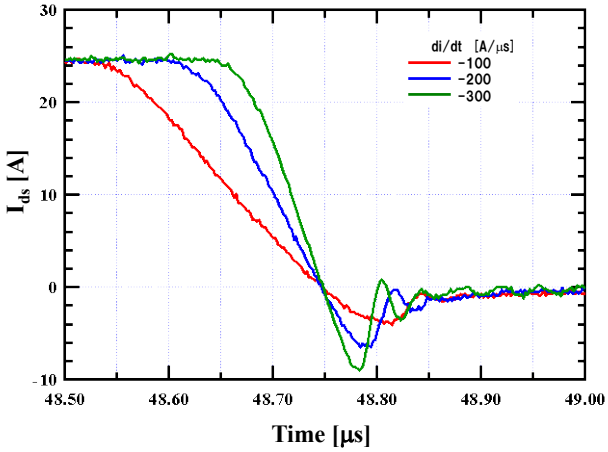

Fig. 3. Measured typical switching waveforms of the channel diode of the DioMOS.

III. Proposed Modeling Methodology

A. *Duality Relation of Forward and Reverse I-V Characteristics*

For estimating the switching loss of the DioMOS power circuits, it is crucial to model the discriminating reverse I-V curves with ease and precision. In the conventional power MOSFET modeling approaches [7-9], the reverse I-V characteristics of the body diode is modeled by the independent

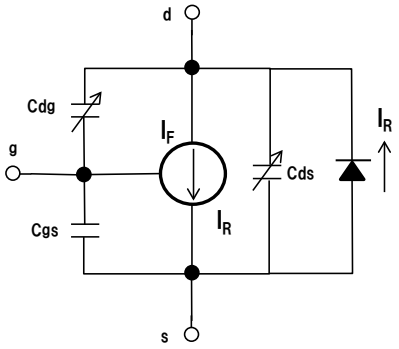

Fig. 4. Conventional equivalent circuit model for power MOSFET.

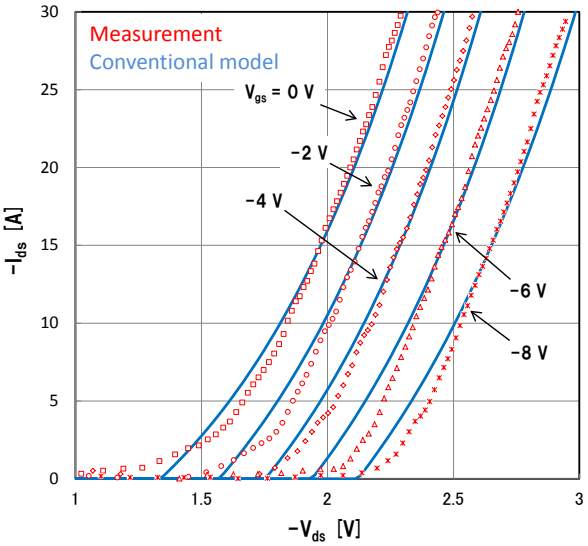

Fig. 5. Comparison of measured reverse I-V curves of the DioMOS and results simulated by the conventional diode model.

diode as shown in Fig. 4. The difference between the simulated and the measured results of the DioMOS around V_f region is large due to the dependency on the gate bias as shown in Fig. 5.

The duality relation between the forward and the reverse I-V characteristics is observed in the measured results of the DioMOS. As an example, Fig. 6 shows the measured I-V curves at V_{gs} = 10 V and at V_{gs} = 15 V. A symmetric relation holds between the solid curve at V_{gs} = 10 V (V_{ds} < 0) and the solid curve at V_{gs} = 15 V (V_{ds} > 0) with a diagonal line. In other words, if a function f is given to satisfy $I_{ds} = f(V_{ds})$ in the forward direction ($V_{ds} > 0$), the duality relation $-\beta V_{ds} = f(-\alpha I_{ds})$ holds in the reverse direction ($V_{ds} < 0$) by simply exchanging I_{ds} and V_{ds}. α and β are positive constants for linear scaling, respectively.

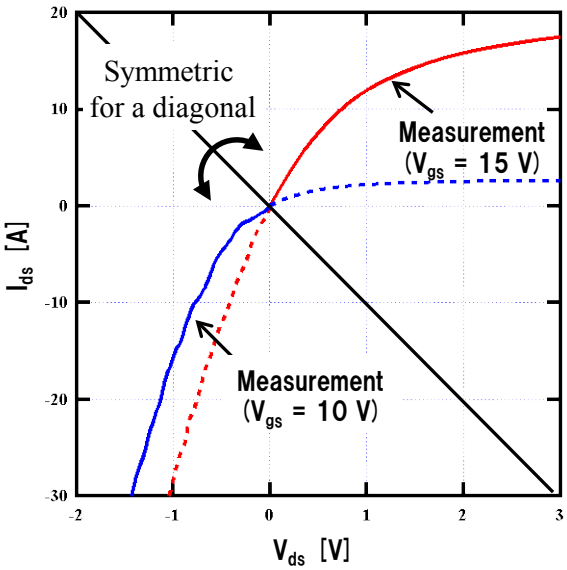

Fig. 6. Measured I-V curves of the DioMOS at Vgs = 10 V and at Vgs = 15 V.

B. *Proposed Model for DioMOS*

The proposed model for the DioMOS is the equivalent circuit as shown in Fig. 7. One voltage controlled current source defined by the following two functions reproduce the reverse I-V characteristics.

$$I_{ds}=\begin{cases}\dfrac{A_f V_{ds}}{1+B_f V_{ds}}(1+C_f V_{ds}) & (V_{ds}>0) \quad (1)\\ A_r\left\{V_{ds}+B_r-\sqrt{(V_{ds}+B_r)^2-C_r V_{ds}}\right\} & (V_{ds}<0) \quad (2)\end{cases}$$

Eq. (1) reproduces the forward current. Eq. (2) for the reverse current is given by the inverse function of Eq. (1). A_f, B_f, C_f, A_r, B_r, and C_r are parameters which depend on V_{gs} and temperature.

In detail, by exchanging V_{ds} and I_{ds} in Eq. (1), the second degree equation of I_{ds} is derived as Eq. (3).

$$A_f C_f I_{ds}^2-(B_f V_{ds}-A_f)I_{ds}-V_{ds}=0 \quad (3)$$

By solving Eq. (3) for I_{ds} in $I_{ds}<0$, the function form of Eq. (2) is derived as follows.

$$I_{ds}=\frac{B_f}{2A_f C_f}\left\{\left(V_{ds}-\frac{A_f}{B_f}\right)-\sqrt{\left(V_{ds}-\frac{A_f}{B_f}\right)^2+\frac{4A_f C_f}{B_f^2}V_{ds}}\right\} \quad (4)$$

Eq. (2) is finally derived by replacing the terms in Eq. (4) with $A_r=\frac{B_f}{2A_f C_f}$, $B_r=-\frac{A_f}{B_f}$, and $C_r=-\frac{4A_f C_f}{B_f^2}$. Since the duality relation does not hold on the same V_{gs}, algebraic calculation of A_r, B_r, and C_r from A_f, B_f, and C_f, fitted to the forward I-V chracteristics is not supported.

By utilizing the duality relation, the only six parameters A_f, B_f, C_f, A_r, B_r, and C_r are enough to reproduce the complete static characteristics of the DioMOS. The gate-drain capacitance (C_{gd}) and the drain-source capacitance (C_{ds}) in Fig. 7 are also determined from the measured capacitance-voltage characteristics as functions of the V_{ds}. Both the static characteristics given by Eqs. (1) and (2), and the dynamic characteristics described by $C_{gd}(V_{ds})$ and $C_{ds}(V_{ds})$ are implemented into one SPICE subcircuit.

IV. Simulation Results

Specification of the DioMOS is described in Tab. 1. With the SPICE model based on the proposed methodology, the forward and the reverse I-V characteristics have been simulated as shown in Fig. 8. In detail, Fig.9 shows the magnified reverse characteristics in log scale. The simulated results have good agreement with the measured results at different operating conditions. In addition, the dynamic characteristics of the DioMOS is reproduced as shown in Fig. 10. The simulated

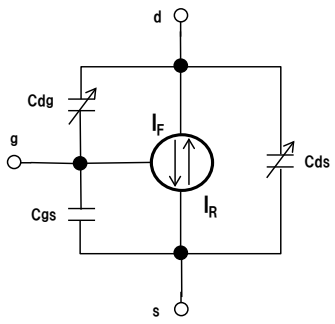

Fig. 7. Equivalent circuit model for the DioMOS.

TABLE I. Specification of the SiC power devices.

	DioMOS	SiC power device (I)	SiC power device(II)
BV_{ds}	1700 V	1200 V	1700 V
I_{max}	25 A	35 A	42 A
R_{on}	40 mΩ	80 mΩ	80 mΩ

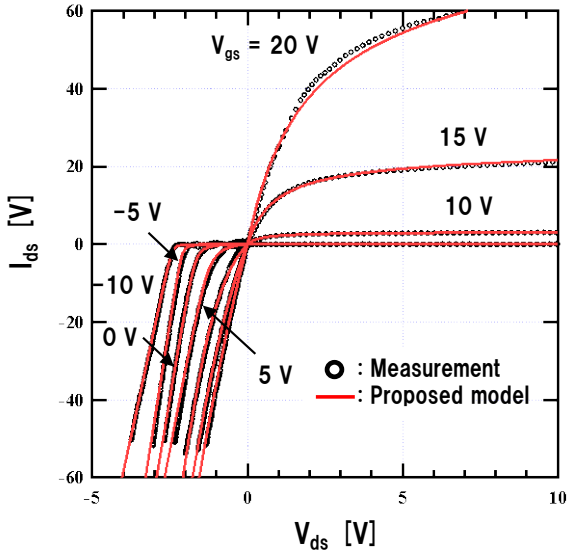

Fig. 8. Comparison of the measured and simulated I-V curves of the DioMOS.

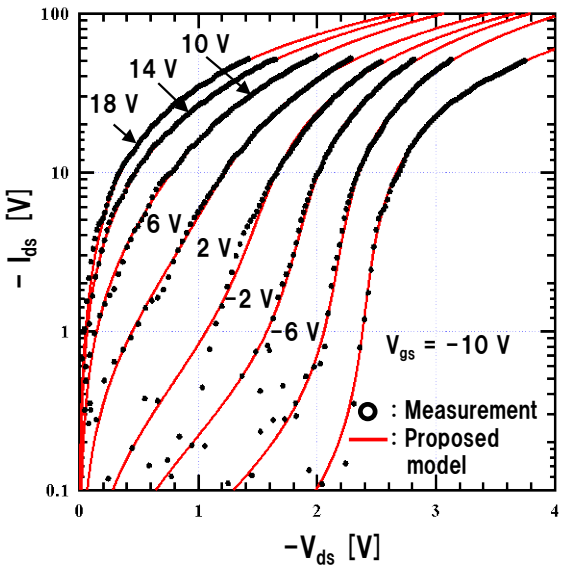

Fig. 9. Comparison of measured and simulated reverse I-V curves of the DioMOS.

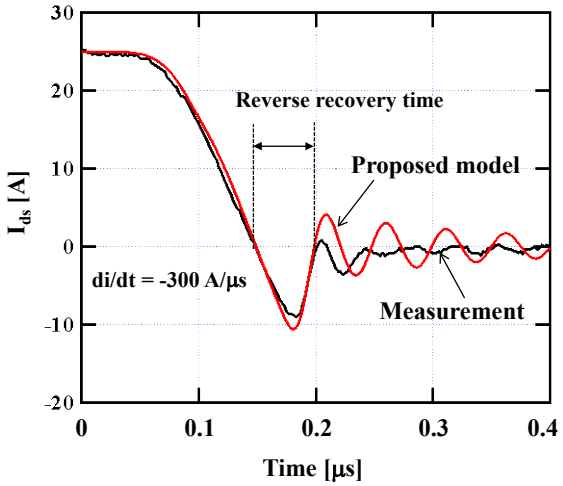

Fig. 10. Comparison of measured and simulated reverse recovery waveforms of the DioMOS.

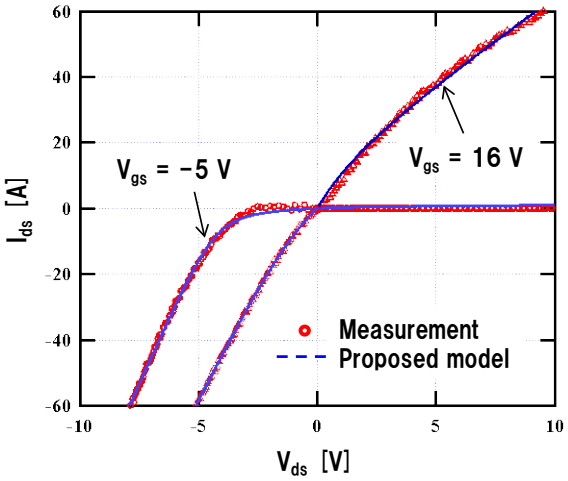

Fig. 12. Comparison of measured and simulated I-V curves of the commercially supplied SiC power device (II).

reverse recovery time which has a close relation to the power loss estimation have good agreement as well. Therefore, it is concluded that Eq. (2) precisely reproduces the characteristics of the channel diode in the DioMOS.

Some commercially supplied SiC power devices have the vertical structure. The proposed methodology is applied as well for the two SiC power devices (I) and (II) in Tab. 1. The simulated I-V characteristics agree with the measured results as shown in Figs. 11 and 12, respectively.

V. Conclusion

By exploiting the duality relation between the forward and the reverse I-V characteristics, a novel modeling methodology to derive a precise but compact SiC SPICE model has been developed for the first time The simulated and the measured results of the static and the dynamic characteristics of the DioMOS have proved that the reverse I-V characteristics are reproduced by the inverse function of the forward I-V characteristics.

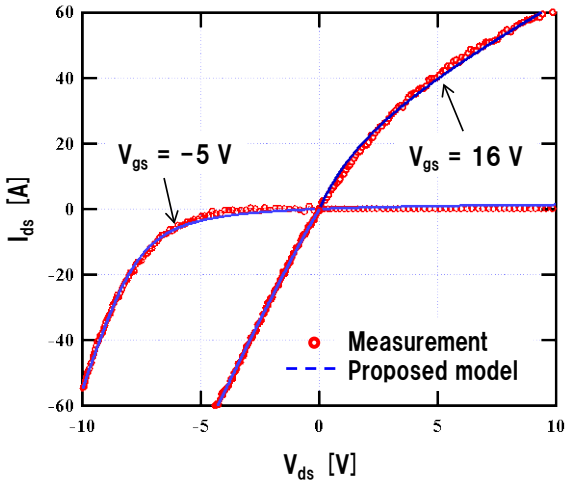

Fig. 11. Comparison of measured and simulated I-V curves of the commercially supplied SiC power device (I).

Universal applicability of the proposed methodology is proved by the two other commercially supplied SiC power devices which have the vertical structure as well.

It is not guaranteed that the qualitative behaviors of the emerging power devices are reproduced by the existing simulation models. The methodology is expected to save a large amount of trials and errors which is required to define the fundamental models to be fitted to the measured results in that case.

References

[1] K. Mizutani et al., "Integrated power design platform based on modeling dynamic behavior of GaN devices," in *IEEE Int. Device Meeting*, Washington, D.C., 2011, pp. 26.4.1-26.4.4.

[2] D. P. Foty, *MOSFET Modeling With SPICE: Principles and Practice.* Prentice Hall, 1996.

[3] R. M. Kielkowski, *Spice: Practical Device Modeling.* Mcgraw-Hill, 1995.

[4] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and Sei-Hyung Ryu, "Silicon Carbide Power MOSFET Modeland Parameter Extraction Sequence," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353-363, Mar. 2007.

[5] M. Uchida et al., "Novel SiC power MOSFET with integrated unipolar internal inverse MOS-channel diode," in *IEEE Int. Device Meeting*, Washington, D.C., 2011, pp. 26.6.1-26.6.4.

[6] A. Ohoka et al., "40mΩ/1700V DioMOS (Diode in SiC MOSFET) for High Power Switching," in *Int. Conf. Silicon Carbide and Related Materials*, Miyazaki, 2013, pp. 911-914.

[7] R. S. Scott and G. A. Franz, "An accurate model for power DMOSFETs including interelectrode capacitances," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 192-198, Apr. 1991.

[8] C. Leonardi, A. Raciti, F. Frisina, and R. Letor, "A new PSpice power MOSFET model with temperature dependent parameters: evaluation of performances and comparison with available models," *32nd Conf. Rec. IEEE IAS Annu. Meeting*, New Orleans, LA, 1997, vol. 2, pp. 1174-1181.

[9] J. Wang et al., "Characterization, Modeling, and Application of 10-kV SiC MOSFET," *IEEE Trans. Electron devices*, vol. 55, no. 8, pp. 1798-1806, Aug. 2008.