Verilog-A Compact Model for Oxide-based Resistive Random Access Memory(RRAM)

Zizhen Jiang[1], Shimeng Yu[2], Yi Wu[3], Jesse H. Engel[1], Ximeng Guan[4], H. –S. Philip Wong[1]

[1]Center for Integrated Systems and Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA,
[2]School of Computing, Informatics and Decision Systems Engineering, Arizona State University, Tempe, AZ 85281, USA,
[3]Oracle America, Inc, CA USA, [4]IBM Research, NY, USA
Email: jiangzz@stanford.edu, shimengy@asu.edu, hspwong@stanford.edu

***Abstract*—We demonstrate a dynamic Verilog-A RRAM compact model capable of simulating real-time DC cycling and pulsed operation device behavior, including random variability that is inherent to RRAM. This paper illustrates the physics and capabilities of the model. The model is verified using different sets of experimental data. The DC/Pulse parameter fitting methodology are illustrated.**

Keywords—RRAM; Compact model; variations; Verilog-A.

I. INTRODUCTION

Metal-oxide based bipolar resistive random access memory (RRAM) is a promising candidate for the future of nonvolatile memory technology [1]. To fulfill the increasing need for high level simulation of emerging memories, several analytical compact analytical models have been developed to describe resistive switching behavior [2][3][4][5][6]. However, these models fail to consider the stochastic aspect of filament switching or were not implemented effectively for circuit simulation. In this paper, we demonstrate a dynamic RRAM compact model using the circuit-compatible Verilog-A language. This RRAM compact model takes into account filament growth fluctuations and variations. The model is verified using both DC switching data and pulse data. Pulse data fitting is found to be more efficient, more representative of the practical usage scenario, and follows more closely the physics of the filament growth.

II. VERILOG-A RRAM COMPACT MODEL

In this model, the complex process of ion and vacancy migration was simplified into the growth of a single dominant filament that preserved the essential switching physics (see Fig. 1) [1] [2] [3]. The size of the tunneling gap (g), which is the distance between the tip of the filament and the opposite electrode, is the primary variable determining device resistance.

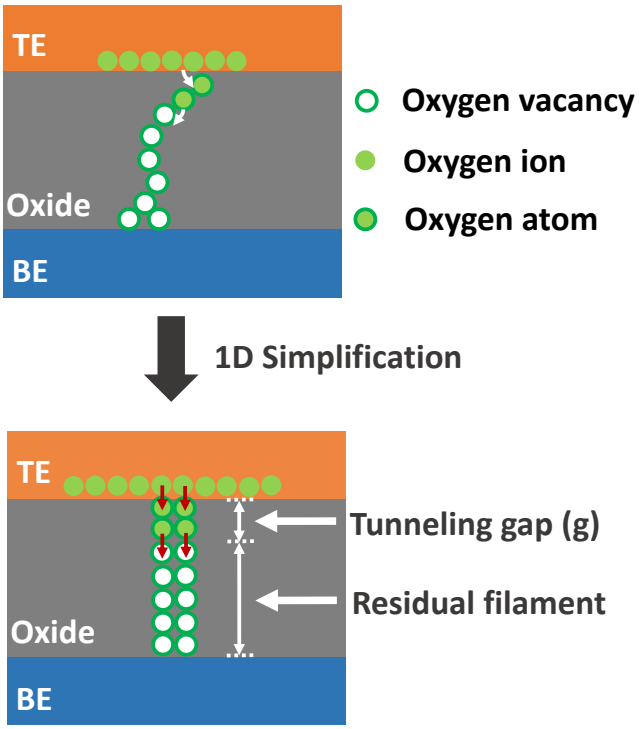

Fig. 1 Conceptual structure simplification for filament growth

RRAM switching dynamics are modeled with a series of related differential and constitutive equations (1-6) [2] [3]. The current conduction is exponentially dependent on the tunneling gap distance, (1). This distance is found by calculating the growth of the gap taking into consideration the electric field, temperature-enhanced oxygen ion migration, (2) (3), and the local temperature due to Joule heating, (4).

$$I = I_0 \times \exp(-\frac{g}{g_0}) \times \sinh(\frac{V}{V_0}) \quad (1)$$

$$\frac{\mathrm{dg}}{\mathrm{dt}} = -v_0 \times \exp\left(-\frac{E_a}{kT}\right) \times \sinh\left(r \times \frac{a_0}{t_{ox}} \times \frac{qV}{kT}\right) \quad (2)$$

$$\gamma = \gamma_0 - \beta \cdot g^3 \quad (3)$$

$$T = T_0 + V \times I \times R_{th} \quad (4)$$

where V is the applied voltage across the cell, I is the current through the cell, g is the average tunneling gap distance, E_a is the activation energy, a_0 is the atomic spacing, t_{ox} is the oxide thickness, q is the elementary charge, k is the Boltzmann constant, T_0 is the room temperature, R_{th} is the equivalent thermal resistance, and I_0, g_0, V_0, v_0, β, γ_0, are fitting parameters.

The use of equivalent thermal resistance in (4) allows us to avoid using the differential equation for the Joule heating temperature used previously in the literature [3]. Currently, differential equations may require implementations outside the Verilog-A program, thereby rendering the Verilog-A program ineffective.

Stochastic and temperature-dependent filament migration (δ_g) is also included in the model (5) (6):

$$\delta_g(T) = \frac{\delta_g^0}{\left\{1+exp\left[\frac{(T_{crit}-T)}{T_{smth}}\right]\right\}} \quad (5)$$

$$g|_{t+\Delta t} = \int \left(\frac{dg}{dt} + \delta_g \times \chi(t)\right) dt \quad (6)$$

where T_{crit} (400–450 K) is a threshold temperature above which significant random variation of the gap size occurs, $\chi(t)$ is a zero-mean Gaussian noise sequence with a root mean square of unity, and δ_0 and T_{smth} (smoothing factor) are fitting coefficients matching the resistance distribution curves to experimental results. The total gap growth as a function of time is shown in (6).

III. Model Verification

Multiple devices are used to verify the model. Here, we illustrate two fitting processes: DC switching fitting and pulse fitting. After setting the fitting parameters in the Verilog-A program to the extracted values, we can apply the program in circuit-level simulation.

A. DC Switching Fitting

The procedure of DC switching fitting is as follows. First, deterministic switching behavior is fitted.

a. Measure a large number (no less than 100) of experimental DC switching cycles from hardware. Pt / HfOx(1.69 nm) / TiOx (4.97 nm) / TiN devices are fabricated and tested for verification.
b. The median I-V curve is used as a representative dataset of the device characteristics. We compared the average (mean) curve and the median curve of 100 DC cycles. The average curve is the sum of currents at the same voltages at the same resistance states. The average I-V switching curve is shown in the blue curve in Fig. 2(a)(b)(d). The median curve is determined from the median currents at the same voltages at the same resistance states, and is shown in the red curve in Fig. 2(a)(b)(d). The transition curve from LRS to HRS of the average curve shown in blue in Fig. 2(b) is unrealistically smooth and is not representative of the experiment. Thereby we extract the model parameter using the median curve.
c. The fitting is performed in MATLAB, where the difference between the median switching curve data and model curve data is minimized.

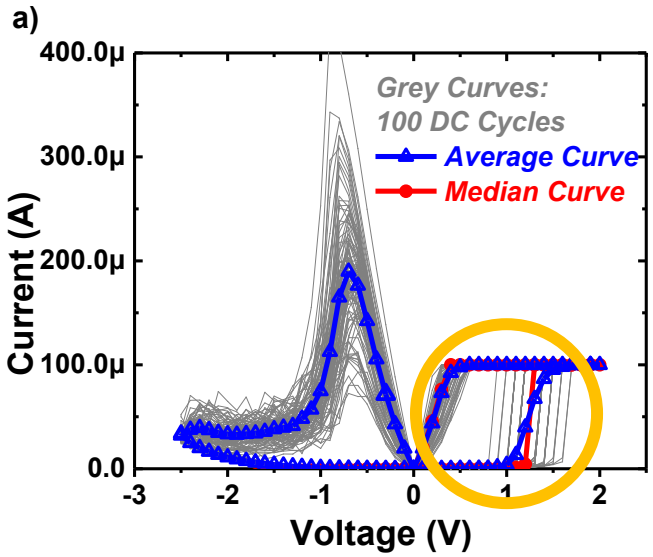

Fig. 2(a) Experimental 100 cycles DC switching curves (grey), average curve (blue) and median curve (red).

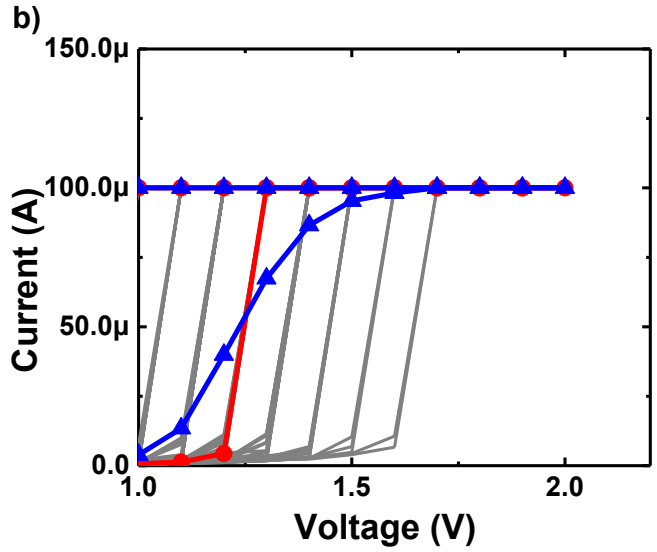

Fig. 2(b) Zoom-in figure for fig. 2(a) SET part.

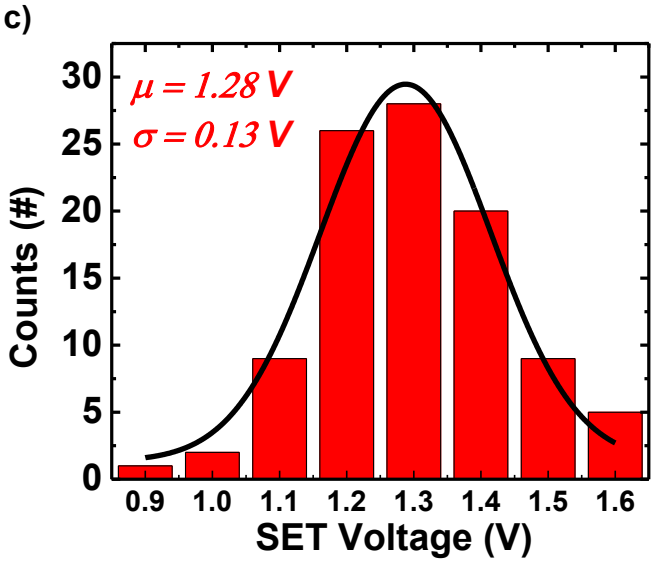

Fig. 2(c) Gaussian distribution of the SET voltages.

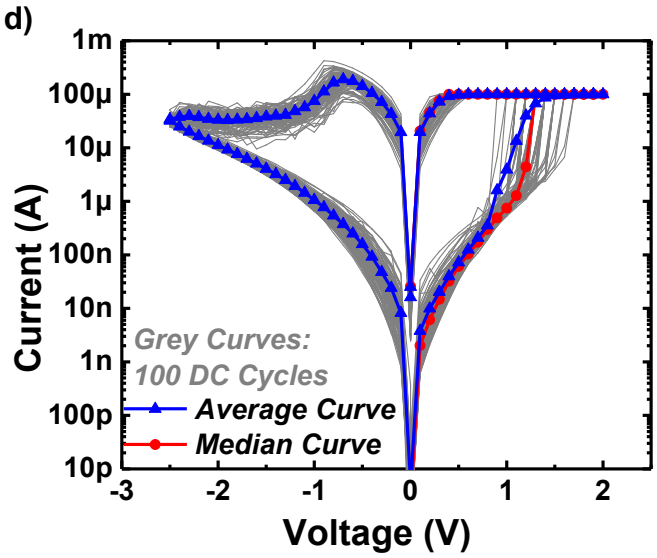

Fig. 2(d) Log scale DC switching curve, same data as in Fig. 2(a).

Variations are added later by tuning the fitting parameters in (5) to match the experimental data. Random DC switching cycles generated by simulation are given in Fig. 3(a).

B. Pulse Fitting

Data for pulse fitting is acquired by applying different pulse amplitudes (Fig. 3(b)) and different pulse widths with various initial resistance values [2]. Pulse fitting is important and necessary for the following reasons,

(1) In a memory system, memory cells are written by a write-and-verify scheme using a series of pulses [7]. Tracking memory system performance is especially important for determining cell disturbance, enabling storage failure recovery, etc.
(2) Filament evolution generally happens on a nanosecond timescale. Accessing RRAM may take less than 10 ns, which requires the modeling of RRAM device behavior on the nanosecond time scale.
(3) Considering the nanosecond time scales of filament formation, simulating the DC switching I-V curve requires ~10^9 calculation per sweep with uniform time steps. For larger time steps, the simulations inaccurately reflect the dynamics of the filament. As observed from experimental data in Fig. 3 (b), resistance tends to saturate after a certain elapsed time. Thus DC fitting may not capture the switching dynamics in the sub-100 nsec regime.

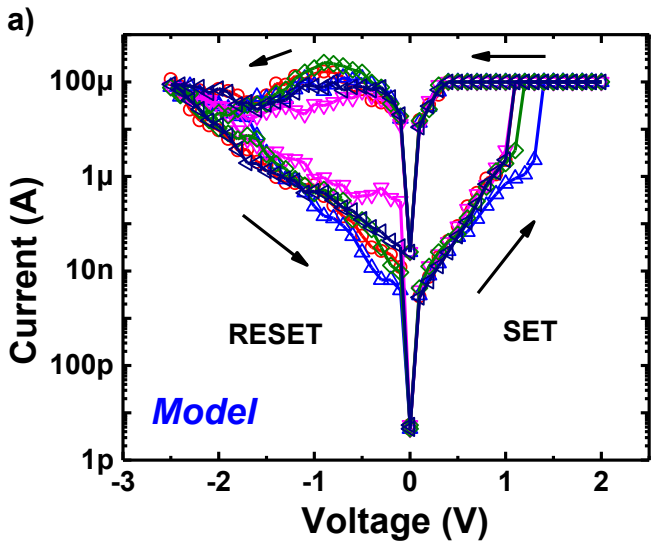

Fig. 3(a) Five DC switching cycles are generated in simulation including gap growth variations δg.

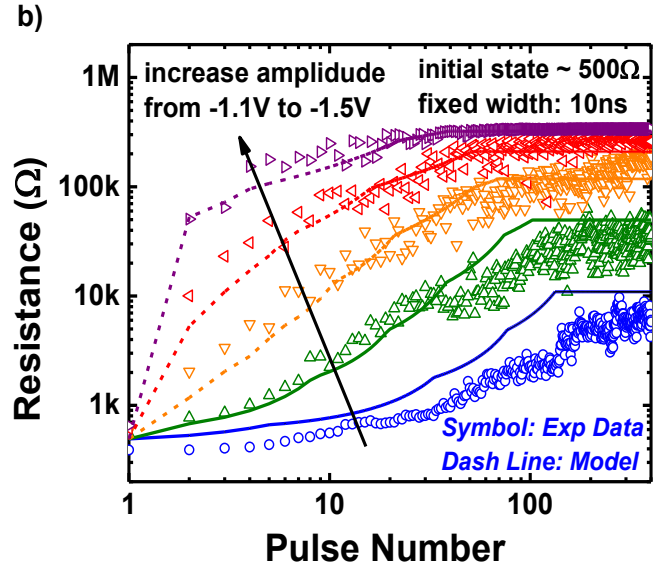

Fig. 3(b) Pulse fitting using data from [2]. Similar results are achieved using Verilog-A.

IV. Conclusion

In this paper, we presented a dynamic RRAM Verilog-A compact model taking into account the filament movement statistical variability. Both DC and pulse measurement evaluations demonstrated the validity of this approach. The procedure to obtain fitting parameters for this model from experiment data is described. Our work highlighted the efficiency and importance of utilizing pulse data for model parameter extraction in order to reflect the physics of the switching behavior in sub-100 nanosecond time scale. This model can be easily employed for circuit level simulation.

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