Accurate Fringe Capacitance Model Considering RSD and Metal Contact for Realistic FinFETs and Circuit Performance Simulation

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***Abstract*—In this paper, analytical gate fringe capacitance model of FinFETs including metal contact and raised source and drain (RSD) are developed. Each cross capacitance models are derived using conformal mapping and field integration. The proposed models are verified with a three-dimensional field solver, Raphael. By including the additional fringe capacitance from RSD and metal contact in BSIM-CMG platform, realistic transition frequency (f_T) and propagation delay of 9-stage ring oscillators are predicted and compared with those predicted by default BSIM-CMG capacitance models.**

Keywords*—*Analytical model, BSIM-CMG, contact, FinFETs, fringe capacitance, parasitic, transition frequency.

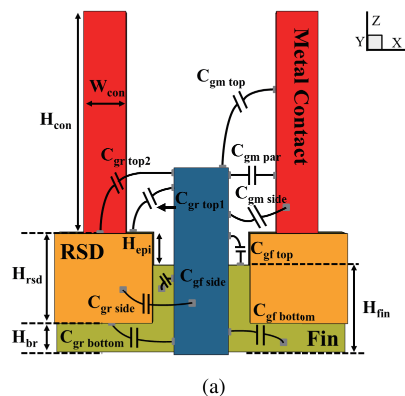
I. Introduction

Recently, FinFETs are considered to be a promising device because of their high immunity to short-channel effects compared with traditional MOSFET. As FinFETs scale down, the thickness of fin (roughly 10 nm nowadays) is getting thinner, which causes increasing source/drain resistance and reduces device current and gain. As a result, FinFETs is fabricated with raised source and drain (RSD) regions using selective epitaxial growth (SEG) process [1]. In addition to that, the massive contact size and short length of interconnect causes increase in the distance between contacts. They result in increase in outer fringe capacitance between the gate metal and other nodes like SEG structure source/drain, fins and metal contacts [2].

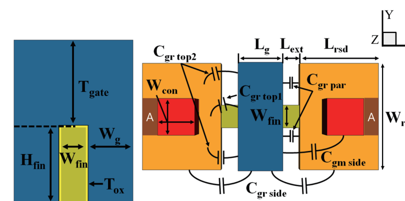
In this paper, we present analytical fringe capacitance model of FinFETs considering RSD structure and metal contact. The proposed model significantly improves the total gate outer fringe capacitance estimation. The outer fringe capacitance is divided into cross coupling capacitance components, and each component model is derived using conformal mapping and field integration. The accuracy of the proposed model is validated using 3D numerical field simulation. The capacitance values obtained from the proposed fringe capacitance models are compared with those predicted from BSIM-CMG [3]. Including the additional fringe capacitance components from RSD and metal contact, the unity gain frequency and ring oscillator propagation delay are estimated for sub-22 nm FinFETs transistor as fin height and spacing to RSD/metal contact vary.

II. Device and simulation method

The BSIM-CMG model of triple gate multi-fin FinFETs with 22 nm gate length is fitted to measured DC characteristics



(a)



(b)

Fig. 1. Modeled FinFET structure. Coupling capacitance components and various geometric parameters used in the model are shown. (a) Side view and (b) cross sectional view (left) and top view (right) of the gate.

of published data of the Intel sub-22 nm process [4], [5], [6]. After fitting the DC data, the proposed analytical fringe capacitance model is implemented using Verilog-A. The simplified structure of FinFETs including RSD and metal contact is shown in Fig. 1.

The input of the 3D static field solver, Raphael [7], is prepared following the dimensions summarized in Table 1. To apply process dependent and physics parameters to the device model cards of compact model, BSIM-CMG, the fabricated device data [8], [9] are used and are calibrated by following pa-

TABLE I. Geometric parameters of FinFETs.

Values	Description	(nm)	Values	Description	(nm)
L_g	Gate length	25.00	T_{gate}	Gate top side height	43.20
W_g	Gate wing length	22.64	L_{ox}	Oxide thickness	1.10
L_{ext}	Fin extension	9.94	H_{fin}	Fin height	39.36
W_{fin}	Fin width	12.99	L_{rsd}	RSD length	44.63
H_{rsd}	RSD height	40.26	W_{rsd}	RSD width	46.27
H_{epi}	EPI height	14.72	H_{con}	Contact height	100.60
W_{con}	Contact width	19.55	H_{br}	Bottomfin height	13.82

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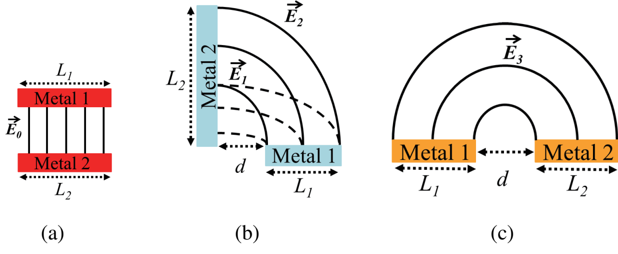


Fig. 2. Geometry-dependent cross capacitance components and cases of their corresponding E-field coupling: (a) parallel, (b) perpendicular, (c) co-planar case.

rameters. Tungsten is adopted as a gate metal, so workfunction parameter PHIG parameter is calibrated to 4.37 eV for N-FET and 4.92 eV for P-FET. The doping profiles are set as follows: source/drain area (NSD) - 1 $\times$ 10^{26} cm^{-3}, source/drain edge (NSDE) - 1 $\times$ 10^{26} cm^{-3}, substrate region (NBODY) - 1 $\times$ 10^{24} cm^{-3}, and channel (NC0SUB) is implanted as a 5 $\times$ 10^{22} cm^{-3}. And length reduction parameter LINT is calibrated to include the dopant diffusion effect. After the calibration, the I-V characteristics of a single device are fitted. For circuit simulation, HSPICE [7] is used.

III. Fringe Capacitance modeling approach

In this work, we model the total outer fringe capacitance as a sum of C_{gf}, C_{gr}, and C_{gm}.

$$C_{gtot} = C_{gf} + C_{gr} + C_{gm} \tag{1}$$

Each component is further divided into cross coupling capacitance components as shown in Fig. 1. C_{gf} is the coupling capacitance from gate to fin, and it models the electric field coupling from each gate plane to fin top, side and bottom ($C_{gf\ side}$, $C_{gf\ top}$, $C_{gf\ bottom}$). C_{gr} is the capacitance from gate-to-RSD region, and it models the electric field coupling from gate to top, bottom and side of RSD ($C_{gr\ top1}$, $C_{gr\ top2}$, $C_{gr\ bottom}$, $C_{gr\ side}$). The existence of metal contact reduces coupling electric field between top and edge of the RSD to gate, so the model needs to carefully include the effect of the metal contact. C_{gm} is the capacitance from gate to metal contact, and it includes the coupling from top and side of the gate to metal contact ($C_{gm\ side}$, $C_{gm\ top}$).

Fig. 2 shows the possible configurations of two metals that define the coupling capacitance. Fig. 2 (a) shows the simple parallel plate capacitance configuration, and $C_{gm\ side}$ and $C_{gr\ side}$ are modeled using this model. For the configurations shown in Fig. 2 (b) and (c), the capacitance can be modeled using conformal mapping [10]. Fig. 2 (b) is the case when two metals are perpendicular to each other and the capacitance can be expressed as (2).

$$\begin{aligned} C_{perpendicular} &= k\frac{\epsilon_{ox}H}{2\pi}\ln\left[\frac{\pi H}{d}\right] + \\ &\frac{\epsilon_{ox}}{2\pi}\ln\left[\frac{d + \eta min(L_1, L_2) + \sqrt{\begin{matrix}(\eta min(L_1, L_2))^2\\ +2\eta min(L_1, L_2)d\end{matrix}}}{d}\right] \end{aligned} \tag{2}$$

where d, L_1, L_2, H, k are the variables that corresponds to the modeled FinFET geometry to calculate fringe capacitance and η and k are the empirical parameters. When conformal mapping is used for fringe capacitance modeling, the general assumption is that the length of fin extension (L_{ext}) is much larger than gate thickness (T_{gate}) [4]. However, this assumption rarely holds in advanced FinFET technologies, because the gate length scales down faster than fin height to achieve high on-current (T_{gate} : 43.20 nm >> L_{ext} : 9.94 nm). In Fig. 2 (b), the conformal mapping models only E_2, additional model that second part of (2) is added. The empirical parameter η is modeled as following.

$$\eta = \exp\left[\frac{L_1 - \sqrt{[L_2]^2 + 2L_2 d}}{L_1} + \gamma\right] \tag{3}$$

The empirical parameter η is used to reduce the length mismatch between two metals and γ is used to decrease error for variation of metal length. Fig. 2 (c) is the case when they are in the same plane, which is called coplanar, which is derived as the following.

$$\begin{aligned} C_{coplanar} &= \frac{\epsilon_{ox}}{2\pi}\times \\ &\ln\left[1 + 2\delta\frac{\sqrt{(L_1 + 0.5L_2)(L_1 + d)L_1 0.5L_2}}{(d + L_1 + 0.5L_2)d}\right] \end{aligned} \tag{4}$$

Equation (4) is used to calculate $C_{gr\ side}$, and L_1, L_2 and correspond to L_{rsd}, L_g and L_{ext} respectively. Table 2 summarizes the coupling capacitance terms that construct C_{gf}, C_{gr}, and C_{gm}, and the variables (d, L_1, L_2, H, k) for the fringe capacitance equation (2), (3), and (4). Extra coefficients are defined in Table 2 to simplify the expressions; $A= L_{ext} + L_{rsd}$, $B= 0.5(L_{rsd} - H_{br})$, $C= 0.5(F_{pitch} - H_{br})$, $D= H_{con} - (H_g - H_{epi} - H_{fin})$, $E= H_{con} - D$, $F= H_g - H_{br} - H_{rsd}$.

TABLE II. THE CROSS COUPLING CAPACITANCE MODELS AND ITS GEOMETRIC PARAMETERS.

C_{fringe}	d	L_1	L_2	H	k
$C_{gf\ side}$	T_{ox}	W_g	L_{ext}	H_{fin} - H_{br}	4.82
$C_{gf\ top}$	T_{ox}	T_{gate}	L_{ext}	T_{fin}	6.23
$C_{gf\ bottom}$	T_{ox}	W_g	A	H_{br}	5.54
$C_{gr\ top1}$	L_{ext}	C	F	W_{con}	0
$C_{gr\ top2}$	L_{ext}	L_{rsd}	E	W_{rsd} - W_{con}	0
$C_{gr\ bottom}$	L_{ext}	H_{br}	L_{rsd}	W_{rsd} - W_{fin}	0
$C_{gm\ side}$	L_{ext} + B	C	W_{con}	E	0
$C_{gm\ top}$	L_{ext} + B	$0.5L_g$	D	W_{con}	2.92

IV. Model validation

The accuracy of the proposed model is validated through 3D Raphael simulation. Fig. 3 (a) shows verification of total gate fringe capacitance by sweeping L_{ext} for different H_{fin} (29.36 nm, 39.36 nm, and 49.36 nm). Fig. 3 (b) shows the validation results of C_{of}; C_{gf}, C_{gr}, and C_{gm} models. Fig. 3 (c) and (d) shows the validation results of top and side components of C_{gm} and C_{gr}. The proposed model matches the 3D Raphael simulation results well. In BSIM-CMG, the gate-to-RSD capacitance model only includes the $C_{gr\ par}$, $C_{gr\ side}$ for cross capacitance components. In the gate-to-RSD model proposed in this work includes electric field coupling component from the top plane of gate metal to the top plane of the RSD, which are $C_{gr\ top1}$ and $C_{gr\ top2}$ shown in Fig. 1 (b). The coupling capacitance value of gate top plane to the top plane of the RSD is a function of the W_{rsd} and H_{rsd}. After applying top plane components of RSD, the summation of C_{gf} and C_{gr} shows higher capacitance compared with BSIM-CMG in Fig. 4 (a) and (b). Coupling between metal contact and gate consides to consider effect of metal contact structure and is modeled as a function of W_{con}. C_{gr} + C_{gf} is compared

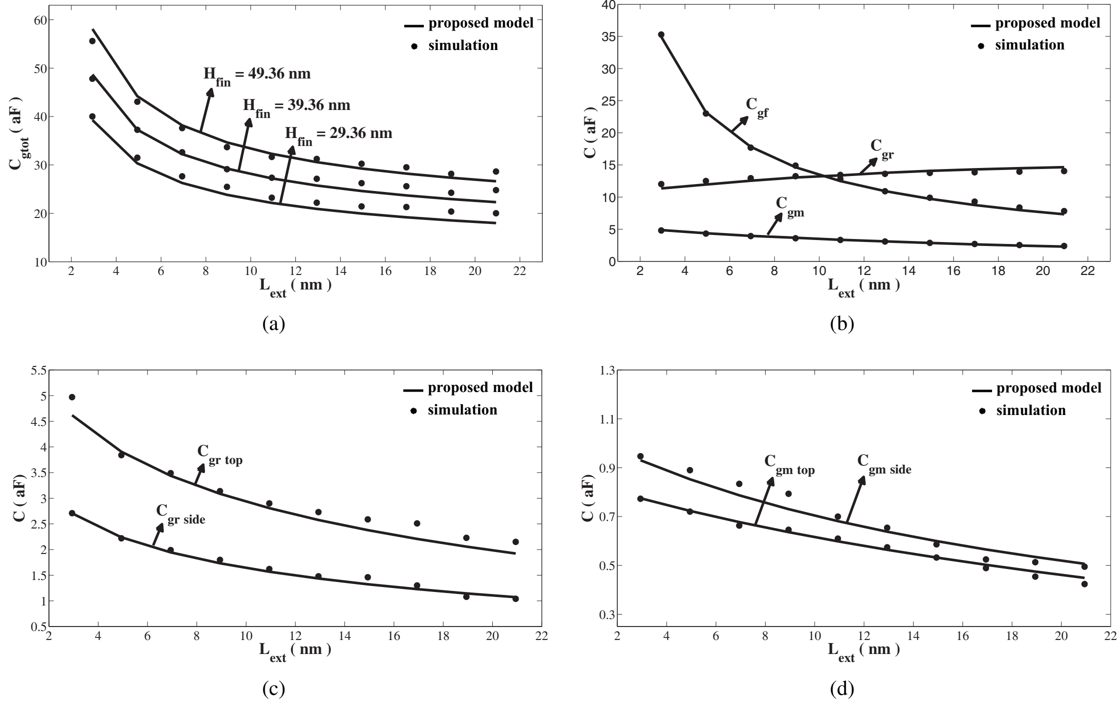


Fig. 3. Proposed model accuracy validation compared to Raphael 3D simulation. (a) Total gate fringe capacitance, (b) cross components C_{gf}, C_{gr}, C_{gm}, (c) C_{gr}, and (d) C_{gm} for L_{ext} variation.

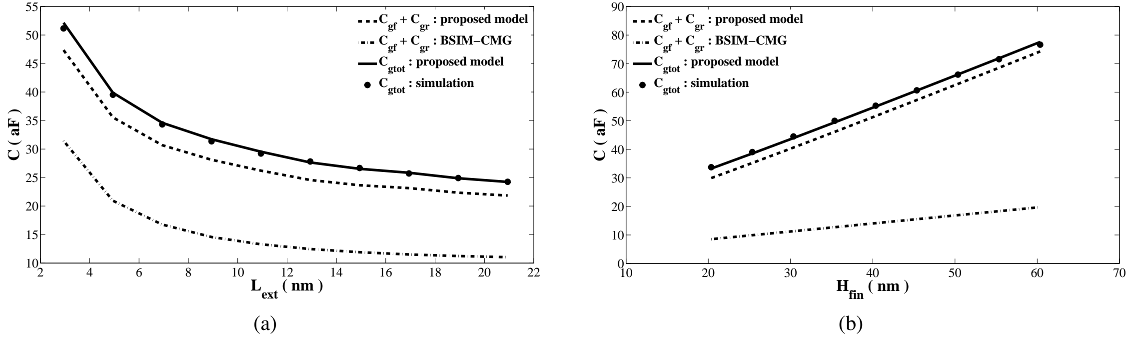


Fig. 4. Comparison of C_{gr} + C_{gf} changes between the proposed model and BSIM-CMG. (a) L_{ext} and (b) H_{fin}.

between proposed model and BSIM-CMG, and the proposed model shows better accuracy compared to 3D simulation data. Fig. 5 (a) shows the trends of cross capacitance portion for H_{fin} variation after adding C_{gm}. Each cross capacitance components are normalized to total capacitance C_{of} as H_{fin} variation. C_{gm} accounts for approximately one tenth of the total gate fringe capacitance. The contribution of C_{gm} gradually increases, when H_{fin} and L_{ext} scale down further.

Fig. 5 also shows H_{fin} variation has stronger influence on C_{gr} than C_{gf}. Below reference fin height of 39.36 nm, the amount of the gate-to-RSD capacitance is dominant. In Fig. 5 (b), default BSIM-CMG fringe capacitance model shows constant C_{gr} over C_{gf} ratio, but the proposed model captures the dependence of H_{fin} variation. As the device length scales, the distance between gate and RSD structure will become smaller, so the impact of C_{gr} will impact the circuit performance further.

V. Circuit Performance Simulation

Transition frequency (f_T) is considered as a performance indicator of high frequency device. The proposed fringe capacitance model is implemented using Verilog-A in BSIM-CMG to estimate the transition frequency of single device. The BSIM-CMG predictions of transition frequencies based on the default fringe capacitance model the proposed fringe capacitance model are compared in Fig. 6. For geometric parameter H_{fin} and L_{ext} variation, BSIM-CMG default model predicts the transition frequencies around 20 % more optimistic than those predicted by the proposed model.

Fig. 7 (a) shows the schematic of an inverter and 9-stage inverter based ring oscillator. DC fitted NFET and PFET compose the basic inverter. The impact of outer fringe capacitance on the ring oscillator characteristics are simulated using HSPICE circuit simulator. Fig. 7 shows the performance comparison of 9-stage ring oscillator. Transient simulation is performed and rise-fall delay and propagation delay are measured. The propagation delay from first inverter output signal to last signal is shown in Fig. 7 (c). $t_{p\ BSIM}$ is the propagation delay estimated using the BSIM-CMG default capacitance model and $t_{p\ model}$ is that from the model developed in this work. Fig. 7 (d) shows the propagation delay change as L_{ext}

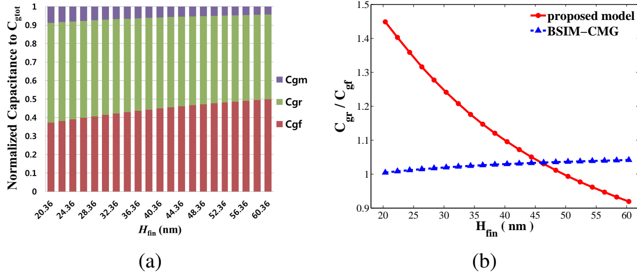
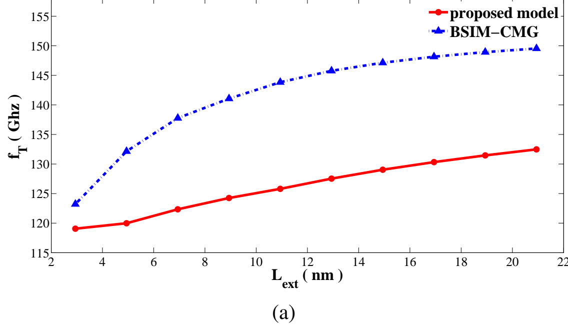


Fig. 5. Contribution comparison of C_{gr} and C_{gf}. (a) Cross capacitance components are normalized to total capacitance and (b) comparison ratio of cross capacitance C_{gr} to C_{gf} between proposed model (•) and default model in BSIM-CMG(▲).



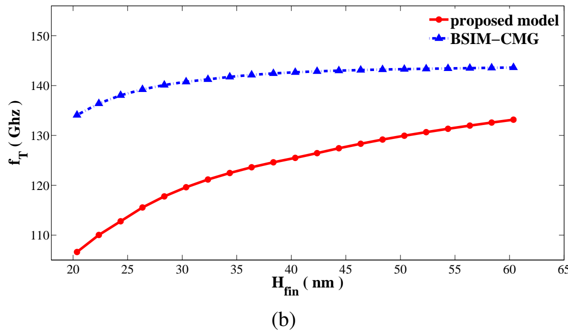


Fig. 6. Comparison of f_T predicted using the proposed gate fringe capacitance model (•) and default model in BSIM-CMG(▲). (a) L_{ext} variation and (b) H_{fin} variation.

(distance from gate to RSD) changes. The propagation delay based on the proposed model is higher than that based on the default BSIM-CMG fringe capacitance model.

VI. Conclusion

The three-dimensional gate-to-RSD and gate-to-contact fringe capacitance for sub-22 nm FinFETs is developed. Each coupling capacitance term is divided into two-dimensional components, and each component is derived by the conformal mapping and field integration. The accuracy of the proposed model is verified with three-dimensional field solver, Raphael. The maximum average error of total fringe capacitance is less than 1 %. The trend of cross capacitance shows that C_{gr} is dominant compared to C_{gf} when technical node scaling continues. The transition frequency (f_T) is predicted and the proposed model shows 20 % more pessimistic estimation compared to that of the default model in BSIM-CMG. The 9-stage ring oscillator performance based on FinFETs is estimated including the realistic capacitance models proposed in this

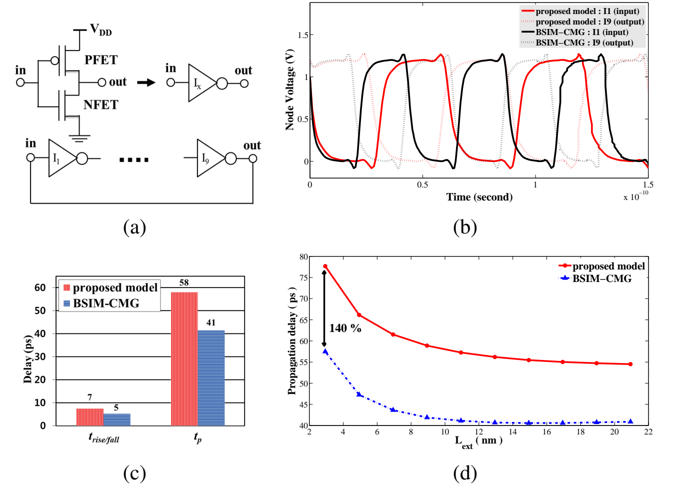


Fig. 7. 9-stage ring oscillator schematic and simulation results. (a) Simulated output waveform, (b) comparison of 9-stage ring oscillator delay, (c) propagation delay comparison between two models for various L_{ext}.

work. And proposed model predicts ring oscillator propagation delay 1.4 times higher than that estimated from BSIM-CMG.

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