USJ engineering impacts on FinFETs and RDF investigation using full 3D Process/Device simulation

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***Abstract*— The impacts of FinFET channel and extension S/D region implantations on relevant device parameters such as electrostatic control and Vth mismatch (MM) are investigated. We used 3D TCAD process and device simulations to gain physical understanding and to optimize the performance/variability of bulk-FinFETs. For the first time, the full FinFET process flow simulation was performed using diffusion, activation and segregation models identical to those used in planar nodes. In this work a wide range of implantation and anneal splits is used to demonstrate the 3D simulation accuracy. After achieving good agreement with experiments in terms of Vth and Ion/Ioff, considering lateral dopant diffusion and activation, the simulation was used to investigate SRAM random doping fluctuation RDF.**

Keywords—Predictive TCAD; variability; simulation; FinFET;

I. INTRODUCTION

Tri-gate devices, like Finfet, are now widely used for 14nm nodes and below. FinFET [1] process flow can re-use many integration steps from planar CMOS, while providing better electrostatic integrity relative to planar FETs, owing to tighter control of the channel potential by multiple gates wrapped around the body. This translates to excellent SCE, low-leakage, and high performance devices. In order to perform timing analysis for multigate devices accurately and determine the most efficient knobs for optimization, it is essential to model and capture the dopants physical behavior accurately. This paper presents a full 3D FinFET process modeling, re-using TCAD knowledge gained from 1D/2D planar nodes. The impacts of the channel and extension source/drain (S/D) implantations/annealing on relevant device characteristics such as electrostatic control and Vth mismatch (MM) are addressed at device geometries relevant to 14nm technology.

II. DEVICE PREPARATION AND TCAD MODELLING

A. Device Preperation

Fig. 1 highlights the major steps of the "gate-last" [2-3] process for bulk FinFETs, which involves fin definition, STI, and high-k dielectric formation, followed by poly gate and spacer formation. Next, S/D selective epitaxial growth is performed, followed by poly gate removal and metal gate deposition, and, finally, the contact vias are formed. These experiments were carried out on a state of the art 14nm-node [4]. A raised S/D is used for N and P-type. In addition, the P-type incorporates an eSiGe as stressor for the channel [5]. Implants wise, devices receive a triple-well implant scheme. The channel profile was determined so as to achieve higher drive current as well as lower punch-through current. Halo/extension implants were especially used. After S/D implant, appropriate thermal budget for dopants diffusion and activation was utilized.

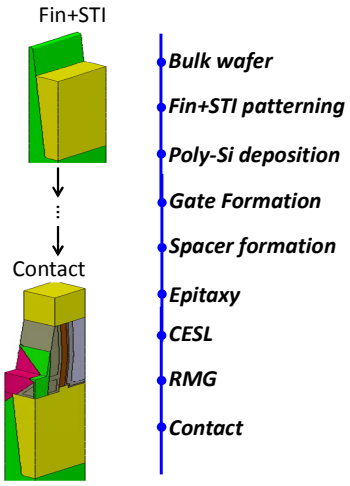

Fig. 1. Bulk FinFET "gate-last" process simulation steps based on process flow.

Fig. 2 shows simplified process flow focusing on dopants implantation and annealing sequences. Furthermore, the amount of splits used and presented in this work is marked.

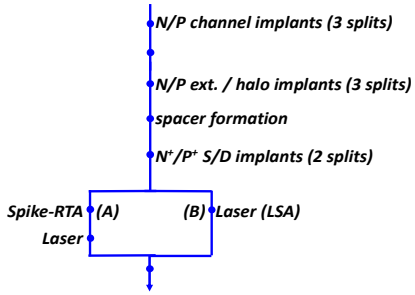

Fig. 2. well, ext./halo and S/D implantation splits and laser annealing sequence studied in this work.

B. TCAD Modelling

Throughout this work, a TCAD suite including process and device simulation capabilities has been used. A 3D device structure has been first built based on Transmission electron microscopy (TEM) images, which then allows to realistically simulate the fabrication process flow including dopant implantation and annealing conditions. For 3D simulation modelling, we used all the methodologies developed for 1D/2D [6, 7] calibration. In fact the dopants diffusion/activation, defects evolution, segregation, and Transient Enhanced Diffusion models as well as the co-implant models (Carbon, Fluorine, Nitrogen) [8] are directly copied from the 2D TCAD decks. The dopant diffusion is described by a 3-stream drift-diffusion model and its activation by a transient precipitation model where the equilibrium precipitate concentration is reached when the active doping concentration is equal to the solubility. Advanced dopant implantation models, such as Monte Carlo, are used in order to generate ultra shallow junction profiles and account for the point defect generation and damage accumulation. However, the trapping and co-activation models were adapted for FinFET where the interface phenomena become pre-dominant and where the S/D doping concentration is very high compared to previous nodes. In order to model the experiments results obtained after the investigated splits (Fig. 2), a 3D process simulation is performed to generate bulk N and P-type FinFET structures (Fig. 3).

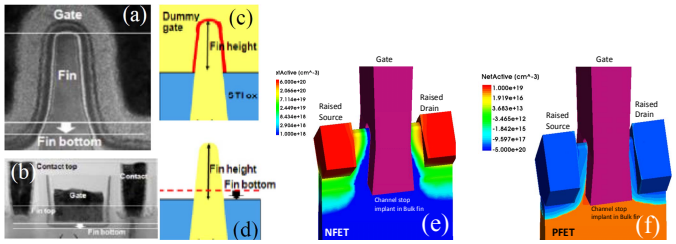

Fig. 3. XTEM images (a) across fin and (b) across gate. x-section acrossfin (c) before dummy gate removal and (d) after dummy gate removal [9]. (e) N and (f) P-type Bulk FinFETs simulated structures.

For the device simulation, the channel stress and doping profile generated with full 3D process [10] simulations are integrated in 3D device [11] simulator to match the IV characteristics from long to short channels. Indeed, in this work continuum device simulation has been performed using the drift-diffusion (DD) equation. The quantum confinement in the channel is accounted using the density gradient (DG) model, and the stress effect on the holes mobility is derived from the 6x6 k.p theory [12]. For low field mobility, Lombardi model is used [13] with orientation dependency, while the high filed mobility model uses the Caughey-Thomas formula [14]. The DD model remains valid for the simulation of deep-submicron MOS devices due to the limited effect of the velocity overshoot in silicon. Similar to planar devices, Silicon Tri-gate transistor shows much lower mobility than bulk silicon because of surface roughness scattering as Vg increases. This leads to reduced none-equilibrium transport. The ballistic transport for transistor with gate length of 25nm is not dominant. The probability of none-scattering event in the channel drops below 50% for 25nm gate length silicon transistor. For 35nm gate length device this probability is lower than 30% [15]. The mobility parameters are calibrated for matching the long channel transfer characteristics and the saturation velocity adjustment is used to match the saturation current. The contact resistance is calibrated based on measured data and extracted contact area from the cross-sectional TEM.

III. Experimental and Simulation Results and Discussion

To demonstrate the capabilities of TCAD simulation, Fig. 4 reports a comparison of simulated and SIMS profiles for N-type and P-type FinFETs dopants Arsenic/Phosphorus (As/P) and Boron (B), respectively. SIMS boron profiles at the SiGe S/D region (the germanium content is plotted on the graph). Indeed, it has been observed that the SiGe barrier layers are effective in reducing the B redistribution during the spike anneal [16]. The SIMS profiles in Fig. 4. The simulated boron profile reported in Fig. 4 is in a good agreement with measurements (all curves are normalized with respect to the peak value of boron SIMS). The activation, segregation, and transient enhanced diffusion (TED) models were successfully applied to simulate diffusion and activation of boron during the annealing steps. In particular, the Ge content effect on boron diffusion is well reproduced which allows to correctly simulate the junction depth. For the N-type, Spike temperature scaling is

used to perform shallower S/D junctions, which combined to laser anneal gives higher dopant activation. The good agreement with measurements demonstrates that, As/P dopants co-implantation is well captured for both anneal sequences LSA alone and RTA+LSA.

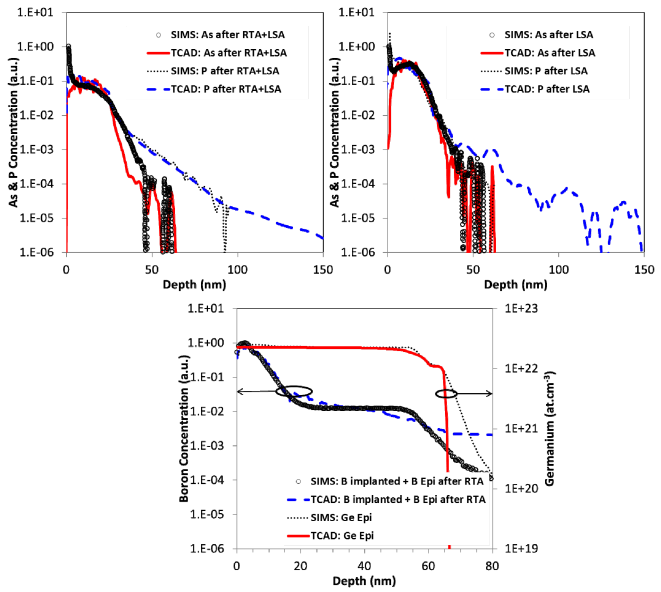

Fig. 4. Comparison of S/D As/Phosphorus co-implantation profiles for RTA+LSA vs LSA for N-type and implanted Boron + Boron Epi profiles after spike-RTA for P-type. Ge content is shown on the right axes. Good agreement is achieved between TCAD and SIMS.

To investigate the bulk FinFET electrostatic control and Vth mismatch, ultr-shalow junction (USJ) engineering with less-diffusion/high-activation technique is used. The FinFETs channel doping achieved with different doses allow Vth,sat modulation vs. dose and vs. Lg as shown in Fig. 5.

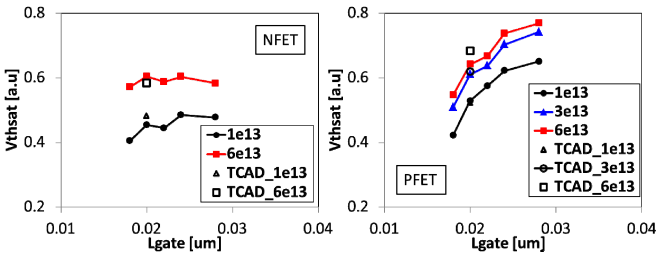

Fig. 5. Vth,sat vs. Lg with various well dose. And Vth,sat vs. B/As dose of NFET/PFET. Vth modulation is achieved across wide range of Lg and dose. Good agreement between TCAD (short Lg) and experiments.

RTA temperatures scaling is necessary for shallow S/D formation. Indeed, Fig. 6 shows the Vth roll-off plots for RTA+Laser (LSA) vs. LSA only. When LSA is used, a slight improvement on SCE and an increase in Vth are observed. The Ion characteristic is degraded due to a Ron increase (not shown). The simulation results of the FinFET N and P-type devices are also reported in Fig. 6.

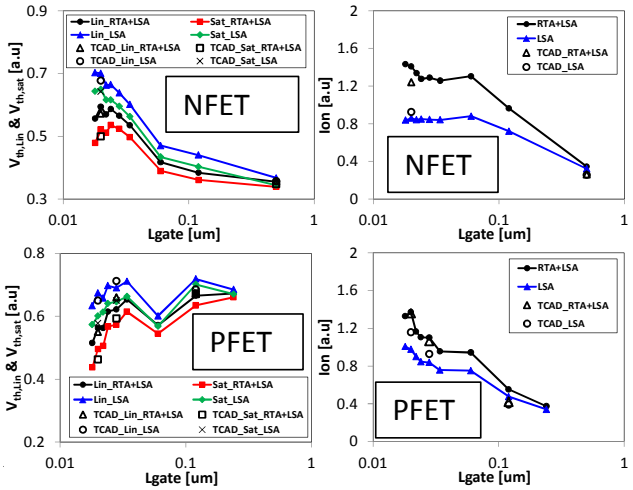

Fig. 6. N-type and P-type bulk FinFET Vth roll-off and Idon characteristic vs. Lg. TCAD simulations (only long and short devices are reported) well reproduce the measurements especially RTA+LSA vs. LSA. For N-FinFET, Arsenic and Phosphorus co-activation and diffusion is accounted for, and for P-FinFET Boron diffusion account for SiGe effect at S/D region.

The achieved good agreements in terms of Vth roll-off characteristics and Ion for long and short devices show that lateral S/D diffusion is well reproduced by simulation. Indeed, Fig. 7 reports the junction profiles of the S/D extensions in the channel side resulting from different USJ anneals. This figure shows a reduced lateral diffusion for LSA compared to RTA+LSA.

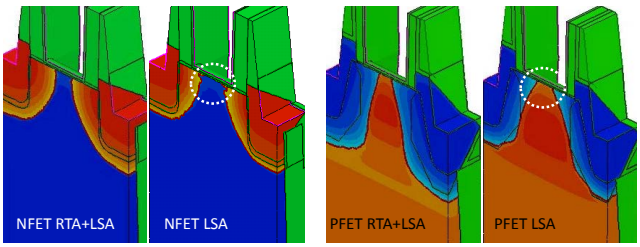

Fig. 7. Net doping variation for RTA+LSA vs. LSA for N and P-type bulk FinFETs. Lower junctions overlap is achieved with LSA only.

Fig. 8 shows additionally the TCAD accuracy to capture the doping profiles induced Idon variation vs. a wide range of process conditions including well, extension/halo and S/D implantation splits beside laser annealing sequence. Both NFET and PFET results are reported.

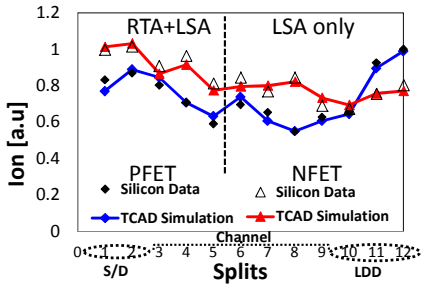

Fig. 8. Ion vs. well, ext./halo and S/D implants splits. The good agreement between TCAD and data demonstrates the accuracy to capture the process variation

Finally, one of the major concerns of adding doping to FinFETs is the expected worsening of device variability due to RDF. The below developed calibration methodology is applied to investigate SRAM Vth MM. A comparison, of the measured and simulated Vth,sat mismatch for different channel implant doses is shown in Fig. 9 for Pull-Down (NFET) and Pull-Up (PFET).

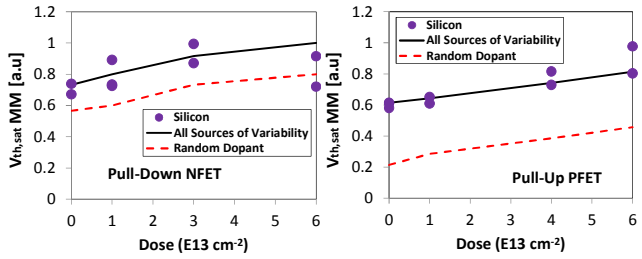

Fig. 9. Vth,sat mismatch vs. different channel implant doses for SRAM Pull-Down and Pull-Up. MGG (metal gate granularity), LER (line edge roughness), RDF, OTF (oxide thickness fluctuation), fin thickness variation are included as mismatch sources. Measured (Silicon curve) Vth,sat MM data is well reproduced by simulation (black line) when all sources of variability are included. Furthermore, TCAD allows to decouple the RDF contribution (red curve) to the total mismatch, and thus further optimization of this component

The 3D simulation allows to assess and quantify the electrical effect of each mismatch source to break down the global mismatch in different contributors (Fig. 10). Based on TCAD, RDF contributed ~25% for PFET and ~60% for NFET of the total variation in doped channel FinFETs.

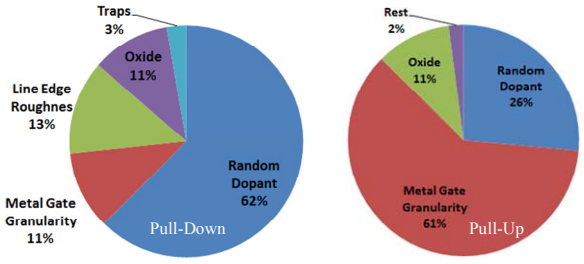

Fig. 10. Pull-Down and Pull-Up mismatch simulation where MGG (metalgategranularity), LER (lineedgeroughness), RDF, OTF (oxidethicknessfluctuation), finthickness variation are included as mismatch sources. Mismatch sources breakdown only possible with the proposed TCAD methodology

IV. Conclusion

An optimized TCAD strategy simulation for full 3D process/device FinFET is presented. After calibration, the resulting 3D doping profiles correctly predict the short-channel behavior of the devices even for Laser annealing only. The calibrated decks are used for FinFET performance optimization and variability improvement.

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