Analysis of Heat Conduction Property in FinFETs Using Phonon Monte Carlo Simulation

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***Abstract*—A phonon transport simulator using a Monte Carlo method is used to analyze the heat conduction properties in FinFET structure. We compare the simulation results to those obtained from the conventional heat conduction equation based on the Fourier's law, and discuss about the discrepancies attributed to ballistic transport effect. We also analyze the impact of additional heat path through gate contact, and show that it has a less significant but non-negligible contribution which could slightly reduce the hot spot temperature.**

I. Introduction

The heat conduction property is one of the main concerns for nanoscale FETs relating to reliability and performance [1][2]. The non-planar structures surrounded by insulating films are preferred to maintain the gate controllability. However, in terms of the thermal property, they are not favorable because there are only narrow paths to conduct the higher density power ($\gg$ 1 TW/cm^3) away from the hot spot created in the drain [3]. So new simulation tools to accurately evaluate the heat conduction phenomena in nanoscale are now strongly required. We have recently developed Monte Carlo (MC) simulator for solving the phonon's Boltzmann transport equation taking account of rigorous physical models [4]. Furthermore, we have utilized this tool to explore heat transport properties not only in nanoscale test structures [5], but also the FinFET devices [6], and discussed the validity or limitations of the conventional Fourier-based approach, where the thermal flux is proportional to the temperature gradient, due to the quasi-ballistic phonon transport effect [7].

In this study, we present in-depth analysis about the heat conduction properties in nanoscale FinFET structure based on the various simulation techniques (MC, a finite element method, and an equivalent thermal circuit model).

II. Monte Carlo Simulation Results

Fig. 1 schematically illustrates the FinFET structure simulated in this study. Bulk FinFET structure with a gate length of 22 nm and a Fin thickness of 8 nm [8] was considered. MC particles were assumed to be confined only inside the Si region, i.e., the perfectly reflecting boundary condition (assuming purely diffuse boundary scattering [4]) was enforced at the Si/insulator interfaces. A heat source with a power density of 7.1 TW/cm^3 mimicking the hot spot (total input power = 34 μW) was placed at the drain edge. In addition, the constant-temperature reservoirs at 300 K were set on the source/drain contacts and below the Si substrate, which act as heat sinks to remove the accumulated heat in the device.

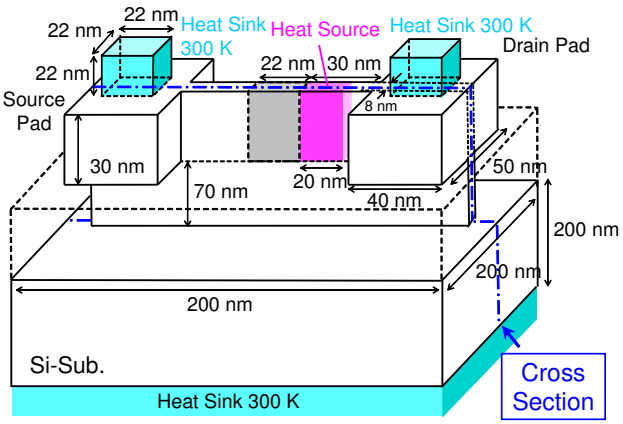

Fig. 1. Schematic view of the FinFET structure simulated in this study. The heat source was placed at the drain edge with a heat density of 7.1 TW/cm^3, and the constant-temperature reservoirs at 300 K were set on the top of the source/drain pads and below the bottom of the Si substrate.

Fig. 2 shows the net dissipated heat in each reservoir calculated by averaging over the simulation time after turning

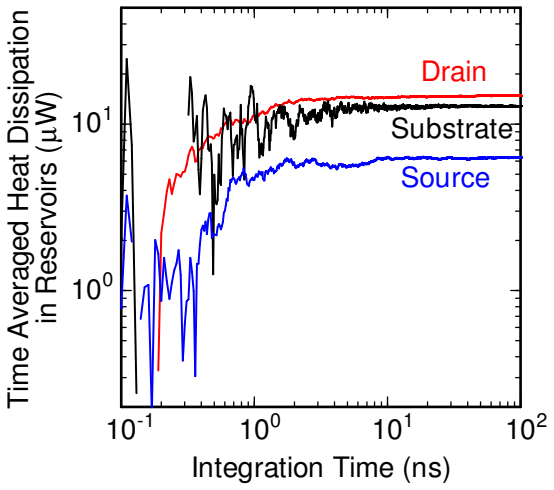

Fig. 2. Time-averaged heat dissipation in reservoirs placed at the source, drain, and substrate contacts. The net removal of MC particles were counted in each reservoir region.

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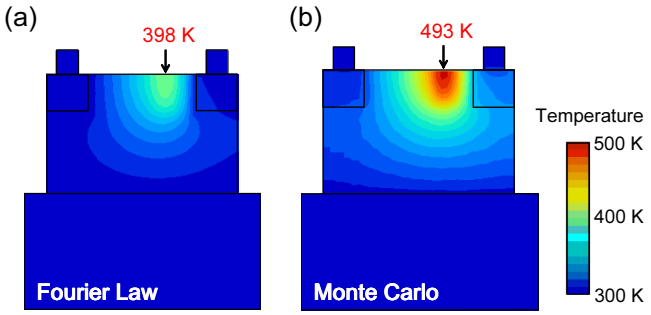

Fig. 3. Steady-state temperature distribution on the vertical cross-section indicated in Fig. 1. The simulation results obtained from (a) the heat conduction equation based on Fourier's law and (b) the present MC method are compared.

on the heat source. The steady state was reached after ~ 10 ns, and the drain and substrate were found to be the main thermal contacts to remove the heat. More details on the physical models and algorithms regarding the phonon MC simulation are described in our previous publications [4][5].

The MC simulation results were compared to those obtained by solving the heat conduction equation based on the Fourier's law. Fig. 3 shows the steady-state temperature distribution; although we calibrated the Fourier-based simulator to yield the same thermal conductivities of bulk Si and infinite Si thinfilms as the MC simulator, significantly different hot spot temperature ($\Delta T \sim 95$ K) was observed between the two methods. On the other hand, as shown in Fig. 4, similar results were obtained for the percentage of the heat flow coming out from each reservoir.

III. Discussion

A. Thermal Circuit Analysis

To understand the mechanisms behind the simulation results, the considerations based on the equivalent thermal circuit model were carried out. As shown in Fig. 5, the thermal paths from the heat source to each reservoir are divided into two resistance components in series, i.e., the inside Fin region ($R_{\rm fin}$) and the residual part ($R_{\rm pad}$ or $R_{\rm sub}$). Then, the magnitudes of thermal resistances were roughly estimated from

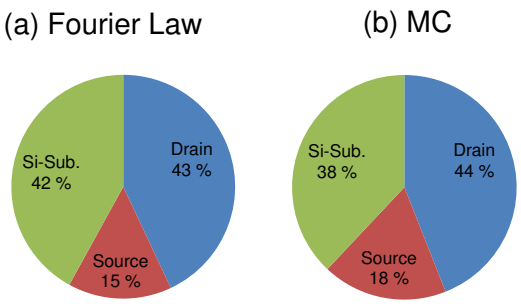

Fig. 4. Percentage of heat flux coming out from Si substrate, drain and source contacts calculated using (a) Fourier law and (b) MC method.

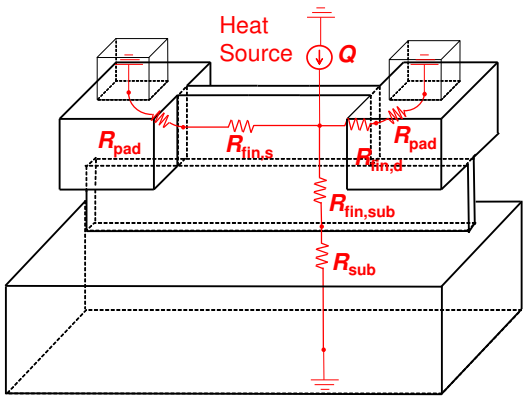

Fig. 5. Equivalent thermal circuit model for the simulated FinFET structure.

$R = \Delta T/Q$, where ΔT is the temperature difference across the heat path and Q is the heat flux. The calculated results are shown in Fig. 6.

MC results exhibit larger thermal resistances compared to the Fourier law particularly in the paths from the Fin exit to the heat sink. This is due to the quasi-ballistic transport effect of phonons, which becomes significant when the system size is comparable or less than the phonon mean free path λ (Fig. 7). Also note that even inside the Fin, the MC results show the larger $R_{\rm fin}$, indicating the quasi-ballistic transport effect. Although λ is considered to be significantly shortened in the Fin due to the frequent phonon boundary scattering, the phonon conduction nature is not fully diffusive in the simulated system assumed in this study.

B. Gate as Additional Heat Path

Finally, a rough estimation is made to assess the contribution of the gate electrode to remove the heat from the hot spot. As mentioned above, the current simulation is neglecting the heat flow though the Si/insulator interfaces due to the poor thermal conductivities of insulating materials and/or the existence of the interfacial thermal resistance [9]. However, the metal gate, which is expected to be a good heat sink, is located

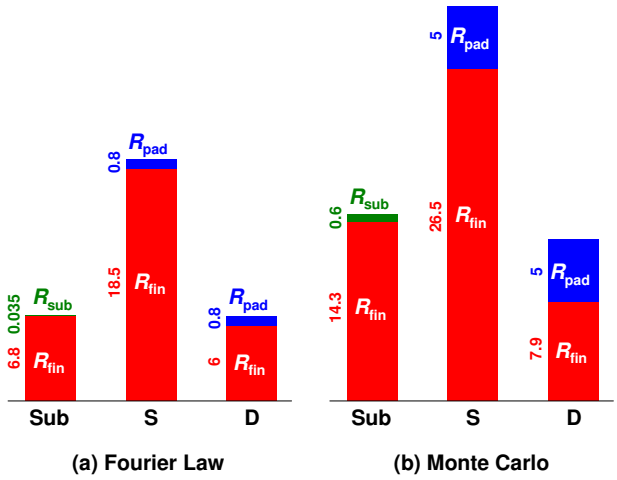

Fig. 6. Magnitudes for the thermal resistances (MK/W) in Fig. 5 evaluated from the simulations using (a) Fourier law and (b) MC method.

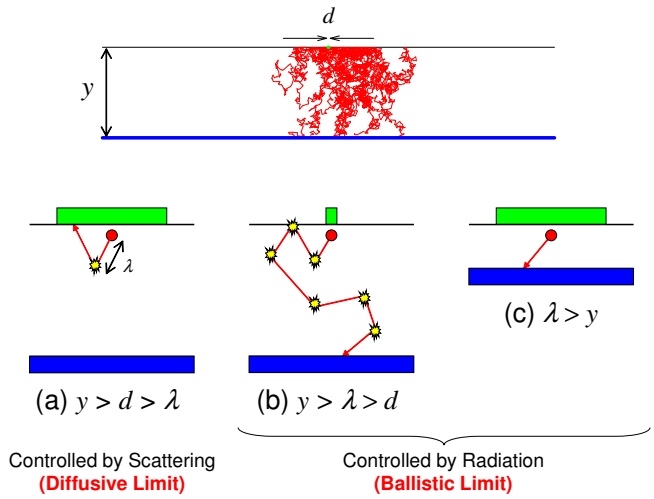

Fig. 7. (Top) Example of the phonon trajectories for simulating the thermal point contact structure. (Bottom) Schematic illustration showing the phonon ballistic transport effect. (a) If $y > d > \lambda$, the phonon emitted from the top contact easily returns back by the scattering. (b) If $\lambda > d$, it has less chance to return and instead is likely to reach the bottom contact. The thermal resistance is then limited by the phonon radiative flux from the top contact. This is also the case for (c) $\lambda > y$.

close to the hot spot, though the gate insulator is inserted across them. So we have estimated the effect of the additional heat path by using the thermal circuit model. As shown in Fig. 8, the resistance from the hot spot to the source edge ($R_{\mathrm{fin,s}}$) was divided beneath the gate, and a new branch was added to conduct the heat to the gate heat sink. The division of $R_{\mathrm{fin,s}}$ was performed by taking account of the distance $L_{\mathrm{fin,s1}}$ between the center points of the gate and the heat source. According to Fig. 9, $L_{\mathrm{fin,s1}}$ is estimated to be 21 nm, while the entire distance $L_{\mathrm{fin,s}}$ covered by $R_{\mathrm{fin,s}}$ is 62 nm. ¿From these values, we can calculate $R_{\mathrm{fin,s1}}$ and $R_{\mathrm{fin,s2}}$ as follows:

$$R_{\mathrm{fin,s1}} = \frac{L_{\mathrm{fin,s1}}}{L_{\mathrm{fin,s}}} \times R_{\mathrm{fin,s}} \ , \quad (1)$$

$$R_{\mathrm{fin,s2}} = \frac{L_{\mathrm{fin,s}} - L_{\mathrm{fin,s1}}}{L_{\mathrm{fin,s}}} \times R_{\mathrm{fin,s}} \ . \quad (2)$$

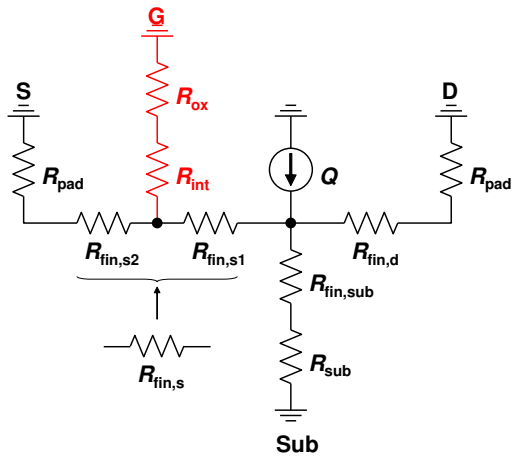

Fig. 8. Equivalent thermal circuit model to estimate the heat dissipation through gate electrode. $R_{\mathrm{fin,s}}$ in Fig. 5 was divided and a new branch was added to conduct the heat to the gate heat sink.

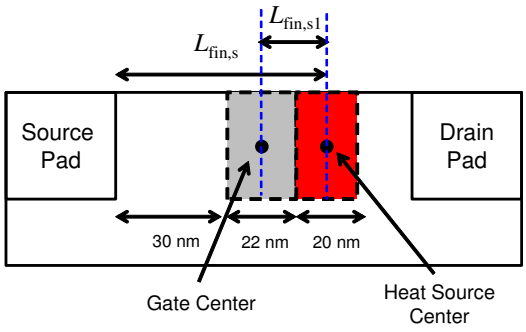

Fig. 9. Schematic cross-sectional view of the simulated FinFET structure along the channel direction.

The additional branch (the red components in Fig. 8) was represented by two resistances in series, i.e., the interfacial resistance $R_{\mathrm{int}} = 13.4$ MK/W and the insulating layer resistance $R_{\mathrm{ox}} = 0.5$ MK/W, where R_{int} was calculated using the parameter for Si/SiO_2 interface (2×10^{-8} $\mathrm{Wm^2K^{-1}}$ [9]) and the gate area of 1.5×10^{-11} $\mathrm{cm^2}$, and R_{ox} was from the thermal conductivity of SiO_2 (1.38 W/mK) assuming the thickness of 1 nm. We then recalculate the maximum temperature using this new circuit with additional gate heat path as shown in Fig. 8. The calculated results are shown in Fig. 10. Since the gate insulator is very thin, itself has a negligible impact, but R_{int} significantly impedes the heat flow. It has been found that the gate has a less significant, but non-negligible contribution, which would reduce the hot spot temperature slightly.

IV. Conclusion

A phonon transport simulator using the Monte Carlo method has been used to calculate the heat conduction properties in the FinFET structure, and the simulated results were analyzed with the help of the equivalent thermal circuit model. The simulated results have been compared to those of the

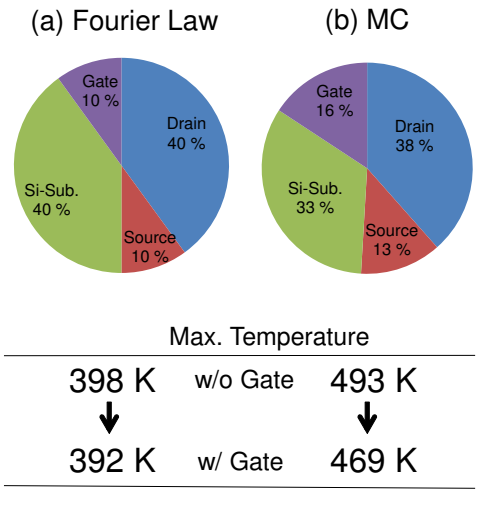

Fig. 10. (Top) Heat flow percentage through the gate electrode, Si substrate, drain, and source contacts, estimated from the model shown in Fig. 8 based on the results of (a) Fourier law and (b) MC method. (Bottom) Change of the hot spot temperature before and after the insertion of the gate heat path.

conventional heat conduction equation based on the Fourier's law, and the discrepancy in the estimated hot spot temperatures was found between the two methods. This observation could be attributed to the quasi-ballistic transport effect of phonons, which is significant mainly in the pad region but also important inside the Fin. We also analyzed the impact of additional heat path through gate contact, and demonstrated that it has a less significant but non-negligible contribution which could slightly reduce the hot spot temperature.

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REFERENCES

[1] C. Prasad, L. Jiang, D. Singh, M. Agostinelli, C. Auth, P. Bai, T. Eiles, J. Hicks, C. Jan, K. Mistry, S. Natarajan, B. Niu, P. Packan, D. Pantuso, I. Post, S. Ramey, A. Schmitz, B. Sell, S. Suthram, J. Thomas, C. Tsai, and P. Vandervoorn, "Self-heat reliability considerations on intel's 22nm tri-gate technology," in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, April 2013, pp. 5D.1.1–5D.1.5.

[2] S. Lee, R. Wachnik, P. Hyde, L. Wagner, J. Johnson, A. Chou, A. Kumar, S. Narasimha, T. Standaert, B. Greene, T. Yamashita, J. Johnson, K. Balakrishnan, H. Bu, S. Springer, G. Freeman, W. Henson, and E. Nowak, "Experimental analysis and modeling of self heating effect in dielectric isolated planar and fin devices," in *VLSI Technology (VLSIT), 2013 Symposium on*, June 2013, pp. T248–T249.

[3] J. Rowlette and K. E. Goodson, "Fully coupled nonequilibrium electron-phonon transport in nanometer-scale silicon fets," *Electron Devices, IEEE Transactions on*, vol. 55, no. 1, pp. 220–232, Jan 2008.

[4] K. Kukita and Y. Kamakura, "Monte carlo simulation of phonon transport in silicon including a realistic dispersion relation," *Journal of Applied Physics*, vol. 114, no. 15, pp. 154 312–154 312–8, Oct 2013.

[5] K. Kukita, I. Adisusilo, and Y. Kamakura, "Monte carlo simulation of diffusive-to-ballistic transition in phonon transport," *Journal of Computational Electronics*, vol. 13, no. 1, pp. 264–270, 2014.

[6] K. Kukita, I. Adisusilo, and Y. Kamakura, "Impact of quasi-ballistic phonon transport on thermal properties in nanoscale devices: A monte carlo approach," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, Dec 2012, pp. 17.5.1–17.5.4.

[7] M. E. Siemens, Q. Li, R. Yang, K. A. Nelson, E. H. Anderson, M. M. Murnane, and H. C. Kapteyn, "Quasi-ballistic thermal transport from nanoscale interfaces observed using ultrafast coherent soft x-ray beams," *Nature materials*, vol. 9, no. 1, pp. 26–30, 2009.

[8] M. Shrivastava, M. Agrawal, S. Mahajan, H. Gossner, T. Schulz, D. Sharma, and V. Ramgopal Rao, "Physical insight toward heat transport and an improved electrothermal modeling framework for finfet architectures," *Electron Devices, IEEE Transactions on*, vol. 59, no. 5, pp. 1353–1363, May 2012.

[9] T. Yamane, N. Nagai, S.-i. Katayama, and M. Todoki, "Measurement of thermal conductivity of silicon dioxide thin films using a 3ω; method," *Journal of Applied Physics*, vol. 91, no. 12, pp. 9772–9776, Jun 2002.