Physics of electronic transport in low-dimensionality materials for future FETs

(Invited Paper)

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***Abstract*—We show that scaling rules, quantum confinement in thin bodies, and the resulting gate leakage render imperative the use of low-dimensionality materials as channels in devices scaled beyond the 10 nm gate length. We then consider a few examples of two-dimensional materials of great interest, graphene and bilayer graphene, and show how the dielectric environment (gate and interlayer insulators, nearby gates) has a dramatically strong effect on the electronic properties of systems such as supported graphene, nanoribbons, and graphene bilayers in which a Bose-Einstein exciton condensation has been predicted to occur at high temperature. Finally, we consider the novel concept of devices based on monolayer tin ('stannanane') as a topological insulator.**

I. Introduction

When approaching the problem of scaling electronic devices beyond the 10 nm gate length, shorter-term industrial goals understandably focus on realistic low-to-medium-risk avenues, some already in production – such as strained Si/Ge, FinFETs, or high-κ dielectrics, some yet to be translated to products in the near future – such III-V semiconductors, tunnel- and nanowire-FETs. Longer-term avenues, however, must also be investigated even going beyond carbon-based electronics (carbon nanotubes, graphene, nanoribbons), such as transition metal dichalcogenides, silicene/ane, germanene/ane (together with other sp^2 and sp^3 hybridized monolayers), topological insulators, Weyl semimetals, and other strongly correlated fermion systems... as 'improbable' as they might be. Here we will first discuss how, if we really wish to scale to 5 nm, simple electrostatic scaling laws demand that we take low-dimensionality materials very seriously, despite the daunting associated processing difficulties.[1] We will then consider whether graphene has any chance of replacing Si by looking at how the extremely promising electronic properties it exhibits in its ideal form become much less interesting when used as active layer in of some non-ideal dielectric structure (such when supported and gated and/or in nanoribbon form)[2]. Finally, we will discuss a couple of very interesting, albeit admittedly improbable, ideas: 1. The Bose-Einstein condensation in bilayer systems (motivating the concept of BiSFETs[3]) as an example of how issues of practical implementation may regrettably transform an excellent idea into a pure academic exercise; and 2. Monolayer tin (stannanane) as a 2D topological insulator with potential applications in spintronics and low-power high-performance devices[4], [5].

II. Gate leakage and quantum confinement

The need to consider low-dimensionality channels stems from a simple consideration[1]: As we scale the gate length of field-effect transistors (FETs) with 'conventional' semiconductor channels we must also scale the thickness/diameter

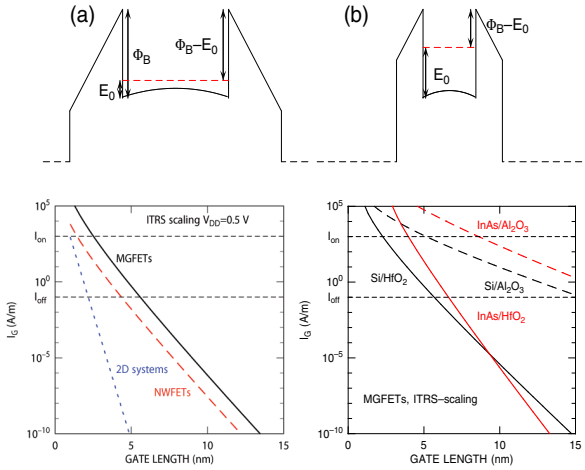

Fig. 1. **Top left (a):** Sketch showing the band diagram of a thick-body double-gate device. **Top right (b):** The same, but for a scaled thin-body device. Quantum confinement in the channel opens the gap, shifts the ground-state subband upward in energy thus reducing the potential barrier between the channel and the gate insulator and increasing the gate tunneling current. **Bottom left:** Tunneling gate leakage current calculated using the 'relaxed' ITRS scaling rules for MGFETs, NWFETs, and 2D systems (graphene). These results have been obtained employing a 'toy' semiconductor described by an electron dispersion with an effective mass m^* = 0.25 m_0 and a non-parabolicity parameter of -2.0/eV and an HfO_2-like insulator with $\epsilon_{\rm ins}$ = 24 $\epsilon_{\rm vac}$, a tunneling mass $m_{\rm ins}$=0.5 m_0, and a semiconductor/insulator barrier $\Phi_{\rm B}$ = 2.75 eV. A line showing the 'on-current' (of the order of 1 mA/μm) and the 'off-current' (a factor of $\approx 10^4$ smaller than the on-current) are shown to emphasize the fact that the gate leakage can become a serious problem also in the on-state. **Bottom right:** As in the left frame, but now for MGFETs only, ITRS scaling, and using semiconductor and insulator parameters relative to the materials shown and subband energy in the thin body obtained from empirical pseudopotential calculations, as given in [1]. Note that the use of a more 'correct' Poisson scaling would yield even larger values of the gate current $I_{\rm G}$. (From [1], Copyright IEEE, 2013.)

of the channel-body itself. Following [6] (fully-depleted SOI, FDSOI) and [7], [8] (nanowires, NW), the total 'dielectric thickness' of the semiconductor body, t_s for a static dielectric constant ϵ_s, and total thickness of the insulating layer(s), $t_{\rm ins}$, with dielectric constant $\epsilon_{\rm ins}$ must be smaller than the gate length $L_{\rm G}$ according to the relation:

$$L_{\rm G} \;\geq\; \alpha\;[t_{\rm s} \;+\; (\epsilon_{\rm s}/\epsilon_{\rm ins})\;t_{\rm ins}] \qquad (1)$$

where the parameter α – obtained either from analytic studies of the 2D Poisson equation[6] or numerical simulations of the threshold-voltage roll-off and sub-threshold swing of

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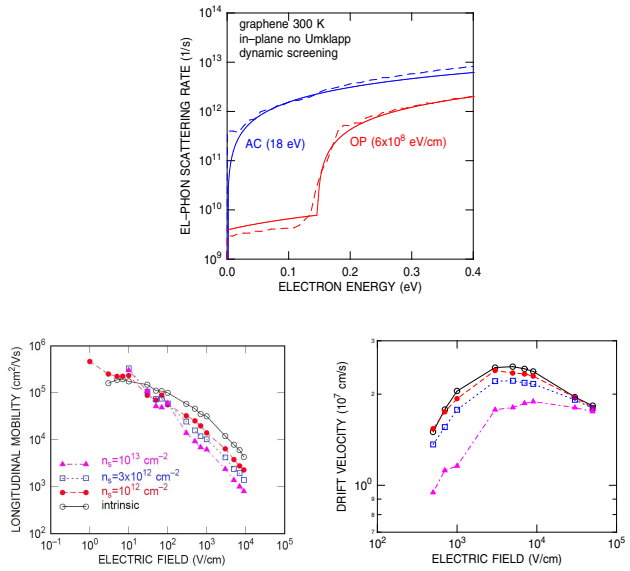

Fig. 2. **Top:** Total electron/acoustic-phonon and electron/optical-phonon scattering rates calculated using a conventional analytic expression (solid lines) fitted to the screened rigid-ion results (dashed lines). The empirical deformation potentials so obtained can be compared with those employed in the literature. **Bottom:** Longitudinal electron mobility (left) and drift velocity (right) in graphene at 300 K as a function of electric field along the [10] direction calculated using the Monte Carlo method. The various curves are parametrized by the electron density. (From [2], Copyright Institute of Physics, 2013.)

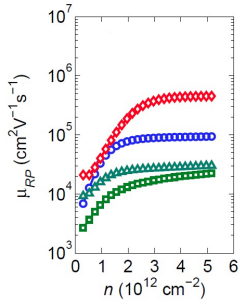

Fig. 3. Calculated electron mobility limited by remote-phonon scattering for ideal graphene supported by SiO_2, HfO_2, h-BN, and Al_2O_3. (From [10], Copyright American Institute of Physics, 2012.)

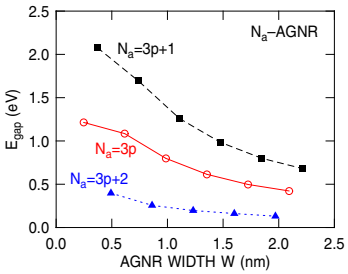

Fig. 4. Dependence of the bandgap of AGNRs on ribbon-width. The lines connecting the calculated points are only a guide to the eye. (From [13], Copyright American Institute of Physics, 2011.)

NWFETs[7] – takes the values $\alpha = \alpha_{\rm SOI} \approx 3.5$ and $\alpha = \alpha_{\rm NW} \approx 1.5$ for FDSOIs and NWFETs, respectively. The parameter α suitable for multi-gate FETs (MGFETs) is expected to be somewhere in between these extremes and, as shown in [1], we have found that a value $\alpha_{\rm MG} \approx 2.5$ guarantees satisfactory electrostatic integrity.

As the body-thickness $t_{\rm s}$ is reduced, the ground-state subband is pushed to higher energies. This results in a reduction of the effective channel/gate-insulator(s) barrier(s) and thus in a higher gate-current leakage. We have studied the problem using scaling rules extracted from either the 2011 ITRS-Roadmap[9] (finding them excessively 'relaxed') or the aforementioned stricter scaling rules from the literature confirmed by simulations of 5 nm gate-length III-V FETs[1]. Employing local empirical pseudopotentials to calculate the electronic structure of Si and InAs thin bodies, the leakage gate current in the on-state is shown to reach worrisome values at gate lengths of about 5 nm. These results, shown in Fig. 1, suggest that 1D channels (*i.e.*, nanowires) but especially channels based on 'intrinsically' 2D (*e.g.*, graphene/graphane or transition-metals dichalcogenides) or 1D (*e.g.*, carbon nanotubes) structures are required to push scaling towards the 5 nm gate length.

III. Supported Graphene and Nanoribbons

The outstanding intrinsic electronic properties of graphene are well known and are illustrated in Fig. 2. We have calculated the intrinsic electron-phonon interaction using the rigid-ion approximation and empirical pseudopotentials, as described in [2] (Fig. 2, top) and calculated the electron mobility (Fig. 2, bottom left) and drift-velocity *vs.* field characteristics (Fig. 2, right), results in rough agreement with available experimental data. However, the use of graphene in VLSI technology requires opening a gap (as in biased bilayer graphene or armchair-edge nanoribbons, AGNRs) and a dielectric environment consisting of a supporting substrate and gate insulators. Each of these constraints contribute to a reduction of the electronic properties. These effects are illustrated in Figs. 3-6. The first figure shows the calculated electron mobility in ideal graphene sheets supported by an insulating substrate: Scattering with the coupled plasmon/insulator-optical-phonons depresses the electron mobility, significantly so at low densities when dielectric screening is less effective[10]. AGNRs present an even more interesting physical picture: Because of the 'claromatic' effects that, depending on ribbon-width, lead to different electronic properties (band gap, Fig. 4, and deformation potential for scattering with longitudinal acoustic phonons[2], [11], [12], Fig. 5, left), the electron mobility shown in Fig. 5, right, can be depressed significantly to values of a few 1000s cm^2/Vs unless precise control of the AGNR width is enforced. Even more serious are the concerns caused by line-edge scattering in AGNRs: Because of the claromatic dependence of the band gap on ribbon-width, the roughness associated with the removal/addition of even a single atom can lead to a scattering potential so strong as to invalidate the Born approximation and lead to an extremely small electron mobility.[13]. This is illustrated in Fig. 6.

IV. Gated BiSFETs and Bose-Einstein Condensation

A transition from a normal to a superfluid state has been predicted to occur in bilayer graphene (BLG) at temperatures approaching 300 K[14], [15], [16]. Biasing gated BLGs so that equal densities of electrons and holes are induced in the two layers, strong Coulomb interactions cause the excitonic pairing of electrons and holes with opposite momenta and their Bose-Einstein condensation, as in the Bardeen-Cooper-Schrieffer (BCS) theory, the which layer degree of freedom (pseudospin) replacing spin. Based on these predictions, novel low-power high-performance devices exploiting the unique properties of the condensate have been proposed (bilayer pseudospin field-effect transistors, BiSFETs)[3]. Here we show that, bypassing the controversy on how to account correctly for dielectric

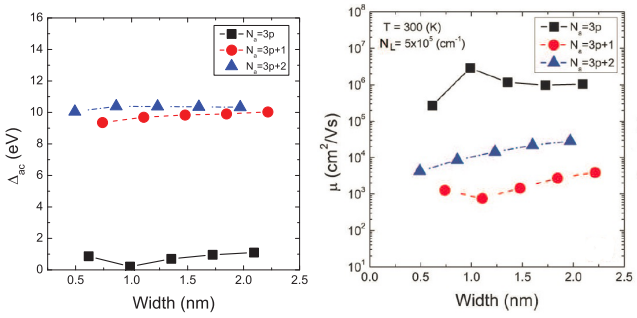

Fig. 5. Longitudinal acoustic deformation potential for AGNRs as a function of ribbon width calculated from density functional theory (left) and phonon-limited electron mobility calculated using the Kubo-Greenwood formula with full band structure (right). Note that only AGNRs with width corresponding to a number of atomic lines equal to a multiple of 3 does the electron mobility retain values similar to those of ideal infinite graphene sheets. (From [2], Copyright Institute of Physics, 2013.)

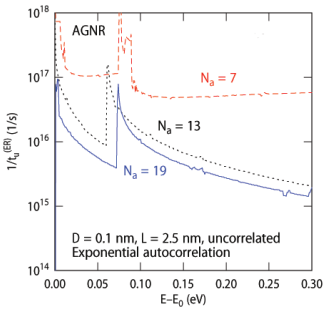

Fig. 6. Velocity relaxation time due to scattering with line-edge-roughness (Prange-Nee component only) as a function of electron energy (measured from the bottom of the conduction band) in three H-terminated armchair-edge GNRs with width given by $N_a = 3p+1$ atomic lines (N_a = 7, 13, and 19). A total number of 6 subbands has been employed together with an exponential autocorrelation. Note the very large scattering rates originating from the claromatic dependence of the gap shown in the top frame of Fig. 4. Relaxation rates so large obviously bear implications on the electron mobility of narrow AGNRs, but their magnitude casts doubts on the suitability of perturbation theory (Born approximation) and, more appropriately, of employing Bloch states to to deal with this issue. (From [2], Copyright Institute of Physics, 2013.)

screening of the electron-hole interaction, the presence of the ideal metallic gates reduces dramatically the magnitude of the superfluid gap (and so, the transition temperature), rendering alternative device designs[17] a necessity. Details can be found in [18].

As discussed in [19], there are diverging opinions on how to account correctly for the dielectric screening of the interlayer Coulomb interaction $V(q)$. The values for the superfluid gap at the Fermi surface, $\Delta(k_{\rm F})$, calculated in terms of the Fermi energy, $E_{\rm F}$, range from $\Delta(k_{\rm F}) \sim 0.1E_{\rm F}$ (unscreened interaction as in [15], corresponding to a transition temperature $T_{\rm C} \sim 100$ K) to $\Delta(k_{\rm F}) \sim 10^{-7}E_{\rm F}$ (statically screened as in [20], $T_{\rm C} \sim 1$ mK), a huge difference with obvious practical implications. In all cases, only the ideal geometry of BLGs embedded in an infinite dielectric medium had been considered. In practice, however, in trying to detect the phase transition and in designing BiSFETs, one must employ a gated and supported BLG. Here we show that even assuming the very optimistic scenario of an unscreened interlayer interaction, the proximity of ideal metal gates screens the interaction to the extent of reducing $T_{\rm C}$ to values too small to be of practical use or even observable.

We have considered BLGs with interlayer separation $d \sim$

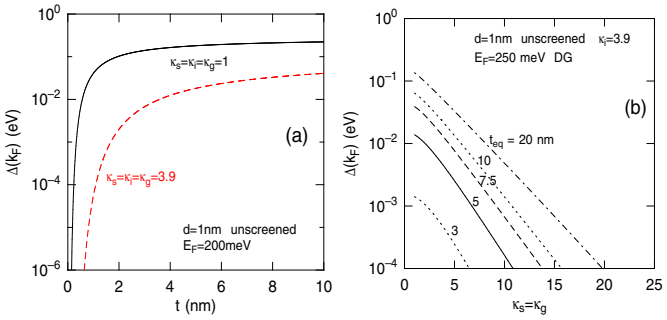

Fig. 7. **Left:** Dependence of the calculated superfluid gap at the Fermi surface on physical gate-insulator thickness t (a) assuming the dielectric geometries indicated, a Fermi energy of 200 meV, and an unscreened interlayer interaction. Since interlayer tunneling is ignored, small values of d represent an unrealistically idealized situation. **Right:** Dependence of the calculated superfluid gap at the Fermi surface on the relative dielectric constant $\kappa_{\rm g} = \kappa_{\rm s}$ of the top- and bottom-gate dielectrics for a fully symmetric double-gate geometry. An interlayer dielectric with dielectric constant $\kappa_{\rm i}$ =3.9 is assumed. The curves are parametrized by the equivalent oxide thickness over the range $t_{\rm eq}$ = 20, 10, 7.5, 5, and 3 nm. A Fermi energy of 250 meV and an unscreened interlayer interaction is also assumed. (From [18], Copyright American Institute of Physics, 2014.)

1 nm and either a single metallic gate at a distance t above the top layer or a symmetric double-gate geometry. We indicate with $\kappa_{\rm s}$, $\kappa_{\rm i}$, and $\kappa_{\rm g}$ the dielectric constants of the substrate/bottom dielectric, interlayer and gate dielectrics, respectively. We have obtained the Greens function for the Poisson equation in the gated BLG geometry, derived the expression for the interaction potential $V(q)$, and solved iteratively the gap integral equation to obtain $\Delta(k)$.

To summarize our main results: For single-gate geometries, a very close gate (with an equivalent SiO_2 thickness $t_{\rm eq}$ = 1 nm) reduces the magnitude of the gap to insignificant levels and even more so in the presence of the strong dielectric mismatch that arises when different insulators are employed. The left frame of Fig. 7 quantifies this conclusion showing that, even in homogeneous low-κ environments, a $t_{\rm eq}$ as large as 5-to-10 nm is required to maintain a high $T_{\rm C}$. The right frame of Fig. 7 shows how the presence of a double gate affects negatively the already pessimistic conclusions hinted at left: Only thick ($t_{\rm eq} > 10$nm), low-κ (< 2) gate insulators can afford the observation of the phase transition, but with this constraint the design of BiSFETs faces significantly challenges.

V. Tin Monolayer: Stannanane

Tin monolayers ('stannanane', with a buckled sp^3 hexagonal structure like graphane) functionalized by halogens, iodine in particular, have been theoretically predicted to be two-dimensional topological insulators with a band gap exceeding tens of $k_{\rm B}T$[4], so that 'iodostannanane' ribbons will possess topologically-protected edge states. Electronic transport in these edge states exhibits intriguing properties: Since spin and wavevector (velocity) are locked because of time-reversal symmetry, carriers cannot back-scatter within the same edge-state, but only to states at the other edge. In wide ribbons this is an unlikely process, because of the small overlap integral between 'far away' wavefunctions at opposite edges (see Fig. 8). However, by increasing the gate bias, and so moving the Fermi level within the bulk band gap, it is possible to increase the overlap integral, thus dramatically reducing the conductivity of the ribbons. The mobility and conductivity of iodostannanane ribbons can thus be modulated over several orders of magnitude[5] (see Fig. 9), thus opening the possibility of conceiving field-effect transistors that operate in a manner

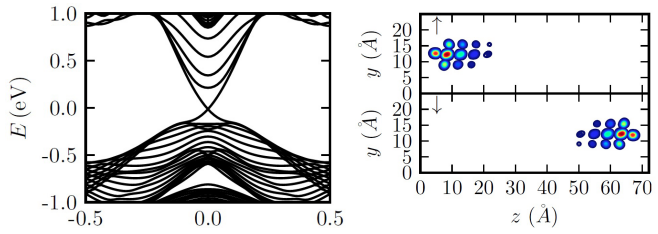

Fig. 8. **Left:** Band structure of a stannanane nanoribbon functionalized by iodine. The band structure emerges from the folding of the 'bulk' stannanane band structure along the Γ-to-K direction, except for the edge-states with Dirac-like dispersion crossing the gap. **Right:** Squared amplitude of the wavefunction for one spin component for the k <0 edge-states. Intra-edge scattering is prohibited because of spin-polarization whereas inter-edge backscattering is rendered unlikely because of the small overlap between the edge-state wavefunctions in wide ribbons.

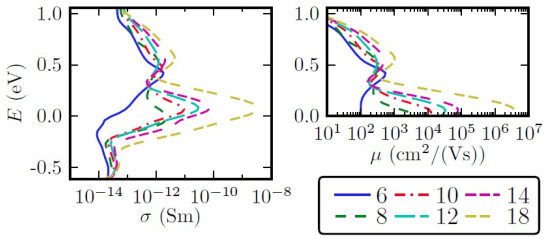

Fig. 9. Calculated conductivity and mobility for iodostannanane. The phonon spectrum and the deformation potential for scattering with longitudinal acoustic phonons have been obtained from DFT calculations. Note that the conductivity reaches a maximum when the Fermi level is inside the band gap and it is reduced by up to 4 orders of magnitude when the Fermi level moves into the conduction or valence band. The labels 6 through 18 in the legend indicate the ribbon-width expressed in number of atomic lines.

opposite to conventional FETs, the drain current decreasing sharply with increasing carrier density. The expected excellent I_{on}/I_{off} ratio and on-current of iodostannanane-based FETs[21], together with the small bias required and the near-ballistic transport in this system suggests potential low-power, high-performance applications.

Clearly, the major concern is whether or not stannanane can even exist: Density functional theory (DFT) and *ab initio*-thermodynamics calculations suggest that indeed I-functionalized Sn-monolayers are stable when grown on a proper substrate, such as (111) InSb or CdTe[22], but experimental confirmation is still missing.

VI. Conclusions

We have shown that it may be necessary to use low-dimensionality-materials as channel materials for sub-10 nm FETs, despite the processing challenges their growth and quality-control may pose. We have shown, however, that even materials with outstanding intrinsic electronic properties may suffer when embedded in a realistic dielectric environment as required when designing and fabricating FETs: The effect of the insulating substrate or gate dielectric and the patterning of graphene into AGNRs degrades significantly electronic transport, although proper processing control in a mature technology may bypass these difficulties. On the other hand, we have shown that the unavoidable presence of metallic gates may depress the normal-superfluid transition temperature in BiSFETs to values so low as not to be practical. Finally, we have considered the idea of 2D topological insulators, showing the potential (only theoretical for now) of iodostannanane as the channel material in a new kind of FETs.

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