Experimental characterization of BTI defects

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Abstract— **Selected physical and electrical characterization of gate-oxide defects is reviewed. Interfacial dangling bond defects at interfaces of Si and SiGe are characterized electrically and compared to the electron spin resonance data. It is found that additional silicon dangling bonds (P_{b0}-ceters) acting as amphoteric interface traps are generated upon oxygen scavenging anneal. A close density of P_{b0} centers is also found in Si/SiGe/Si/HfO_2 stack. The Ge dangling bond defects (Ge P_{b1} centers) found at interfaces of SiGe with thermal SiO_2 are shown to behave as acceptor centers. The properties of individual gate-oxide defects in FETs are studied with Time-Dependent Defect Spectroscopy (TDDS), an electrical characterization technique. The primary properties of a defect are its capture and emission time constants, both dependent on the local electric gate field and the temperature. Considering the wide distributions of these defect properties, complete characterization of many defects is required over the full gate and drain voltage range from 0 to VDD at different temperatures. This is desirable in order to model degradation for large, "analog" FETs and to model the ΔV_{th}-variability of deeply-scaled FETs. The impact of individual charged defects on transistor properties is then discussed. It is shown that the shift in the threshold voltage is exponentially distributed, with a small fraction of defects causing significant shifts of tens of mV. The average impact per charged defect is experimentally confirmed to be increasing with the gate oxide thickness, the substrate doping, and with the decreasing FET area. The average impact per charged defect is found to be reduced in SiGe substrates, contributing to lower degradation of SiGe-based FETs. In low-doped substrates, other sources of variability, such as interface states, are shown to take over. The impact of a single charged gate-oxide defect on the full I-V characteristic is measured and corroborated by atomistic device simulations, thus enabling the path to compact modeling of degraded deeply-scaled FET devices. Finally, the model explaining the correlation between drain and gate current RTN is discussed.**

I. Introduction

The so-called Bias-temperature instability (BTI) in CMOS technologies with both conventional and advanced gate stacks remains at the forefront of reliability concerns. The device instability arises from charging of defects (traps) in the gate dielectric and at its interface with the substrate. Here we review several recent insights into the properties of these traps obtained with both electrical and physical characterization techniques. In Section II, the properties of interface defects are studied in large devices. In Sections III and IV, we discuss the temporal and electrostatic properties of individual bulk oxide traps, as investigated in deeply-scaled devices.

II. Si/ and SiGe/SiO_2 Interface traps

Compared to the workhorse (100) face, transport along the (110) crystallographic plane of Si offers enhancement in hole mobility as well as a more compact architecture of metal-oxide-semiconductor (MOS) field-effect transistor (MOSFET), e.g., vertical MOSFET and finFET devices, while remaining within the framework of the highly developed Si MOS fabrication process. We evaluated the trap density at interfaces D_{it} of (110), (111) and (100)Si with thermal SiO_2 systems by using conductance and capacitance methods. The results of these experiments are illustrated by the experimental $D_{it}(E)$ profiles shown in Fig. 1. The inferred D_{it} is found highly sensitive to the Si crystal orientation, highest for the (111) face, and lowest for the (100) face, with (110)Si/SiO_2 closely resembling the (111)Si/SiO_2 case. Two peaks in the $D_{it}(E)$ profile within Si band gap, at about 0.25 eV and 0.85 eV above the valence band (VB), are observed for all three orientations and correlate with the densities of Electron-Spin Resonance (ESR) active P_b interface defects (dangling bonds of the surface Si atoms), responsible for the majority of amphoteric interface traps.

As the next step, we addressed the effect of oxygen scavenging on the interface defect density in p-Si/HfO_2 (1.8 nm)/TiN_x/poly-Si structures. The scavenging has been performed by applying laser annealing to the samples in O-free ambient at 700, 900, or 1100 °C. Since these structures have aggressively downscaled insulator thickness (EOT=0.6 nm), they exhibit considerable leakage current which precluded us from the application of conventional interface trap characterization techniques. For the p-Si/HfO_2 (1.8 nm) interface the total N_{it} of about $5\times10^{12}cm^{-2}$ is estimated.

Despite the absence of reliable electrical data, density of interface defects can still be evaluated by ESR. The ESR measurements allowed us to estimate density of P_{b0} centers which, as it has been discussed above, provide the major contribution to interface trap density at the interfaces of thermally oxidized silicon. Densities of paramagnetic P_{b0} centers found from these measurements are summarized in Fig. 2 for 1.8 nm thick HfO_2 and ZrO_2 insulators. The results indicate an increase in the density of P_{b0} centers after high-temperature

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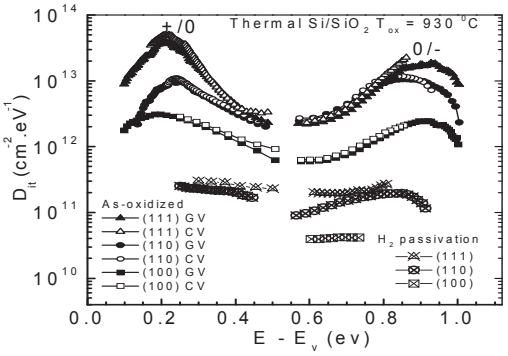

Fig. 1. $D_{it}(E)$ profiles of Si/SiO_2 interfaces derived from CV (solid symbols) and GV (open symbols) methods in Si/SiO_2 samples fabricated on (100), (110), and (111) faces of Si.

annealing of Si/HfO_2 interface suggesting its structural and electrical degradation. Interestingly, if performing the O scavenging annealing by using spike-processing in He at 1035 °C (cf. Fig. 2), no measurable interface damage is found. This observation points towards interface degradation mechanism triggered by formation of Si-O molecules by reaction of a SiO_2-like IL with Si substrate:

$$SiO_2 + Si \rightarrow 2SiO(gas), \qquad (1)$$

which has earlier been identified as the primary mechanism of degradation of Si/SiO_2 interfaces upon annealing in the O-deficient ambient. Application of He gas during annealing allows one to significantly suppress this kind of degradation [1]. No traces of E' centers which are frequently invoked to explain charge trapping in the oxides on silicon and other degradation phenomena are found in the studied samples.

The interaction of molecular hydrogen with dangling bond defects represents the key technological processing allowing one to reduce the density of harmful interface traps to the device-acceptable level. On the other hand the release (re-activation) of the passivated dangling bonds is considered nowadays as the basic process of electrical degradation of semiconductor interfaces including BTI. In an attempt to verify the applicability of this concept beyond the well-studied Si dangling bond defects, we addressed dangling bonds of germanium atoms (P_b-type defects) in $Si_{1-x}Ge_x$ alloys (x = 0.75) at the interface with well-studied thermal SiO_2 insulator as affected by annealing in molecular hydrogen (passivation) and by the subsequent annealing in high vacuum (de-passivation).

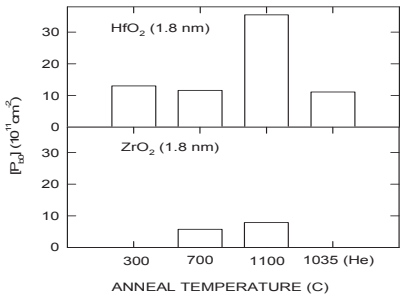

Fig. 2. Density of interfacial P_{b0} defects found at interfaces of (100)Si with 1.8-nm thick layers of HfO_2 (top panel) and ZrO_2 (bottom panel) after different annealing treatments.

Analysis of the density of the Ge dangling bond defects remaining electrically and ESR active was conducted upon isochronal anneals in the range of temperatures from 100 to 425 °C shown in Fig. 3, as well as kinetics of isothermal passivation and de- passivation (cf. Fig. 4) using the standard first-order kinetics equations. These observations were conducted using both the electrical detection of the Ge P_{b1} centers as acceptors in SiGe [2] and by ESR. In general, both passivation and de-passivation processes are observed to occur at lower temperatures than at the Si/SiO_2 interfaces. The activation energies of germanium dangling bond passivation by H_2 molecule and the activation energy of Ge-H bond thermal dissociation were found equal to E_f =1.44 ± 0.04 eV and E_d= 2.23 ±0.04 eV, respectively.

Contrary to the well-studied case of dangling bonds of silicon atoms at the interfaces with the same insulator (SiO_2),

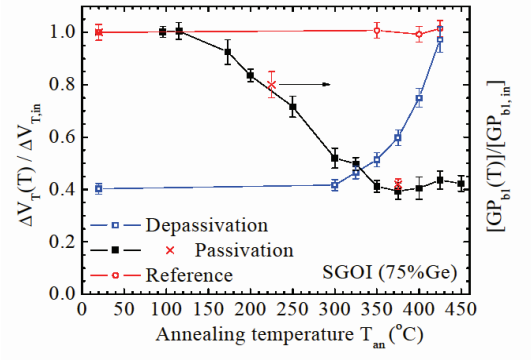

Fig. 3. Density of electrically active paramagnetic Ge P_{b1} defects observed at the interfaces of $Si_{0.25}Ge_{0.75}$ alloy with thermal SiO_2 as a function of isochronal (30 min) anneal temperature in 1.1 atm. H_2 (passivation) or in vacuum (dissociation).

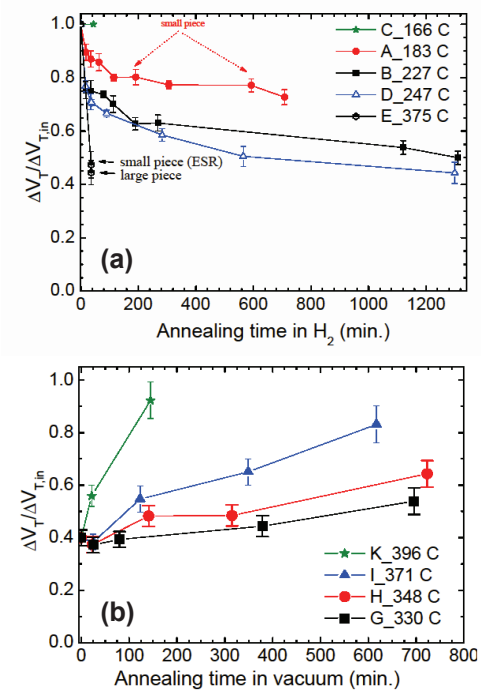

Fig. 4. Density of electrically active paramagnetic Ge P_{b1} defects observed at the interfaces of $Si_{0.25}Ge_{0.75}$ alloy with thermal SiO_2 as a function of isothermal anneal time in (a) 1.1 atm. H_2 (passivation) or (b) in vacuum (dissociation).

the sum of these two energies appears to be significantly lower than the thermodynamic binding energy of the H_2 molecule (4.4 eV). This discrepancy might be explained either by different charge state of the Ge P_b-type defects (negatively charged) during passivation or, else, by the presence of additional H_2 cracking centers. Furthermore, the statistical (site-to-site) spread of the activation energies for Ge P_b-center passivation and de-passivation appears to be significantly larger (by a factor of about 3) than for Si dangling bonds. This large variability makes it impossible to achieve the complete passivation of the Ge dangling bonds, about 40 % of which remain electrically active even after highest thermal budget of the H_2 passivation anneal (425 °C).

III. Individual Trap Properties

The understanding of oxide trap behavior is crucial for a number of reliability issues, like the bias temperature instability, hot carrier degradation, time-dependent dielectric breakdown, random telegraph and 1/f noise. Recent results have demonstrated that hole capture and emission into oxide traps in pMOS transistors are more complicated than the usually assumed Shockley-Read-Hall-like process [3, 4]. In particular, both charging and discharging proceed via a non-radiative multiphonon (NMP) mechanism involving metastable defect states.

The Time-Dependent Defect Spectroscopy (TDDS) is an electrical characterization technique allowing the extraction of properties of individual gate-oxide defects in FETs. The primary properties of a defect are its capture and emission time constants, both dependent on the local electric gate field and the temperature. Considering the wide distributions of these defect properties, complete characterization of hundreds of defects is required over the full gate and drain voltage range from 0 to VDD and also at different temperatures. This is desirable in order to model degradation for large, "analog" MOSFETs and to model the ΔV_{th}-variability of deeply-scaled FETs.

Employing the "conventional" TDDS technique illustrated in Fig.5, and by varying temperature and gate bias we could determine the field dependence and thermal activation of individual defects [5].

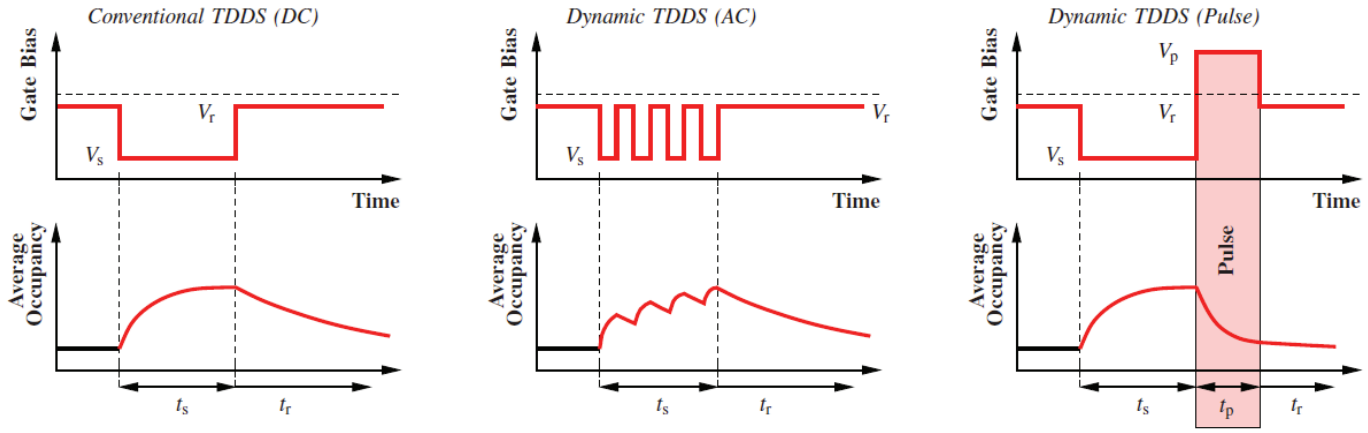

Fig. 5. Illustration of the 3 different measuring schemes used by TDDS: Shown **left** is the conventional DC TDDS measurement procedure, during which defects are charged at a stress voltage V_s and discharged during the subsequent recovery at V_r. This sequence is typically repeated 100 times to allow for a statistical analysis of the discrete emission events. In the **middle,** the dynamic AC TDDS measurement is shown, where defects are subjected to an AC signal switching between V_s and V_r, followed by a discharge period at V_r [6]. Finally, on the **right**, for the dynamic pulse TDDS, a pulse V_p is applied for the duration t_p between the charging and discharging biases [7].

Fig. 6 shows our proposed defect model, including two stable and two metastable states. The existence of these metastable states could be clearly demonstrated by extending the previously introduced time-dependent defect spectroscopy to a more general dynamic case, by employing AC stress [8]. Varying the AC stress frequency for 1kHz to 5MHz clearly reveals a frequency-dependence of the capture time of individual defects [7]. Such a frequency-dependence would not exist for a first order capture process and thus clearly confirms the existence of the intermediate metastable state 2'.

Fig. 7 shows that charge emission can be drastically accelerated for some defects by applying a gate bias V_p into the depletion regime. Since the drain current is very small in depletion, emission events cannot be directly measured. Therefore the emission time constant is indirectly measured in this regime: After charging a given defect to an occupancy level of 100% by applying a sufficiently long stress pulse, a series of "recovery-pulse" with a given bias V_p and lengths t_p are applied, followed by a standard recovery trace testing the occupancy. τ_e then is calculated from the decay rate $\exp(-t_p/\tau_e)$, which describes the occupancy during the recovery pulse.

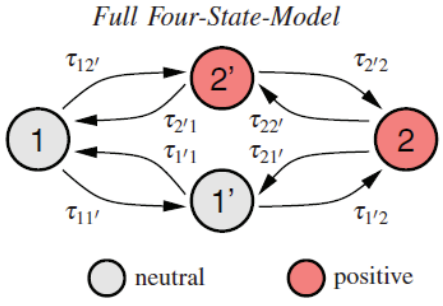

Fig. 6. The four states of oxide defects extracted from TDDS experiments [7-10]. Each defect has two stable states, 1 and 2, and possible two metastable states 1' and 2'. The metastable state 2' seems to be always present, while the existence of metastable state 1' decides on whether the trap behaves like a fixed positive or a switching trap [11].

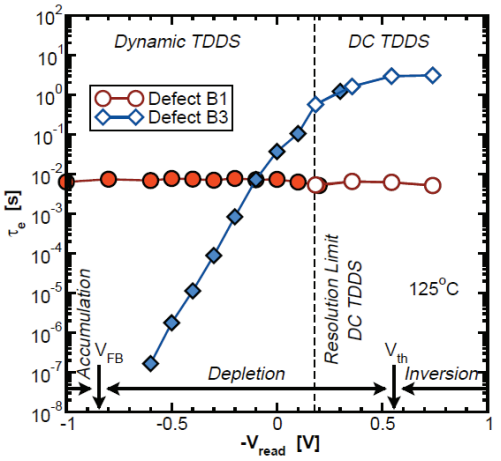

Fig. 7. An example for the wide range of extracted emission time constants for two defects using the "dynamic" TDDS technique. The range is extended to gate voltages far below threshold where no drain current can be measured. The emission time constant of defect B1 is bias-independent revealing B1 as a fixed positive trap. Defect B3 is a switching trap because of its bias-dependent emission time constant. The symbols are the data while the lines are from the NMP model [7].

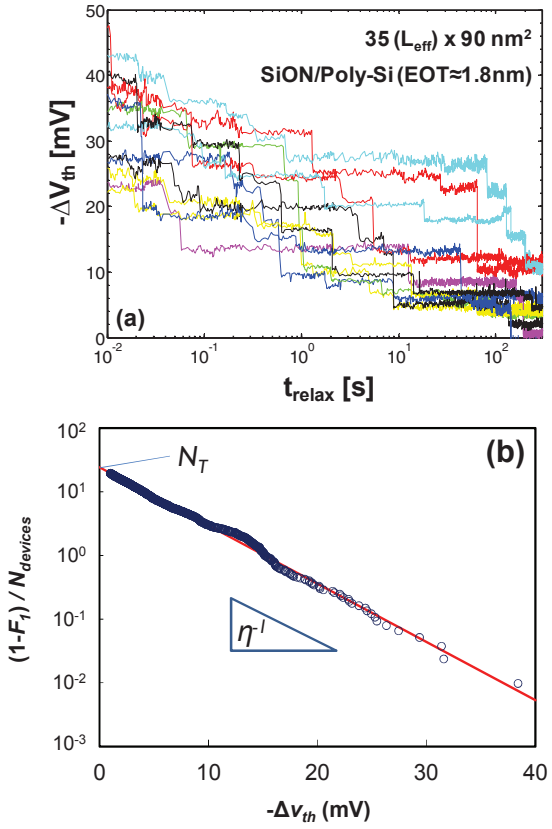

Fig. 8. (a) Typical NBTI relaxation transients, each recorded on a fresh nanoscaled pFET (W=90nm, L_{eff}=35nm, SiON/Poly-Si, EOT≈1.8nm) [14]. Steps of varying heights due to single defect-discharge events are clearly visible. (b) The ΔV_{th} step heights corresponding to the individual discharge events observed in the relaxation transients plotted on a complementary cumulative distribution function (1-*CDF*) plot. When normalized by the number of devices, the intercept with the y-axis gives the average number of defects per device N_T that emitted in the measured relaxation interval.

In summary, while all investigated traps show a frequency-dependent capture time constant, suggesting them to be of the same microscopic origin, we find two different kinds of emission behavior, namely fixed positive and switching traps, as shown in Fig.3. The multi-state NMP model perfectly captures both cases.

IV. Trap Impact on FET Properties

The reduction of FET device dimensions to nanometer scales implies that literally only a handful of defects will be present in each device, while each defect will have a substantial impact on the device operation [12]. The impact of individual charged defects on transistor properties is now discussed. Clearly defined steps due to *single*-carrier discharge events are visible in Fig. 8a in the ΔV_{th} relaxation curves in TDDS-like measurements (cf. Section III) performed on *multiple* deeply-scaled devices. Each device behaves differently, resulting in large time-dependent variability of the total ΔV_{th}. The ΔV_{th} step heights appear exponentially distributed, with the cumulative distribution function (CDF)

$$F_\eta(\Delta v_{th}) = 1 - \exp\left(-\frac{\Delta v_{th}}{\eta}\right), \tag{2}$$

with an average step height η (Fig. 8b). Note that while the majority of charged traps results in small ΔV_{th}'s, a small fraction of traps will significantly change V_{th} by up to tens of mV [12].

The average impact of a single defect η on the threshold voltage is a fundamental parameter determining the variability of deeply scaled technologies [13]. The time-dependent variance of the threshold voltage shifts of a population of devices (such as e.g. in Fig. 8a) can be shown to behave as

$$\sigma^2_{\Delta V_{th}}(t) = 2\eta\left\langle \Delta V_{th}(t)\right\rangle, \tag{3}$$

where $\langle \Delta V_{th} \rangle$ is the average threshold voltage shift due to BTI [13, 14]. Because of the similarities between BTI and Random Telegraph Noise (RTN) [12], this parameter also reflects the average expected amplitude of the RTN signal in deeply-scaled devices [14].

A low value of η is generally desired. η has been argued to scale as

$$\eta \cong \frac{t_{inv}\, N_A^{\alpha}}{A}\ , \tag{4}$$

where t_{inv} is the oxide thickness corresponding to capacitance in inversion, A the area of the device channel, and N_A the channel doping, with the exponent α has been observed to be around 0.5 in simulations [13]. In order to test Eq. 4 experimentally, we collected an extensive dataset of NBTI relaxation transients devices with different areas. Figure 9a demonstrates η scales reciprocally with device gate area, in agreement with Eq. 4 [15]. Figure 9b then demonstrates that η decreases with oxide thickness and can be changed by back bias, which effectively modulates the number of charged dopants in the channel. Both of those observations are in line with Eq. 4 [16].

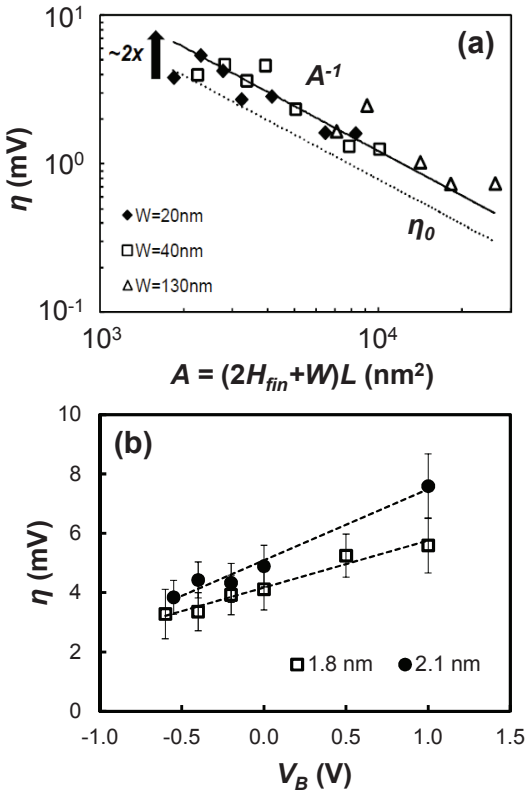

Fig. 9. (a) The average step height η scales as A^{-1} on Si pFinFETs (high-k/MG, $t_{inv} \approx 1.7$nm) with varying fin width W and gate length L (fin height H is fixed). Each point is extracted from a set of multiple devices with identical dimensions as in Fig. 8. (b) The average step height η values extracted from distributions measured for varying back-bias V_B on two wafers with identical Si/SiON/Poly-Si planar pFETs and identical doping levels, but slightly different oxide thicknesses (t_{inv} = ~1.8 and ~2.1nm). Thicker oxide increases η while forward (reverse) back bias reduces (increases) the depletion width and thus reduces (increases) η, as per Eq. 4.

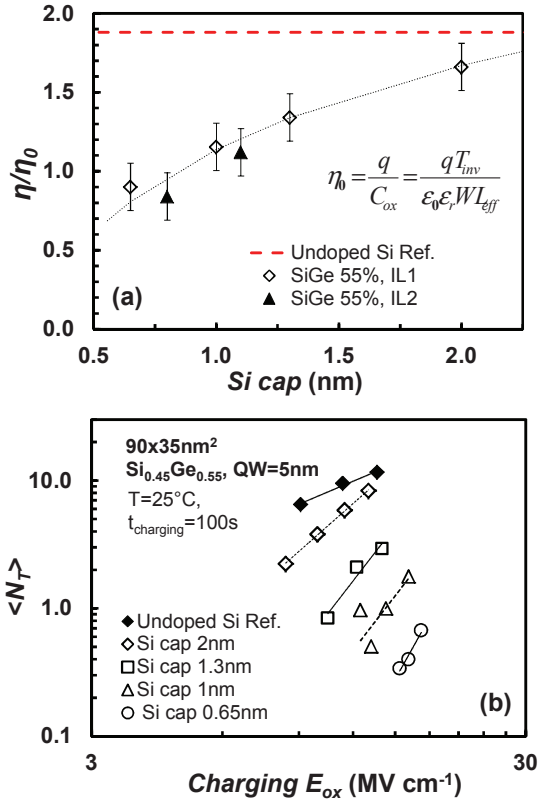

Fig. 10. (a) Extracted average ΔV_{th} step heights η for SiGe devices with different Si cap and for undoped Si channel devices, after a charging phase at $E_{ox} \approx 12$MV/cm. The extracted values of η are normalized by η_0. SiGe devices with the thinnest Si cap show a significantly lower η. The observation is confirmed on SiGe devices with two different SiO_2 interfacial layer thicknesses. The red dashed line demarcates the benchmark value experimentally estimated on undoped Si channel ref. devices. (b) Consistently with the significant NBTI reduction in large area devices, nanoscaled SiGe channel pMOSFETs with a reduced Si cap thickness show reduced average number of charging/discharging defects per device $\langle N_T \rangle$, and a stronger field acceleration.

Over the whole measured range in Fig. 9a, η is observed ~2× higher than the "naively" expected impact η_0, given by the charge sheet approximation for a single charge at substrate/dielectric interface [14,15]

$$\eta_0 = \frac{q}{C_{ox}} \cdot \qquad (5)$$

Here, q is the elementary charge and C_{ox} the gate oxide capacitance (in Farads) in inversion. In pFET devices with SiGe substrates we have, however, observed that the relative value of η will be reduced for oxide defects closer to the gate (Fig. 10a) [15]. In addition to the low impact per charged defect η, the superior NBTI robustness of SiGe-based pFET devices is also reflected in the significantly decreased number of active defects, documented in Fig. 10b [17,18].

In low doped channel devices, we have experimentally demonstrated that charged *interface* traps represent a new source of variability, as shown in Fig. 11a [14]. The value of η is then increased by further interface trap generation during operation, see Fig. 11b.

Precise circuit simulations will require models incorporating the impact of the small number of trapped charges on the *entire* FET current characteristics [12]. We have demonstrated the measurements of the impact of *a single charged gate oxide defect on the entire I_D-V_G characteristic*—in fact the ultimate reliability measurement (Fig. 12) [15]. The learning from measurements and full scale 3D 'atomistic' simulations (Fig. 12c) can be captured in reliability-aware FET compact models [19].

Finally, in order to understand and to model the impact of gate oxide defects on the FET *gate* current I_G, correlated drain and gate current RTN measurements were performed [20]. We have observed that the same defect controls both processes and constructed a corresponding defect state diagram involving a metastable state, akin to Fig. 6 [21]. Based on this picture we have proposed a qualitative model describing the correlated ΔI_G and ΔI_D distributions (Fig. 13) [21].

V. CONCLUSIONS

Reduction and mitigation of BTI in future CMOS technologies requires thorough understanding of its underlying causes—gate oxide interface and bulk defects. We have reviewed several recent findings of the properties of these defects, obtained with both electrical and physical characterization techniques.

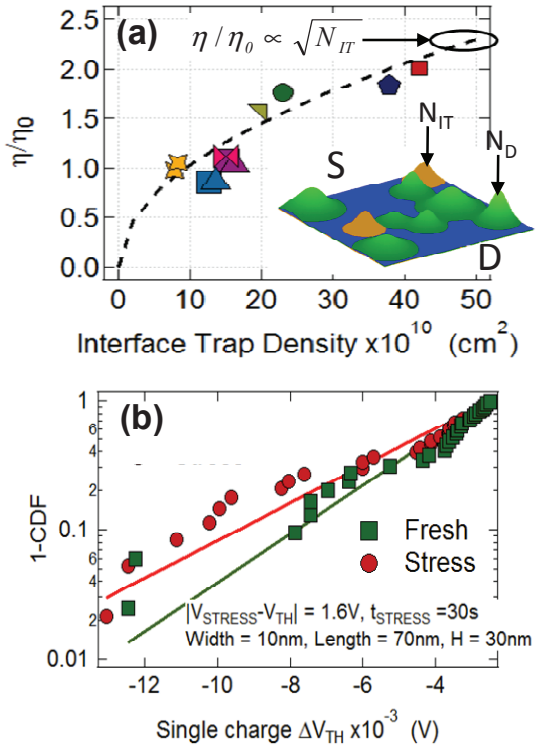

Fig. 11. (a) A clear correlation is found between single-carrier discharge ΔV_{th} and D_{it} in FinFET devices. Interface traps enhance channel conduction percolation between source and drain in the same way dopants do (inset). (b) Generation of D_{it} after electrical stress is reflected in increase of single-carrier discharge ΔV_{TH} .

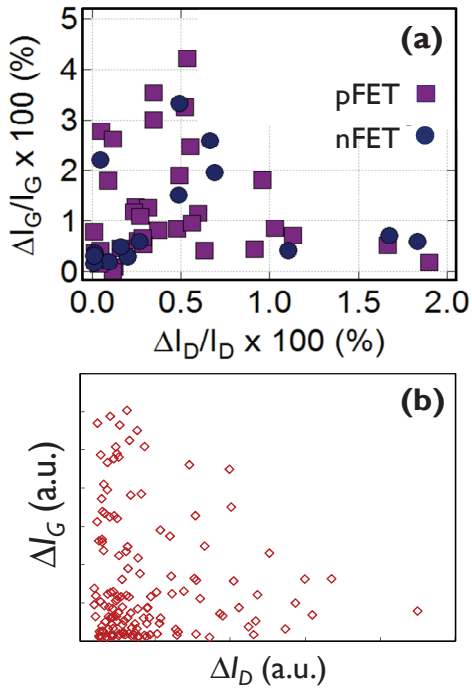

Fig. 6: (a) Correlation plot of relative changes in I_D and I_G (I_G = ~10 pA). Note that upper right corner (large I_D and large I_G fluctuations) is unpopulated. The proposed mechanism involves enhanced conduction through a gate oxide trap when it is unoccupied. Such a process would be most efficient for traps close to the center of the oxide, readily explaining why there are no defects causing both large ΔI_G and large ΔI_D. (b) The same correlation can be qualitatively constructed using this assumption, combined with the impact of a charged trap on I_D depending on the distance of the trap from the critical point of a source-drain percolation path (Fig. 12).

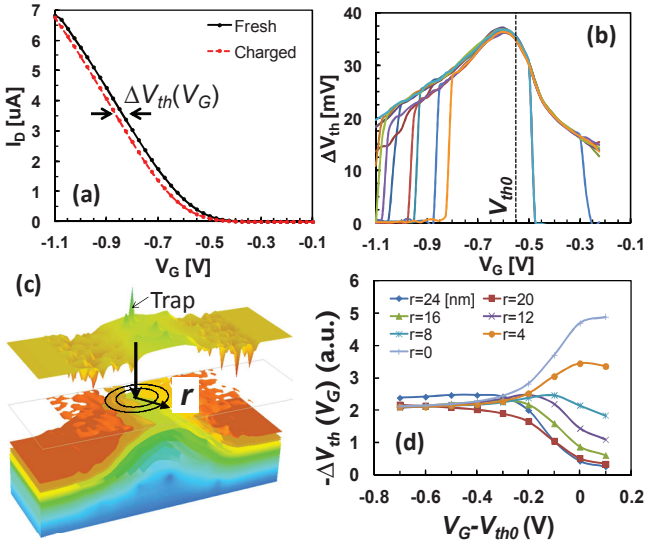

Fig. 12. The "ultimate" reliability measurement: (a) I_D-V_G curves measured at V_D = -0.1 V on a $L \times W$ = 35×90 nm^2 pFET with a single oxide defect uncharged and charged. The corresponding $\Delta V_{th}(V_G)$ is defined as a simple "geometrical" horizontal distance between the two curves at a given V_G (b) Multiple measurements of $\Delta V_{th}(V_G)$ are perfectly reproducible. (c) 3D atomistic simulations of a nanoscaled device showing an oxide defect located exactly above the critical confinement spot of the current percolation path (demarcated by the vertical arrow) can effectively suppress the channel current when charged. The simulations show the defect impact on the device characteristics depends on the radial distance r from the critical spot. (d) Different $\Delta V_{th}(V_G)$ characteristics are expected as a function of r.

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REFERENCES

[1] V. V. Afanas'ev and A. Stesmans, "Blockage of the annealing-induced Si/SiO_2 degradation by helium", Appl. Phys. Lett., vol 74, pp. 1009—1011, 1999.

[2] V. V. Afanas'ev, M. Houssa, A. Stesmans, L. Souriau, R. Loo, M. Meuris, "Electronic properties of Ge dangling bond centers at $Si_{1-x}Ge_x/SiO_2$ interfaces", Appl. Phys. Lett., vol. 95, p. 221106, 2009.

[3] A. Palma, A. Godoy, J. A. Jimenez-Tejada, J. E. Carceller, and J. A. Lopez-Villanueva, "Quantum Two-Dimensional Calculation of Time Constants of Random Telegraph Signals in Metal-Oxide-Semiconductor Structures", Physical Review B, vol. 56, pp. 9565—9574, 1997.

[4] N. Zanolla, D. Siprak, P. Baumgartner, E. Sangiorgi, and C. Fiegna, "Measurement and Simulation of Gate Voltage Dependence of RTS Emission and Capture Time Constants in MOSFETs", Proc. Workshop on Ultimate Integration of Silicon, pp. 137—140, 2008.

[5] T. Grasser, H. Reisinger, P.-J. Wagner, B. Kaczer, "Time-Dependent Defect Spectroscopy for Characterization of Border Traps in Metal-

Oxide-Semiconductor Transistors", Physical Review B, vol. 82, pp. 245318-1 — 10, 2010.

[6] M. Toledano-Luque *et al.*, "Response of a Single Trap to AC Negative Bias Temperature Stress," Proc. IEEE International Reliability Physics Symposium (IRPS), pp. 364—371, 2011.

[7] T. Grasser *et al.*, "Advanced Characterization of Oxide Traps: The Dynamic Time-Dependent Defect Spectroscopy", Proc. IEEE International Reliability Physics Symposium (IRPS), pp. 2D.2.1—7, 2013.

[8] M. Toledano-Luque, B. Kaczer, J. Franco, Ph. J. Roussel, T. Grasser, G. Groeseneken, "Defect-Centric Perspective of Time-Dependent BTI Variability", Microelectronics Reliability, vol. 52, pp. 1883—1890, 2012.

[9] M. Toledano-Luque, B. Kaczer, T. Grasser, Ph. J. Roussel, J. Franco, G. Groeseneken, "Toward a Streamlined Projection of Small Device Bias Temperature Instability Lifetime Distributions", Journal of Vacuum Science & Technology B, vol. 31, pp. 01A114-1 — 4, 2013.

[10] T. Grasser, H. Reisinger, K. Rott, M. Toledano-Luque, B. Kaczer, "On the Microscopic Origin of the Frequency Dependence of Hole Trapping in pMOSFETs", Proc. IEEE International Electron Devices Meeting (IEDM), pp. 470 — 473, 2012.

[11] T. Grasser, B. Kaczer, W. Goes, Th. Aichinger, Ph. Hehenberger, M. Nelhiebel, "Understanding negative bias temperature instability in the context of hole trapping", Microel. Eng., vol. 86, pp. 1876 — 1882, 2009.

[12] B. Kaczer *et al.*, "Atomistic approach to variability of bias-temperature instability in circuit simulations", Proc. IEEE International Reliability Physics Symposium (IRPS), pp. XT.3.1 — 5, 2011.

[13] B. Kaczer, M. Toledano-Luque, J. Franco, and P. Weckx, "Statistical Distribution of Defect Parameters", in T. Grasser (Ed.), Springer, 2013.

[14] M. Toledano-Luque *et al.*, "Degradation of time dependent variability due to interface state generation", Proc. VLSI Symposium, pp. T190—T191, 2013.

[15] J. Franco *et al.*, "Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs", Proc. IEEE International Reliability Physics Symposium (IRPS), pp. 5A.4.1—6, 2012.

[16] J. Franco *et al.*, "Reduction of the BTI Time-Dependent Variability in Nanoscaled MOSFETs by Body Bias", Proc. IEEE International Reliability Physics Symposium (IRPS), pp. 2D.3.1 — 6, 2013.

[17] J. Franco *et al.*, "SiGe Channel Technology: Superior Reliability Toward Ultrathin EOT Devices—Part I: NBTI", IEEE T. Electron Dev., vol. 60, pp. 396—404, 2013.

[18] J. Franco *et al.*, "SiGe Channel Technology: Superior Reliability Toward Ultra-Thin EOT Devices—Part II: Time-Dependent Variability in Nanoscaled Devices and Other Reliability Issues", IEEE T. Electron Dev., vol. 60, pp. 405—412, 2013.

[19] B. Kaczer *et al.*, "The relevance of deeply-scaled FET threshold voltage shifts for operation lifetimes", Proc. IEEE International Reliability Physics Symposium (IRPS), pp. 5A.2.1 — 6, 2013.

[20] M. Toledano-Luque *et al.*, "Correlation of single trapping and detrapping effects in drain and gate currents of nanoscaled nFETs and pFETs", Proc. IEEE International Reliability Physics Symposium (IRPS), pp. XT.5.1 — 6, 2012.

[21] B. Kaczer, M. Toledano-Luque, W. Goes, T. Grasser, and G. Groeseneken, "Gate current random telegraph noise and single defect conduction", Microel. Eng., vol. 109, pp. 123 — 125, 2013.