

# Expanding Role of Predictive TCAD in Advanced Technology Development

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**Abstract**—TCAD plays an increasingly critical role in advanced technology research and development. The areas of impact expanded to not only predicting device outcome from process input, but also to topics traditionally not addressed by TCAD.

**Keywords**—Predictive TCAD; CMOS scaling; stress; atomistic; KMC; hierarchical; variability; simulation

## I. INTRODUCTION

TCAD plays an increasingly critical role in advanced technology research and development. The areas of impact expanded to not only predicting device outcome from process input, but also to topics traditionally not addressed by TCAD. New TCAD simulation models and methodologies need to be developed when technology advances beyond classical scaling regime. The growing number of materials used in devices increases process complexities, experimental design space and R&D cost. Accurately accounting for stress enhancement in various wafer or channel orientations, and in different channel materials is essential to yield predictive simulation of modern devices. Proper and predictive transport modeling in various materials and structures is one of TCAD's most significant challenges. The use of atomistic level and full quantum mechanical simulations becomes indispensable in order to explore materials beyond these having readily available data. In order to deliver timely guidance in development, TCAD needs to be calibrated to have reasonable predictability before reliable data become available. This requires a rethinking of calibration, which needs to be geared toward targeted applications, with main goal to increase its predictive ability in that specific application. A hierarchical approach which leverages ab-initio calculations, KMC, and continuum models to deliver predictive simulations can be highly desirable. TCAD has also been increasingly called upon to address variability and reliability simulations.

## II. DEVICE SCALING TREND AND NEW TCAD CHALLENGES

### A. Enhancement to classical scaling

CMOS chip scaling, predicted by Moore's Law [1], has been the main driving force behind the phenomenal growth of semiconductor industry. The key to scaling is achieving  $\sim 2\times$  increase of circuit density as well as significant transistor switching performance with every technology node. Amazingly, both density and transistor performance gain had been realized for more than three decades by a simple geometrical and supply voltage scaling, first projected by Dennard, et al. [2] in 1974. However, a few years into the new millennium, this straight forward scaling started failing to

realize expected transistor performance gain due to gate leakage limiting  $T_{inv}$  scaling and off state leakage with worsening short channel effect limiting  $V_t$  scaling, as illustrated in Figure 1 [3].

In the last decade, various innovations have been introduced to make up for these transistor performance short falls. As illustrated in Figure 1, these innovations include channel mobility enhancement by process-induced strain [4-10],  $T_{inv}$  scaling with gate tunneling reduction by high-K/metal gate [11-13], and electrostatic control improvement by transition from planar single gate to 3D FinFET/Multi-Gate FET (MUGFET) structures [14-20].

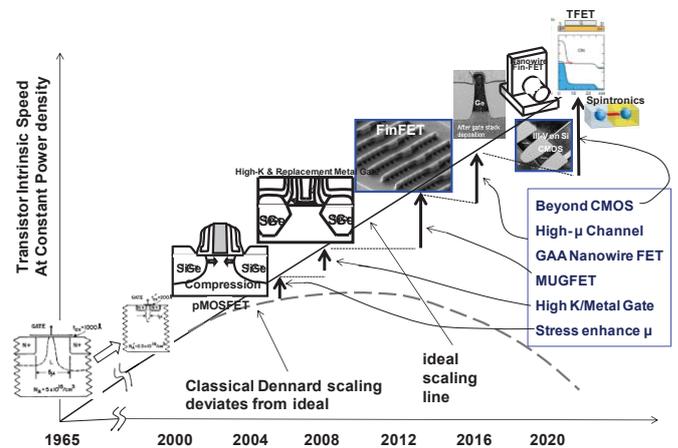


Fig. 1 transistor architecture trend chart [3]

These transistor performance enhancements have also increased process complexity significantly. In addition to geometry and profile engineering, the mechanical stress and its electrical response became an integral part of what determines the device behavior. TCAD quickly expanded beyond electrostatic and doping profile simulations.

The first TCAD expansion is in prediction of transistor characteristics with engineered stress or strain. The simulation of process induced stress has gone through several improvements. It was pointed out that accurate accounting of stress, even in planar devices, needs rigorous 3D simulations [21-22]. Then the influence of multiple process steps on stress, such as stress memorization and stress enhancement by gate material replacement, were simulated [23-24]. In addition, to understand and predict many of the process induced stress technologies, atomistic level simulations may be needed. One example is the simulation of the formation of dislocation which can serve as a source to generate tensile channel stress [25].

Figure 2 illustrates the use of molecular dynamics simulations to predict the formation of dislocations and the resulting stress profile.

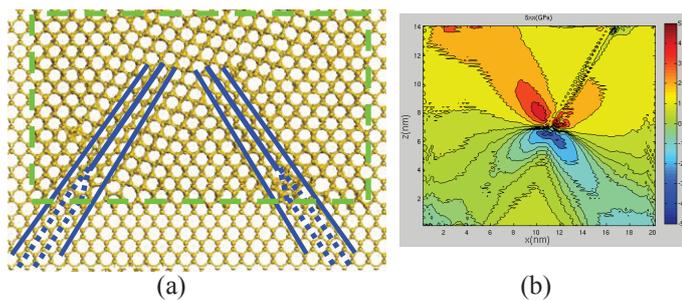


Fig. 2 (a) MD simulation result of SPER process with applied external stress (b) The MD simulation stress contour induced by a SMT dislocation [25]

The second TCAD expansion is to simulate high-K dielectric and metal gate (HK/MG). The challenge is to engineer the gate stack to achieve targeted  $J_g$ , DIT, mobility, and suitable Wf. Opportunity to greatly reduce development time and cost if the vast process space can be screened by simulations and material choices can be narrowed down. Indeed, some success in leveraging ab-initio simulations to study gate stack have been reported, for instance, in predicting influence of impurities on effective work functions [26-27], in predicting the dipole formed at the silicon oxide and high K material interfaces [28], and in predicting other gate stack related properties such as NBTI [29]. Figure 3 shows an example of ab-initio model of the HfO<sub>2</sub>/SiO<sub>2</sub> interface for eWf predictions.

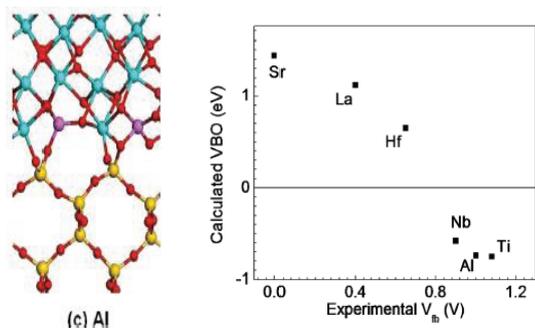


Fig. 3 On the left is the atomic structure of incorporating Al at HfO<sub>2</sub>-SiO<sub>2</sub> interface. On the right is the calculated VBO vs experimental Vfb showing a monotonic correlation [28]

The third TCAD expansion is simulation of multi-gate devices. There are many challenges, for instance, to correctly simulate a FinFET requires models to account for transport on the side wall of the FinFET which is typically close to (110) surfaces. In the realistic case, the side wall channel could be sloped off vertical (110) direction, and the channel stress can be different from simple uni-axial stress and may consist of several non-zero components. The mobility stress response may not be accurately represented by a simple linear combination of response to individual stress components, such

as reported in [30-31]. Figure 4 illustrates the complex stress dependent on different surface orientations.

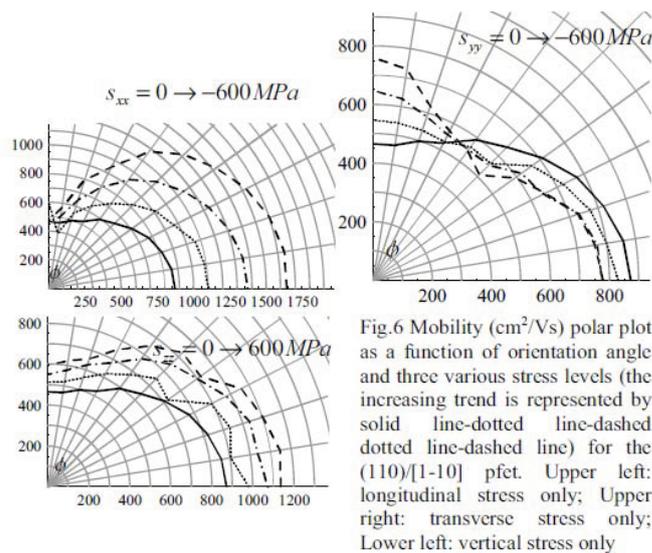


Fig. 4 Hole mobility polar plots for (110)/[1-10] in response to three stress components [30]

From planar to FinFET, another change is inversion layer quantization. When the fin width is scaled down, the inversion layer quantization deviates from triangular well approximation and gets into volume inversion determined by geometrical confinement.

The inversion layer mobility along the side wall channel of FinFET can be simulated by a double gate structure. Multi Sub-bands Monte Carlo device simulations show that the mobility on the FinFET sidewall channel starts to significantly deviate from that of single gate on the same surface orientation, as illustrated in Figure 5 [32].

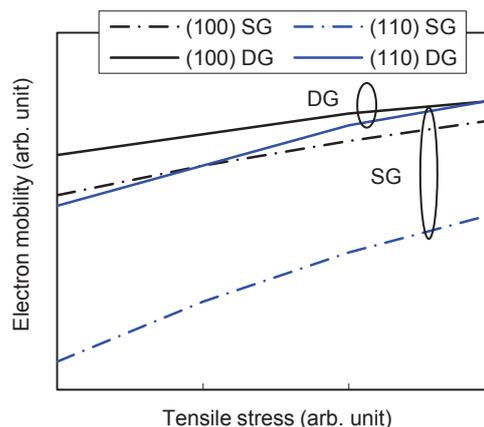


Fig. 5 Volume inversion affecting inversion mobility becomes prominent in FinFET [32]

The quantization effect becomes even more pronounced in nano-wire transistors. More new physics need to be considered arising from nano-wire's 1D nature of carrier transport [33-34]. Nano-wire transistor structures display much better SCE control and thus allow more aggressive channel length scaling.

However, at extremely scaled channel length, source to drain tunneling current can no longer be neglected. Consideration of tunneling is important to correctly predict device performance, as reported in [34] and shown in Figure 6.

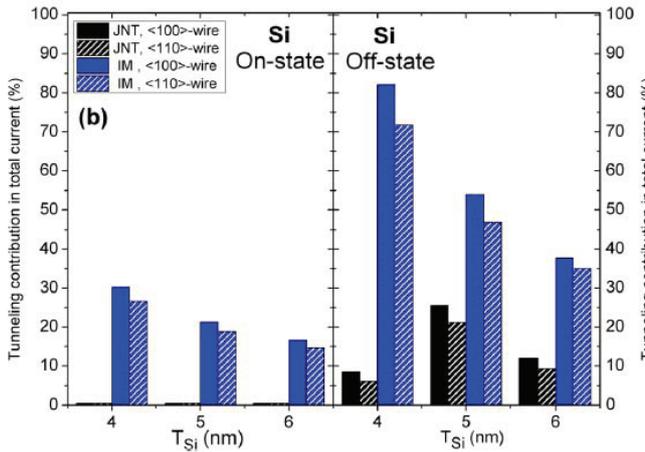


Fig. 6 Significant source to drain tunneling current [34].

### B. New materials and atomistic modeling

To further enhance device performance, there are two paths being explored. One path pushes toward higher mobility by engineering the channel material, and the other leverages a new gate switching mechanism such as tunneling FET to push the sub-threshold swing below the thermal limit of 60mV/dec. Well calibrated predictive TCAD simulations can provide tremendous value in assessment of both paths. Good progress in simulating both the nano-wire transistors with various channel materials and the TFET with exotic junction designs were reported [35-38]. Evidently, simulations including rigorous quantum mechanics at atomistic level show promise with simulations in good agreement with experiments without much empirical fitting [37]. Figure 7 shows examples of atomistic simulations of TFET devices.

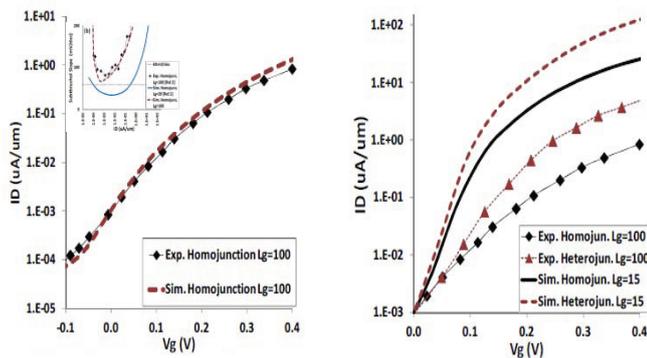


Fig. 7 On the left, TFET simulations validated to experiments. On the right, scaled TFETs are predicted to performance better than scaled MOSFETs [37].

### C. Beyond charge logic

As long as electric charge is used as the logic state variable, Zhimov et al. pointed out that energy reduction will hit a lower bound dictated by the Heisenberg/SNL limit [39]. To move

further down in energy consumption, new logic state variable other than charge needs to be explored. Spintronics, which uses spin to represent the logic states which also has the benefit of being non-volatile, holds promise to lower the switching energy [40-43]. The simulation of spin based devices [44-45] presents another area of expanding usage of TCAD.

## III. EXPANDING TCAD ROLE THROUGHOUT R&D STAGES

### A. Exploratory and path finding stage

R&D cost continues to rise due to the increasing complexity of processes. In the early exploratory stage of a new technology node, companies face tough decisions to choose from a multitude of technology choices. It is rarely the case to have enough experimental data at this stage to help narrow down technology choices. Therefore TCAD, with proper physical models, if applied to pre-screen and help down select, bringing tremendous value to R&D. Atomistic ab-initio simulations became feasible due to the extremely scaled dimensions and the availability of vastly higher computing power. As shown earlier, atomistic simulations have been useful in assess performance potentials of the intrinsic device. However, when incorporated in the integrated circuit with real processes, many parasitic components surrounding the intrinsic device have to be considered together as a whole device system. A hierarchical approach may need to be adopted. One may simulate the intrinsic device or new channel material using full atomistic models, then capture these in a semi-classical Monte Carlo simulator. The MC simulation results can further be used to calibrate continuum device simulator which can then be used to make assessment of realistic device structures. This approach may be illustrated schematically in Figure 8.

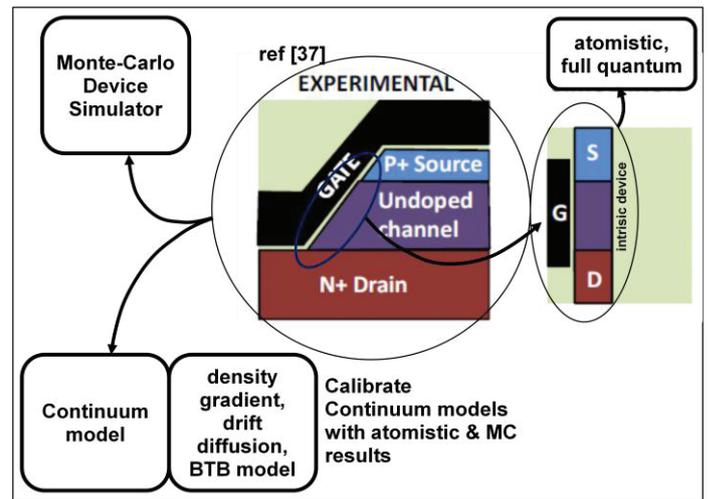


Fig. 8 Hierarchical approach combines atomistic simulations → MC simulations → continuum simulations.

### B. Development stage

Beyond assisting in diagnoses of experimental results using TCAD simulations, accurate prediction of results from process changes is very valuable. In addition to solid models and pre-planned calibration to SIMS, it is often desirable to generate predictive continuum model quickly with no existing data for calibration. Leverage KMC is showing promise [46-48]. The

defect-dopant cluster and reaction rate can be simulated. A hierarchical approach can be useful, as shown in Figure 9 [49].

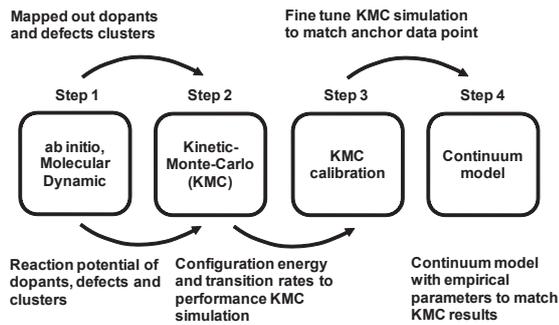


Fig. 9 A hierarchical approach for process simulations [49].

### C. Production stage

In the production stage, quick turn prediction to guide experiments and process changes is highly valued. It is possible to combine TCAD simulation results and DOE experimental data to build a RSM to serve this purpose. Such approach has been reported earlier [50]. The importance of controlling variability has become increasingly important with scaling. The first step to control variability is to simulate it. Progress in modeling of local variations has been reported steadily since RDF (random dopant fluctuation) was brought into attention [51-53]. Monte Carlo stochastic approach is commonly used to estimate  $V_t$  mismatch sigma, however, a large number of simulations are needed to reach desired accuracy [54]. A deterministic approach allowing relative  $V_t$  variation comparison for process optimization purposes may be a desirable alternative [55]. Progress in variability simulations of FinFET and nano-wire transistors has also been reported recently [56-57]. SRAM yield and  $V_{ccmin}$  is largely determined by both local and global variability. Ultimately, SRAM yield and circuit corner performance may be predicted and optimized by the assistance of TCAD simulations.

## IV. CONCLUSIONS

Technology scaling presents abundance of opportunities where TCAD can make significant contributions. However, considerable development effort is required to bring new physics into TCAD tools. Expanding role of predictive TCAD is expected, which will span to atomistic, full quantum mechanical simulations, as well as TCAD based quick turn simulation models, SRAM and circuit applications. We expect TCAD to become an essential part of strategy for companies to contain R&D cost and continue timely delivery of new technology nodes.

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