Technology CAD challenges of modeling multi-gate transistors

Cory Weber, Dipanjan Basu, Roza Kotlyar, and Saurabh Morarka
Process Technology Modeling, Intel Corporation, Hillsboro, Oregon 97124
Email:cory.e.weber@intel.com

***Abstract*—As the economics of Moores law drives transistor feature scaling, multiple gate devices such as Tri-gate and FinFET transistors have been adopted to control short channel effects. As the device pitch is scaled, traditional strain engineering methods lose effectiveness and parasitics can increase, forcing technologists to evaluate disruptive solutions. Moreover, many local continuum models can no longer accurately describe device behaviour at these scaled dimensions and more advanced models must be adopted to guide process and device development. The challenges of present and future multi-gate device development and the role of technology computer aided design in addressing those challenges are discussed.**

To reduce die size and thus product costs according to Moore's law CMOS technologists are driven to shrink device pitch. In addition to die size concerns, the ability to operate at low supply voltages is critical for low power products. In response to these concerns, semiconductor companies are moving to multi-gate gate field-effect transistors(MuGFETs) [1], which offer advantages for scaled gate lengths and supply voltages [1]–[3].

Developing a MuGFET process technology requires significant technology computer aided design(TCAD) simulation involvement, as illustrated in Fig. 1. TCAD simulations are used to help downselect device architecture and process options in the initial stages of development. As experimental data becomes available it is compared with simulation predictions and differences between the experiment and simulations are characterized. After the differences are understood, the entire cycle repeats incorporating the new experimental learning. The TCAD simulations must be fast so they do not become a bottleneck for process development, yet still capture the key physics needed to guide development. For model developers, this may mean running more expensive, first principles simulations to understand a problem, then developing a more compact solution to be implemented in the day to day simulation framework.

Source/drain(S/D) dimensions have scaled drastically over the the past four technology generations leading to some loss of channel stress for devices with epitaxial SiGe source/drain stressors. This scaling penalty can be offset by increased Ge mole fraction [4], as seen in Fig. 2. Continuing this trend in mole fraction will be challenging, as it is difficult to grow high mole fraction SiGe films without dislocations, and other exotic materials like GeSn would be needed to push stress beyond the 100% level. It is clear that mobility enhancement solutions other than source/drain stressors should be evaluated, such as alternate channel materials that have demonstrated enhanced mobility for both NMOS [5]–[7] and PMOS [8] devices. TCAD models need to be ready for new processes and devices with these materials.

New channel materials have their own problems. For example, SiGe channels typically have defective insulator interfaces, requiring a Si capping layer to maintain interface quality [8]. With the introduction of heterostructure channels to MuGFETs, local quantum corrections to carrier profiles may no longer be valid, and more expensive non-local simulations may be needed to accurately predict the carrier concentrations. Figure 3 shows electron profiles for a long channel double-gate SiGe channel device with Si cap layers. The local quantum correction often used in drift-diffusion simulations [9] was not intended for heterointerface channels, and gives a poor fit to the full Schrödinger-Poisson solution. Hybrid approaches using 2D slice samples with the Schrödinger solution may be used to balance accuracy with computational efficiency.

Another way to improve MuGFET performance is to reduce the dimension in the confinement direction [2], [3], improving subthreshold slope and threshold voltage. However, mobility and external resistance(R_{ext}) may degrade at these scaled dimensions, and TCAD models need to capture these effects to help experimentalists design optimal MuGFET devices. Figure 4 shows simulated mobility changes with fin/wire width. For electrons, the mobility degrades as width is scaled due to surface roughness effects [10]. For holes, improvements due to non-parabolicity compete with surface roughness [11], resulting in non-monotonic trends. Interface scattering may also play a significant role in the S/D extensions, degrading R_{ext}. Figure 5 shows the electron mean free path calculated from mobility vs. doping curves [12] for silicon. For typical S/D extension dopings of $\sim 10^{20} cm^{-3}$, the mean free path is $\sim$2nm, suggesting non-local surface scattering [13] in the S/D extensions may need to be captured in the drift-diffusion framework for dimensions of $\sim$5nm.

Accurate process simulations are also important for predicting drive current as fin/wire dimensions are scaled. Figure 6a shows simulations of linear drive current vs. fin width(W_{Si}) for a Tri-gate device with two different S/D extension doping assumptions. Drive increases more than 15% as W_{Si} scales from 13nm to 6nm, provided the doping is constant in the width direction. However, if the doping experiences surface dose loss as illustrated in Fig. 6b, the drive current instead degrades 5% due to poor R_{ext}.

978-1-4673-5736-4/13/$31.00 ©2013 IEEE

REFERENCES

[1] C. Auth *et al.*, in *VLSI Sym. Tech. Dig.*, 2012, pp. 131–132.
[2] D. Frank, Y. Taur, and H. Wong, *IEEE EDL*, vol. 19, no. 10, pp. 385–387, 1998.
[3] D. Hisamoto *et al.*, *IEEE TED*, vol. 47, no. 12, pp. 2320–2325, 2000.
[4] K. J. Kuhn *et al.*, in *IEDM Tech. Dig.*, 2012, pp. 8.1.1–8.1.4.
[5] J. Oh *et al.*, in *VLSI Sym. Tech. Dig.*, 2010, pp. 39–40.
[6] A. Toriumi *et al.*, *IEDM Tech. Dig.*, pp. 28.4.1–28.4.4, 2011.
[7] M. Radosavljevic *et al.*, in *IEDM Tech. Dig.*, 2011, pp. 33.1.1–33.1.4.
[8] S. Verdonckt-Vandebroek *et al.*, *IEEE TED*, vol. 41, no. I, 1994.
[9] W. Hänsch *et al.*, *Solid-State Electron.*, vol. 32, no. 10, pp. 839–849, 1989.
[10] R. Kotlyar *et al.*, *APL*, vol. 84, no. 25, p. 5270, 2004.
[11] R. Kotlyar *et al.*, *JAP*, vol. 111, no. 12, p. 123718, 2012.
[12] G. Masetti, M. Severi, and S. Solmi, *IEEE TED*, pp. 764–769, 1983.
[13] K. Fuchs, *Proc. Cambridge Phil. Soc.*, vol. 34, p. 100, 1938.

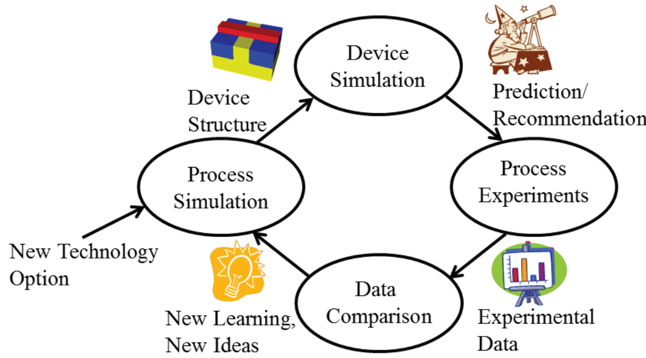

Fig. 1. TCAD involvement in the process technology development cycle.

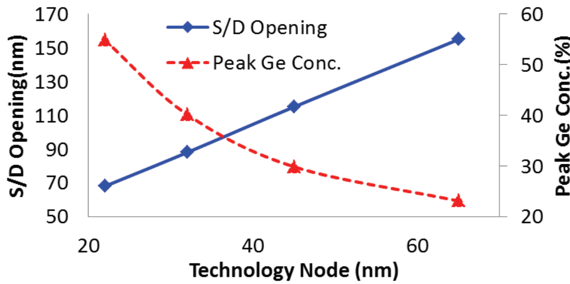

Fig. 2. Source/drain opening dimensions for the last 4 nodes of Intel logic technology, and Ge concentration in the PMOS S/D for those nodes [4].

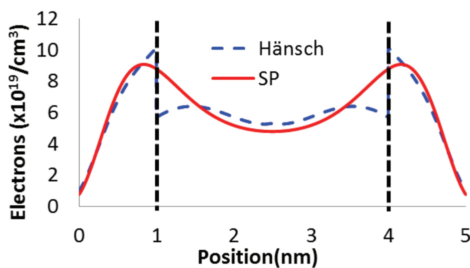

Fig. 3. Electron profiles for a long channel double gate device with a <1nm Si/3nm SiGe/1nm Si> stack. Cases shown are the quantum correction by Hänsch [9] but generalized to 3D, and the full Schrödinger-Poisson solution. V_g =1V, EOT=0.8nm, and Ge mole fraction=50% for both simulations.

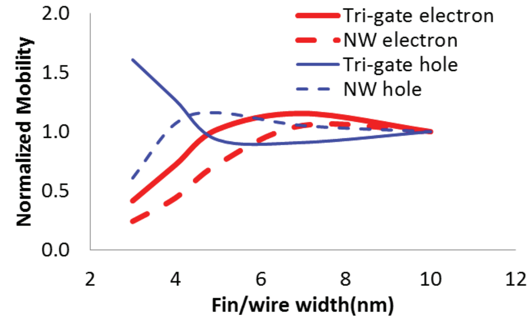

Fig. 4. Simulations of mobility vs. width for fins and wires. Effective mass k.p simulations are used for electrons, and sp3d5s* tight binding for holes. Surface roughness, acoustic, and optical phonons are included. The wires are square and the fins are 30nm tall.

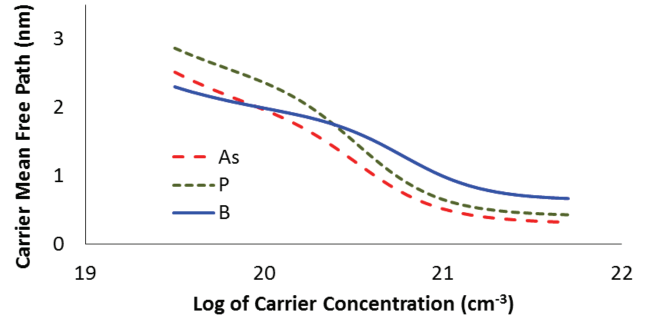

Fig. 5. Silicon carrier mean free path in highly doped S/D extensions as a function of doping.

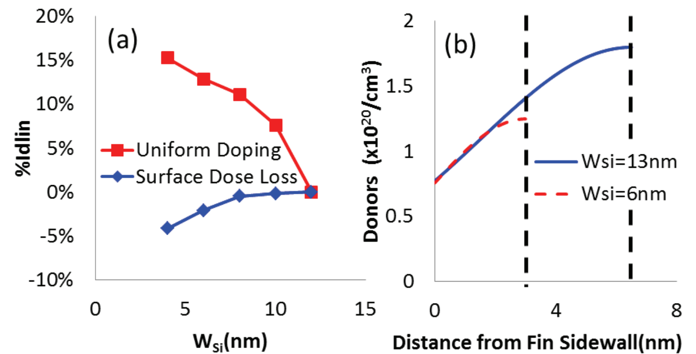

Fig. 6. (a) Simulated NMOS Tri-gate linear drive current($V_{ds} = 50mV$, $V_{gs} = 0.7V$) change vs. W_{Si} for a doping profile that is uniform in the width direction, and one that loses dose from fin sidewalls. (b) S/D doping profiles in the width direction for the surface dose loss case. Workfunction is optimized so that S/D leakage current is 5nA/μm for all devices.