Novel Design of Multiple Negative-Differential Resistance (NDR) Device in a 32nm CMOS Technology using TCAD

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***Abstract*—We propose a novel multiple negative differential resistance (NDR) device with the positive inclined tri-state voltage transfer characteristics (VTC) between drain and gate of 32nm *n*-type MOSFET based on gate-induced drain leakage (GIDL) enhanced off-state CMOS ternary inverter. The ultra-high 1st and 2nd peak-to-valley current ratio (PVCR) over 10^4 can be designed with high slope of inclined ternary VTC by increasing the GIDL effects.**

***Keywords*—Negative differential resistance (NDR), voltage transfer characteristics (VTC), gate-induced drain leakage (GIDL), peak-to-valley current ratio (PVCR)**

I. INTRODUCTION

The negative differential resistance (NDR) is innovative device for multi-valued logic (MVL) and memory (MVM) applications owing to its nonmonotoic behavior. In order to increase bit density per unit memory circuits, the multiple NDR devices have lots of attention [1]. Since the first discovery of NDR characteristics in Esaki tunnel diode [2], the *pn* quantum tunneling diode and resonant tunneling diode (RTD) which have received most attention as alternative NDR devices, however, have been in problem for practical application owing to its low peak-to-valley current ratio (RVCR) and not compatible with CMOS technology, respectively [3-4]. Recently, many researches have been introduced NDR device based on CMOS circuits to overcome the former limits [5-6]. Even though some researches succeed to obtain high PVCR by suppressing peak current at off current (I_{off}) level of MOSFET in single-peak NDR device, the multiple NDR device for MVL and MVM has not been achieved the advantage of bit density, owing to its complicated circuit/device structure [7-8]. In this paper, we propose a novel multiple NDR devices with an enhanced gate-induced drain leakage (GIDL) effect and confirm its process compatibility with 32-nm CMOS technology.

II. OPERATION PRINCIPLE OF MULTIPLE NDR DEVICE

Figure 1(a) shows the circuit scheme of MOS-NDR devices composed with inverter (*Mp*1 and *Mn*1) and *n*MOS (*Mn*2). The *Mn*2 follows 32-nm CMOS technology of ITRS [9] while both

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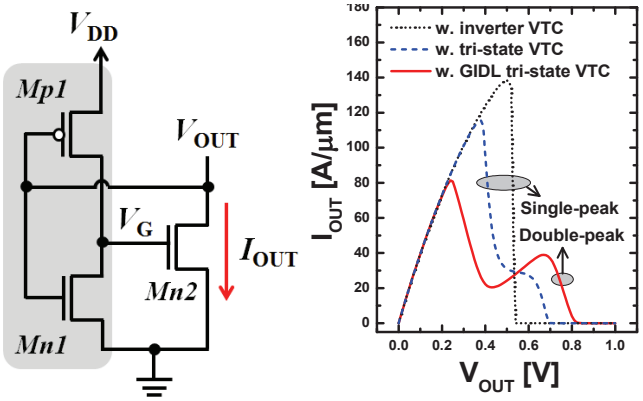

(a) (b)

Fig. 1. (a) Proposed NDR circuit scheme and (b) its I-V curve according to various voltage transfer curve (VTC). Inverter VTC and tri-state VTC have single peak NDR characteristics and tri-state VTC with GIDL effect has double peak NDR characteristics.

*Mp*1 and *Mn*1 would be modified in order to obtain various NDR characteristics having process compatibility. According to the voltage transfer characteristics (VTC: V_G-V_{out}) from *Mp*1 and *Mn*1, *Mn*2 has various I_{out}-V_{out} curves as shown in Fig. 1(b). When the inverter is designed with normal 32-nm CMOS technology, single NDR characteristic with fully suppressed valley current at half of supply voltage (V_{DD}) is obtained as dot line from binary inverted V_G [10]. On the other hand, in case that gate voltage (V_G) has tri-state VTC with additional high impedance intermediated state by using subthreshold region of *n*/*p*MOS, I_{out} is suppressed through the two steps (dashed line). At here, GIDL effect is added at both *Mp*1 and *Mn*1, double-peak NDR characteristic can be obtained as solid line. Therefore, by designing VTC with conventional inverter circuits, various NDR characteristics of *Mn*2 could be obtained.

Figure 2 shows the VTC used in Fig. 1(b). By increasing threshold voltage (V_{th}) with highly doped channel, intermediate state can be obtained with voltage dividing between series resistance of off-state *Mn*1 and *Mp*1 (R_{Mn1_off}/R_{Mp1_off}) as

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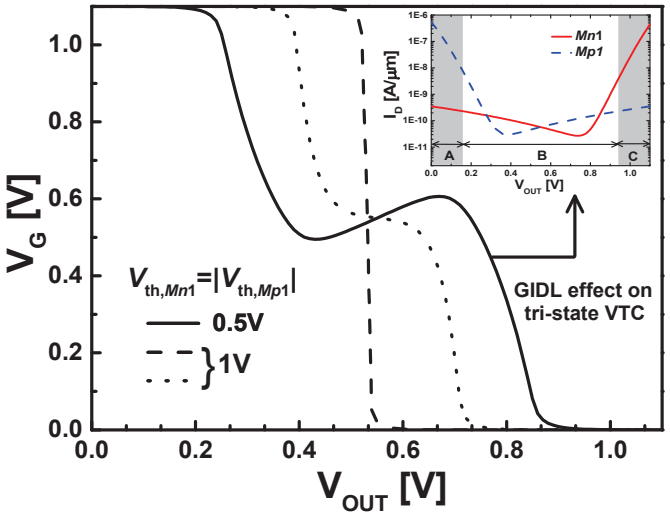


Fig. 2. Voltage transfer curve (VTC) at $V_{th,Mn1}$=|$V_{th,Mp1}$|=0.5V and 1V. GIDL effect makes inclined tri-state VTC with inserted *I-V* characteristics of *Mn*1 and *Mp*1.

V_{out}=[R_{Mn1_off}/(R_{Mn1_off}+R_{Mp1_off})]xV_{DD}. When the GIDL effects included, the I_{off} cannot hold out constant, so that GIDL current (I_{GIDL}) make positive inclined VTC. The inset of Fig. 2 illustrates the I_D-V_G characteristics of *Mn*1 and *Mp*1 for inclined VTC. When one-side current is much larger than that of the other as regions of A and C, 1.1V (V_{DD}-state) and 0V (GND-state) are transferred, respectively. On the other hand, current difference is lower than one order as region of B, voltage dividing between *Mn*1 and *Mp*1 directly influence on VTC.

III. Design Methodology for GIDL Enhanced CMOS Inverter Based on 32-nm CMOS Technology

Figure 3 shows the 32-nm CMOS technology structure and its band-to-band generation compared with our proposed GIDL

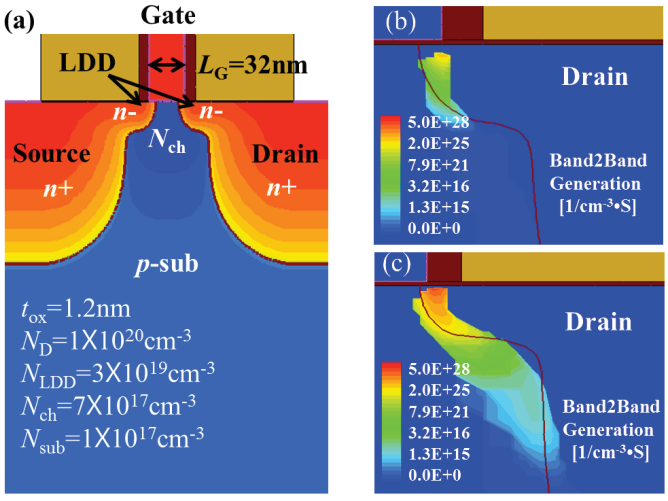


Fig. 3. (a) *n*MOS schematic and (b) band-to-band generation view by using 32-nm CMOS technology structure. (c) Band-to-band generation with our enhanced condition

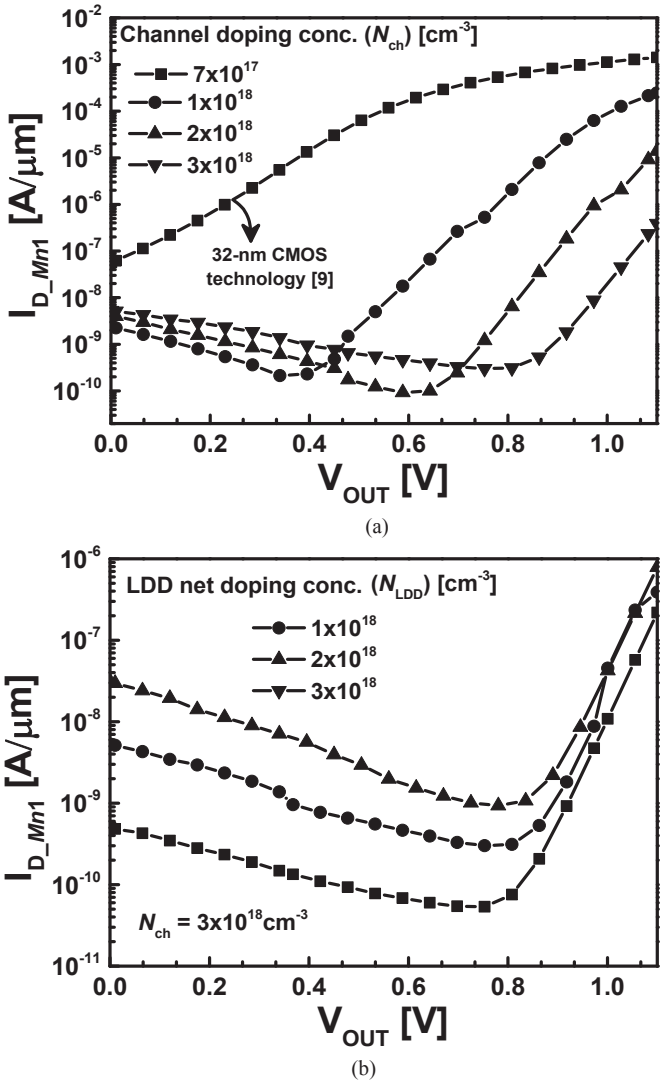
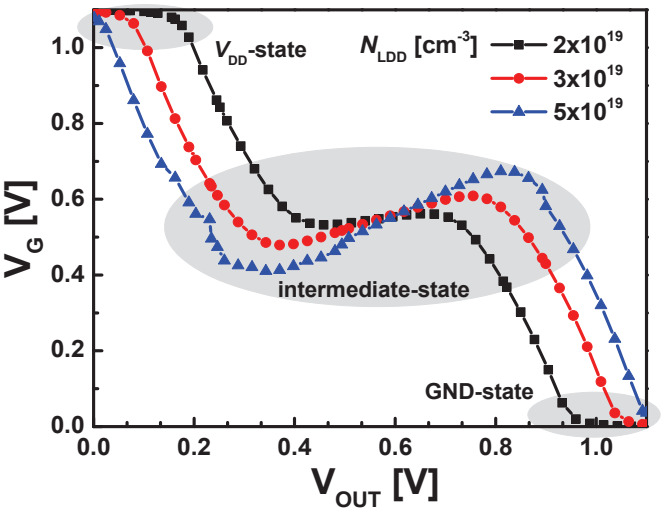
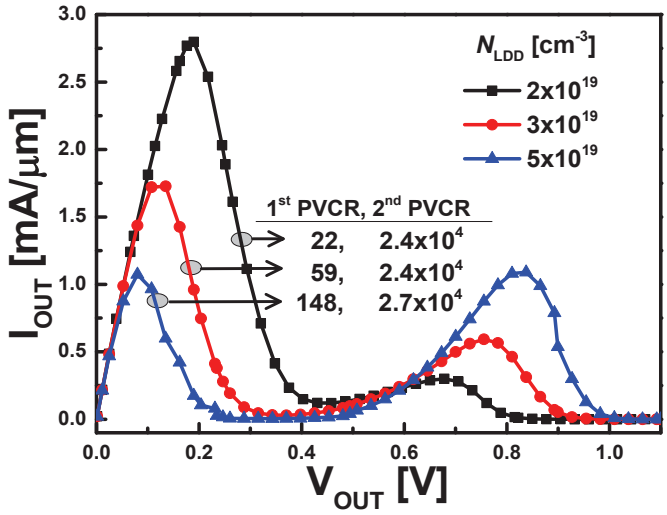


Fig. 4. I-V characteristic of *Mn*1 according to (a) various channel doping concentration (N_{ch}) and (b) net doping concentration of lightly doped drain (N_{LDD})

enhanced structure at V_G=0V. The 32-nm CMOS technology structure has gate length (L_G) of 32nm, oxide thickness (t_{ox}) of 1.2nm, doping concentrations of source and drain (N_D) of 1x10^{20}cm^{-3}, lightly doped drain (LDD) region (N_{LDD}) of 3x10^{19}cm^{-3}, substrate (N_{sub}) of 1x10^{17}cm^{-3}, and channel (N_{ch}) of 7x10^{17}cm^{-3} (Fig. 3(a)). In order to obtain GIDL effect between 0V and 1.1V (V_{DD}), proposed device is designed with N_{ch} of 3x10^{18}cm^{-3}. As shown in Fig. 3(c), proposed device has much higher band-to-band generation rate at the gate overlapped drain region compared with normal 32-nm CMOS technology (Fig. 3(b)). The simulations were performed by using *Sentaurus*^{TM} TCAD device simulator [11]. Figure 4 shows the *I-V* characteristics of *Mn*1 according to the design parameters of N_{ch} and N_{LDD}. As N_{ch} is increased from 7x10^{17}cm^{-3} to 3x10^{18}cm^{-3} in order to obtain inclined tri-state VTC, the GIDL effects relatively decrease owing to offset from reverse-biased *pn* junction band-to-band tunneling (BTBT) as Fig. 4(a), which is also indicated in Fig. 3(c) with extended junction BTBT

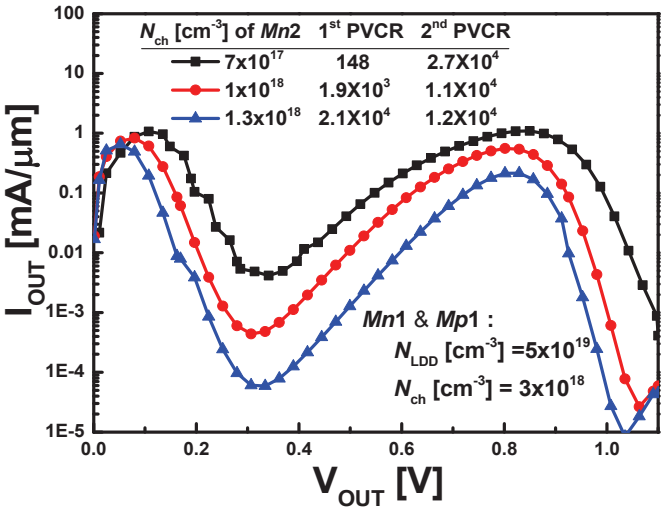


(a)

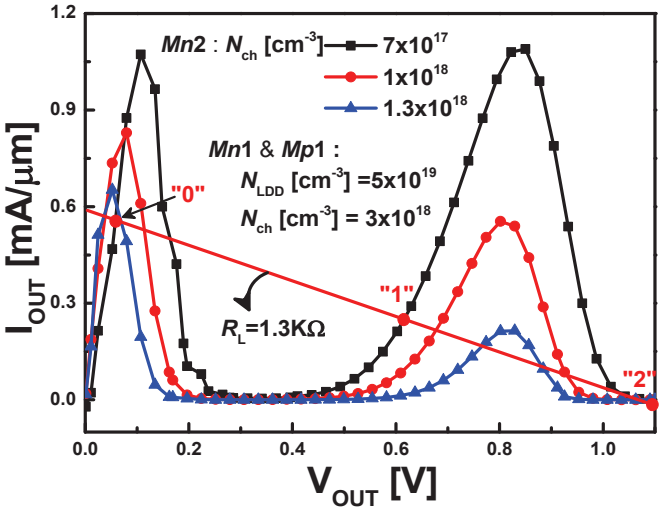


(b)

Fig. 5. (a) VTC and (b) multiple NDR characteristics according to various N_{LDD}. As N_{LDD} increase, VTC has steeper change so that higher 1st and 2nd PVCR and 2nd peak current are obtained.



(a)



(b)

Fig. 6. Multiple NDR characteristics according to various N_{ch} of *Mn*2: (a) log scaled *I-V* curve with table about 1st and 2nd PVCR and (b) linear scaled *I-V* curve with load resistance (R_L) for MVL and MVM. As N_{ch} increased, 1st and 2nd peak decrease and 1st PVCR increased.

region compared with Fig. 3(b). This reduction of GIDL effects can be supplemented by highly doped N_{LDD} even though junction BTBT also increased as shown in Fig. 4(b).

IV. Results and Discussion

By using the *I-V* characteristics of Fig. 4(b), mixed-mode device simulation with BTBT model was performed to verify the multiple NDR characteristics [11]. Figure 5 shows the various VTC from symmetrical GIDL-enhanced *Mn*1 and *Mp*1 and its corresponding double-peak NDR characteristics of *Mn*2 only by changing N_{LDD}. In the Fig. 5(a), when GIDL effects increased with highly doped N_{LDD} of 5x10^{19}cm^{-3}, the inclined intermediate state of VTC is extended with steeper change, while regions for GND- and V_{DD}-states are decreased owing to little change of max drain current in *Mn*1 and *Mp*1 (Fig. 4(b)). In the multiple NDR characteristics of Fig 5(b), it should be noted that I_{out} can increase again due to the increase of transferred V_G in the intermediate region of VTC whereas decrease of V_G makes NDR region. Therefore, the more inclined VTC can improve both 1st/2nd PVCR and 2nd peak current.

Figure 6 shows the multiple NDR characteristics according to *Mn*2 characteristics. By increasing N_{ch} of *Mn*2, both 1st and 2nd PVCR over 10^4 can be obtained with small reduction of 1st and 2nd peak currents as shown in Fig. 6(a). Increase of V_{th} allows *Mn*2 operates at the linear region of MOSFET so that 1st PVCR can be innovatively improved whereas 2nd PVCR has small reduction owing to lower on currents compared with saturation state of MOSFET. Moreover, our NDR device has possibility of tri-state logic having three stable operating points at marked "0", "1", and "2" with simple monotonic load resistance (R_L) as solid line in Fig. 6(b) [1]. Therefore, double

peak NDR device can be obtained by designing VTC with GIDL-enhanced *Mn*1 and *Mp*1 and its 1st and 2nd PVCR are explosively enhanced with V_{th} adjustment, which can be controlled by design parameters such as N_{ch} and N_{LDD}.

V. CONCLUSION

Novel multiple NDR device has been proposed based on voltage transfer circuit composed with *n/p*MOS and additional *n*MOS in a 32nm CMOS technology. The voltage transfer circuit with GIDL enhanced off-state CMOS transistors enables multiple NDR characteristics. By using mixed-mode TCAD device simulation, double-peak NDR with ultra-high 1st and 2nd PVCR over 10^4 based on 3 MOSFETs has been successfully demonstrated having the compatibility with 32nm CMOS technology.

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