Performance Evaluation of p-channel FinFETs using 3D Ensemble Monte Carlo Simulation

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***Abstract*— The impact of alternative channel materials in p-channel FinFETs is considered here using a combination of 3D drift diffusion and ensemble Monte Carlo simulations. This simulation approach allows both the electrostatics and the drive current of these devices to be properly evaluated in determining the potential performance improvement that can be derived from these devices.**

Keywords—Monte Carlo, FinFET, Germanium, Silicon, SiGe, strain.

I. INTRODUCTION

While the scaling of the conventional 'bulk' MOSFET has driven the semiconductor industry for decades, a combination of low performance, intolerable levels of random dopant induced statistical variability and a corresponding increased leakage, coupled to issues with SRAM yield and reliability limits the further scaling of this architecture. As a result, Intel's adoption of FinFET technology at the 22nm CMOS technology [1] has invigorated the interest in multigate MOSFET optimization and scaling. In addition to this the use of high mobility materials in place of conventional Si has gained an increased interest to further boost performance, with Ge and SiGe alloys [2],[3] strong candidates for p-channel transistors. The FinFET architecture lends itself to further enhancement via both uniaxial and biaxial strain and the exploitation of alternative surface orientations for the channel.

In this paper we study a 20nm gate length p-channel SOI FinFET, and consider the impact of scattering, strain and high mobility channel materials on the device performance, giving an indication of relative impact each element has in this architecture.

II. SIMULATION METHODOLOGY

To study this architecture the 3D device simulator GARAND [4] has been employed, with has both drift diffusion (DD) and ensemble Monte Carlo (MC) modules. The MC simulator uses a 6-band k•p approach to describe the valence bandstructure [5] that includes the impact of spin orbit interaction and strain. A full band approach is essential for hole transport in order to properly capture the warped nature of the valence band and the resulting influence on transport.

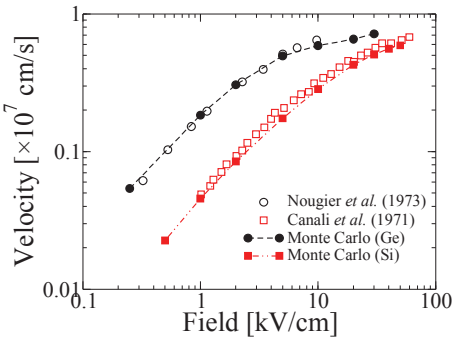

Fig. 1. Hole velocity as a function of applied field in undoped Si and Ge at 300K, compared to experimental data from [8],[9].

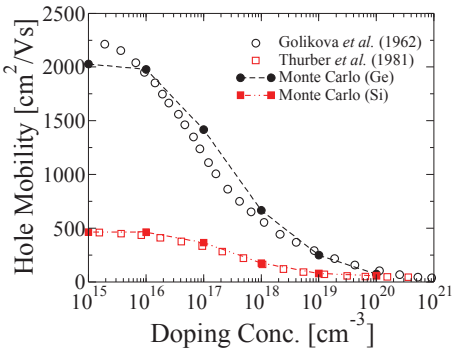

Fig. 2. Hole mobility as a function of doping concentration in Si and Ge, compared to experimental data from [10],[11].

Scattering from inelastic dispersionless optical (IOP) and acoustic (IAP) phonons using a full dispersion relation, ionized impurities (II) using Ridley's Third Body approach and surface roughness (SR) following Ando's approach [6],[7] are all included. This model reproduces experimentally measured bulk velocity and low field mobility in bulk Si and Ge for undoped and doped samples as shown in Fig. 1 and Fig. 2 respectively.

Low field mobility in a MOS capacitor is also well captured via careful calibration of the SR scattering parameters – as shown in Fig. 3 for Si and Fig. 4 for Ge. In the latter case, the impact of SR scattering on mobility is demonstrated by considering initially only phonon scattering, where the bulk-like mobility is recovered at low effective fields, before the

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impact of degeneracy degrades mobility at higher fields. Introducing II scattering reduces the mobility at low effective fields, consistent with Fig. 2, but the most significant impact is seen when SR scattering is introduced, with the hole mobility is now of a similar magnitude to that observed in Si.

As shown in Fig. 5 the mobility for different surface and channel orientations in Si is recovered – this is important for accurate simulation of FinFET structures where the sidewall planes result in transport under the influence of different surfaces which can impact upon carrier mobility. For transport in SiGe, alloy scattering is included as well and as can be seen in Fig. 6 this is necessary to match measured bulk hole mobility for this material.

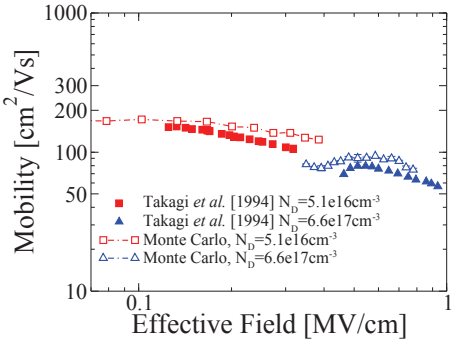

Fig. 3. Comparison of hole inversion layer mobility in Si from MC simulations compared to experimental measurements [12].

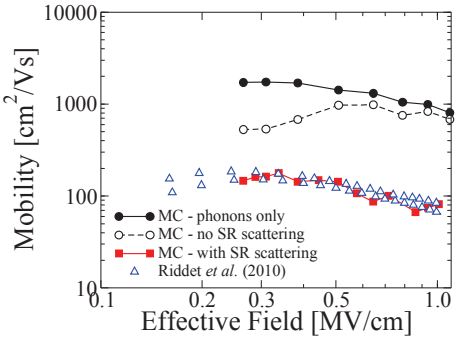

Fig. 4. Comparison of hole inversion layer mobility in Ge (N_D = 5e17 cm^{-3}) from MC simulations compared to experimental measurements [13].

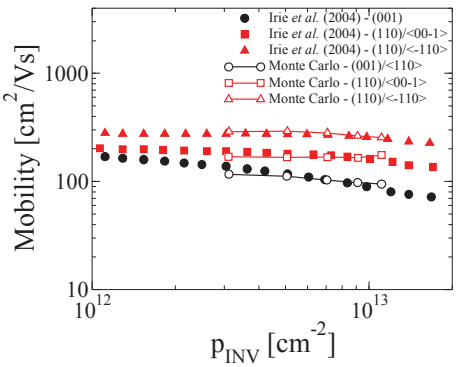

Fig. 5. Hole mobility as a function of inversion density for different substrate and channel orientations, compared to measurements from [14].

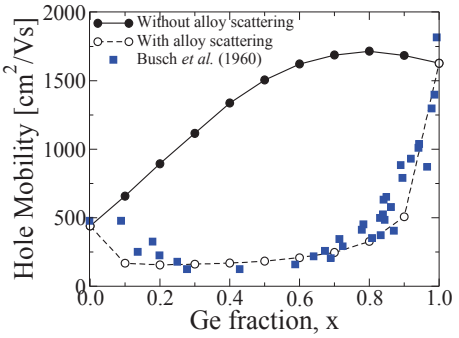

Fig. 6. Hole mobility as a function of Ge fraction for SiGe from experimental measurement [15] and MC simulation.

Additionally, Fermi-Dirac statistics are employed, with a correction applied to the inelastic scattering mechanisms following the approach in [16], and quantum corrections based on the density gradient approach are employed [17].

The inclusion of strain results in a further warping of the bands which under the correct conditions can strongly enhance hole mobility both in terms of transport (lighter conductivity mass) and scattering (via the modified density of states). Further, the normally energetically degenerate heavy and light hole bands are split by strain, which influences scattering and as a result the occupation of the different hole bands and this can in itself alter charge transport in the system.

In Fig. 7 the enhancement of hole mobility as a function of applied uniaxial strain along the ⟨110⟩ (parallel with field) for a Si inversion layer, with a (001) surface, showing a good agreement with measured data. The energy contours for the HH band in Si (Fig. 8) demonstrate the impact of strain on the bandstructure and thus the effective mass.

III. Device Architecture

In this work we consider Si, Ge and SiGe as channel materials in scaled p-channel FinFETs all with a substrate/sidewall surface/channel orientation of (001)/(110)/⟨110⟩, and all using an SOI FinFET design. A device schematic is given in Fig. 9, while the dimensions and doping concentrations are described in Table 1. An EOT of 0.8 nm is used, with high-k gate material employed in all cases.

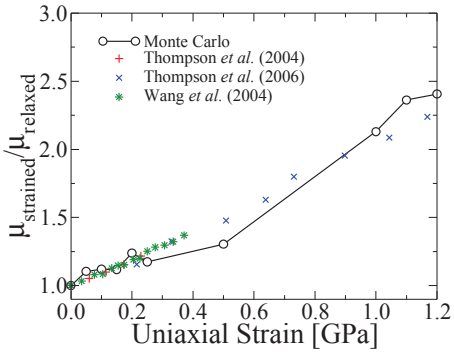

Fig. 7. Mobility enhancement in Si due to compressive uniaxial strain applied along the ⟨110⟩ direction for an effective field 0.7MV/cm, compared to measured data [18],[19],[20].

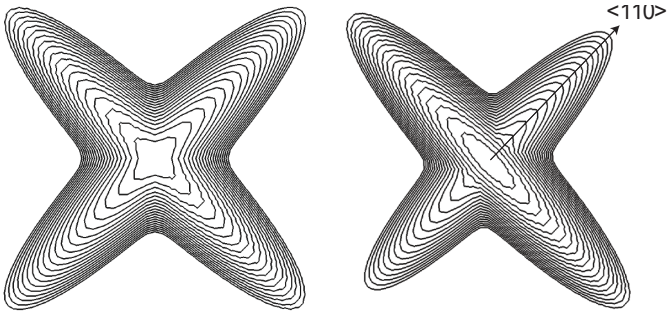

Fig. 8. Equi-energy contours for the HH band out to 0.25eV for relaxed (left) and strained (right) Si (1GPa, compressive, along ⟨110⟩).

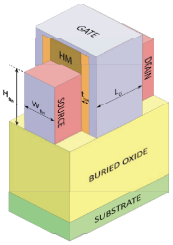

Table 1: FinFET dimensions.

Dimensions	
Gate Length [L_G]	20 nm
Fin Width [W_{fin}]	10 nm
Fin Height [H_{fin}]	25 nm
Doping	
Source/Drain	3×10^{20} cm^{-3}
Channel	1×10^{15} cm^{-3}
Substrate	5×10^{18} cm^{-3}

Fig. 9. Schematic of the FinFET device used in this study

IV. Relaxed Material Simulations

In Fig. 10 I_D-V_G characteristics for a 20nm gate length Si pFinFET are given as simulated using DD and MC. The DD case is shown before and after calibration of the mobility models to the MC characteristics, showing the limitations of this approach in terms of predictive simulations of potential device performance in terms of on current, though the subthreshold behaviour is well captured by both techniques. The underestimation of the hole velocity in the simple DD simulation shown in Fig. 11 before calibration of the mobility models confirms this.

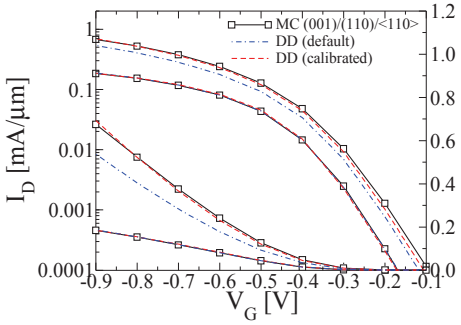

Fig. 10. I_D-V_G characteristics for a 20nm gate length Si p-channel FinFET from DD and MC simulation. DD results are shown using default mobility model parameters and after calibration.

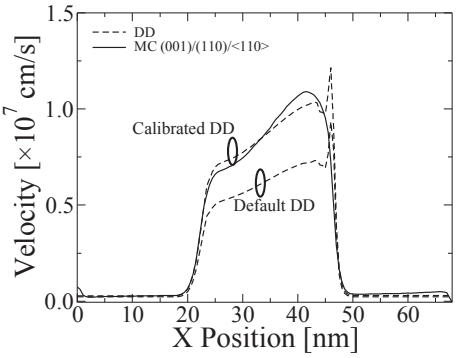

Fig. 11. Hole velocity from source to drain from MC (solid lines) and DD (dashed lines) simulation in the Si p-channel FinFET at V_D=V_G=0.9V. DD results are shown using default mobility model parameters and after calibration to MC results.

MC simulations of p-channel FinFETs employing Si, Ge and $Si_{0.5}Ge_{0.5}$ have been carried out at low (50mV) and high (0.9V) bias. The initial set of simulations neglect SR scattering in order to bracket the upper bounds of drive current resulting purely from the introduction of these materials, which is shown in Fig. 12. The influence of the significantly higher hole mobility (see Fig. 2) in Ge translates into a large gain in I_D over the Si device. However, the introduction of SR scattering significantly degrades this advantage, as demonstrated in Fig. 13, which is consistent with the strong drop in low field mobility observed in Fig. 4. For $Si_{0.5}Ge_{0.5}$ the strong effect of alloy scattering (see Fig. 6) results in poor device performance (Fig. 12), therefore the application of strain is required to make this material viable.

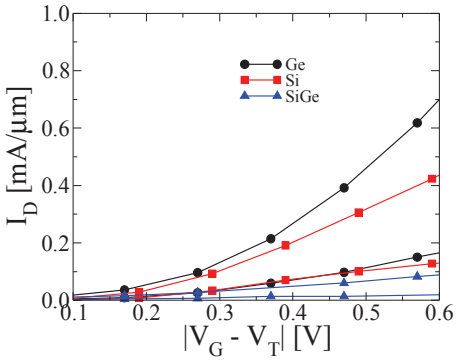

Fig. 12. I_D for Si, SiGe and Ge based FinFETs simulated without SR scattering.

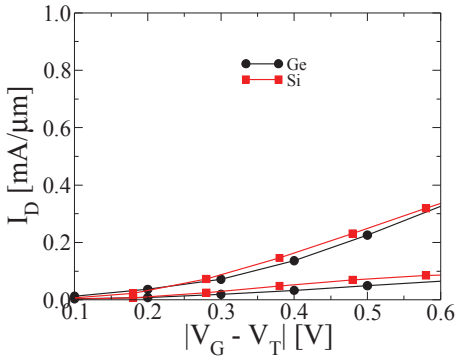

Fig. 13. I_D for Si and Ge based FinFETs with all sources of scattering.

V. Influence of Strain

The use of compressive uniaxial strain has been demonstrated to lead to significant enhancement in hole mobility and thus device performance [18]. Here we apply 1GPa along the ⟨110⟩ - this provides the 1.8 times mobility enhancement prescribed by the ITRS [21] as demonstrated in Fig. 7. As can been seen in Fig. 14, this mobility enhancement translates into a significant performance enhancement, effectively counteracting the impact of SR scattering for Si.

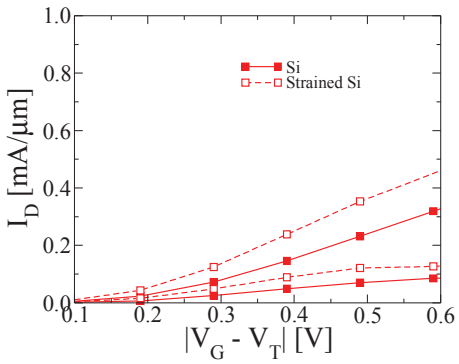

Fig. 14. I_D-for strained and relaxed Si FinFETs with all sources of scattering.

VI. Conclusions

In this paper we have used a 3D MC device simulator to study the on-current performance in a scaled p-channel FinFET. The models used in the simulator have been validated against experimental data, and the use of MC simulation over the simpler DD approach justified in terms of its greater predictive accuracy for drive current. Simulations have then been used to consider the impact of high mobility materials, surface roughness scattering and uniaxial strain on the on-current performance to give an indication of the potential performance of this device architecture.

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