Influence of the back-gate bias on the electron mobility of trigate MOSFETs

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***Abstract*—The influence of the back-gate bias on the threshold voltage and on the electron mobility of silicon trigate devices over ultra-thin-box is studied. The analysis confirms the possibility of achieving body factors higher than γ=0.1 as long as the channel width over height ratio is increased as much as possible. Also, the strong impact of the back-gate bias on the electron mobility is demonstrated using state-of-the-art scattering models for 2D confined devices.**

I. Introduction

The continuous reduction of device dimensions has focused the attention on non-planar devices such as trigate MOSFETs or Gate-All-Around Silicon nanowires (NWs). Therefore, the study of the transport properties of 2D-confined nanowires with sizes ranging in a few nanometers is a research field of high interest. On the other hand, low-power applications require dynamic control of the threshold voltage (V_T) to manage simultaneously power and performance. One potential solution is the back-gate biasing that modifies V_T due to the body effect. However, few works deal with this effect on multi-gate MOSFETs [1]-[4]. Moreover, most of them are focused on the body factor (γ) but they do not study the implications on the transport properties, which may be non-negligible, according to the results found for ultra-thin body SOI devices [5].

In this work, we analyze the behavior of trigate devices including back-gate bias as a function of the device dimensions, and we demonstrate its impact on the electron mobility (μ) using state-of-the-art scattering models for 2D confined devices. In Section II we introduce the numerical model employed to simulate the trigate devices. Section III presents the main results of this work. Finally, Section IV concludes the paper.

II. The model

Silicon trigate structures (Fig. 1) have been studied in this work. A midgap metal gate (Φ_m=4.61eV) is considered, and the gate and buried oxide (SiO_2) thicknesses are T_{ox}=1.2nm and T_{box}=10nm, respectively. The channel is oriented along the [011] crystallographic direction, being the top and bottom Si-insulator interfaces (100)-oriented, and the lateral ones (011)-oriented. Back-gate bias (V_{bg}) is applied beneath the buried oxide, as shown in Fig. 1. A rectangular silicon channel is simulated, being W_{Si} and H_{Si} the silicon width and height respectively.

The electrostatic simulation is performed by self-consistently solving the 2D Schrödinger and Poisson equations

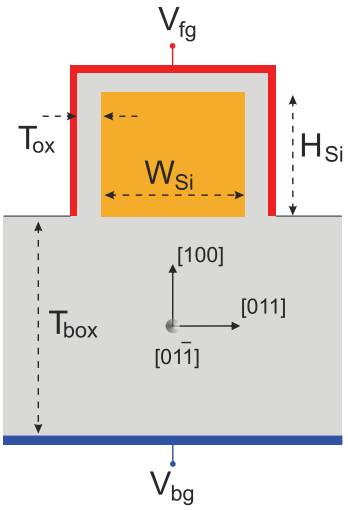

Fig. 1. Trigate SOI MOSFET geometry. The channel size is $W_{Si} \times H_{Si}$. T_{ox} and T_{box} are the front gate insulator thickness and buried oxide thickness, respectively. The channel is oriented along the [011] direction, and fabricated in a (100) wafer.

in a cross-section of the structure, under the anisotropic effective mass approach (EMA). The minimum channel width and height considered in this work is 5nm, making the EMA a good approximation [6]. The channel orientation has been taken into account rotating the effective mass tensor as proposed by Rahman et al. [7]. Also, non-parabolic corrections to the conduction band have been included [8], with a non-parabolicity factor $\alpha = 0.5$ eV^{-1}.

The electron mobility for each subband i has been calculated by means of the Kubo-Greenwood formula [9] as:

$$\mu_i = \frac{g_i e}{n_i 2\pi k_B T} \int_{-\infty}^{\infty} dk v_i^2(k) \tau_i(k) f(E) \left(1 - f(E)\right) \quad (1)$$

where n_i and g_i are the electron density and the degeneration of the i subband, $v_i(k)$ is the carrier velocity, $f(E)$ the Fermi occupation function and $\tau_i(k)$ the total momentum relaxation time, which is calculated by means of the Mathiessen's rule at each energy value. The total electron mobility can be calculated as:

$$\mu = \frac{\sum_i n_i \mu_i}{\sum_i n_i} \quad (2)$$

Bulk optical (OP) and acoustic (AP) phonons, surface-roughness (SR) and Coulomb (CO) scattering mechanisms

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are included in the simulations. Both SR and CO scattering mechanisms are implemented taking into account the tensorial dielectric screening [8], while the phonon interactions remain unscreened. The scattering mechanisms are introduced as described in [8], except for the SR, calculated as in [10], with $\Delta_{sr} = 0.5$nm and $L_{sr} = 1.5$nm. The surface charge value employed ($N_{it} = 4 \times 10^{12}$ cm^{-2}) is similar to that used in [11], where such a high value is needed to fit the experimental results.

III. Results and Discussion

A. Electrostatic results

First, the inversion charge (N_i) versus front gate voltage (V_{fg}) curves have been studied as a function of the back gate bias. Fig. 2 shows the results for a device with $W_{Si} = 5$nm and $H_{Si} = 5$nm. As can be seen, only the threshold voltage (V_T) is modified when V_{bg} changes, while the gate capacitance as a function of the overdrive gate voltage ($V_{fg} - V_T$) remains unaltered. As expected, negative values of V_{bg} increase V_T, as they reduce the overall potential in the channel, while positive ones decrease V_T.

The influence of the back-gate bias varies when different device widths are considered. This is due to a modification of the front-gate control on the back part of the channel. The overall behavior, however, is quite complex, as shown in Fig. 3, where different device widths are taken into account for a fixed device height, H_{Si}=5nm. When W_{Si} is raised, V_T slightly increases for negative values of V_{bg}, while it remarkably decreases for positive values of V_{bg}. To explain this behavior, the influence of the quantum confinement on the threshold voltage has to be taken into account. Hence, for negative V_{bg} values, there are two contributions that tend to cancel each other:

- First, the increase of the device width provokes a larger influence of the back-gate bias and thus, from a classical point of view, V_T should rise.
- Second, the wider the device, the lower the quantum confinement and therefore the lower its influence on the threshold voltage. In the absence of V_{bg}, this would cause a reduction of V_T for wider devices.

As for positive V_{bg} values, the higher influence of the back gate in wider devices tends to reduce V_T, adding up to the quantum confinement effect.

As already reported in [1], both the increase of W_{Si} and the decrease of H_{Si} are useful to augment the body factor, which is defined as

$$\gamma = \left| \frac{\partial V_T}{\partial V_{bg}} \right| \tag{3}$$

Fig. 4 depicts the body factor as a function of the channel width and height. As can be seen, for the values of T_{ox} and T_{box} considered in this work, γ values higher than 0.1 can be achieved. The body factor is closely related to the ratio between the channel-to-back-gate capacitance (C_{bg}) and the channel-to-front-gate capacitance (C_{fg}) [4]. Therefore, the use of Ultra-Thin BOX is critical to get such a high γ value.

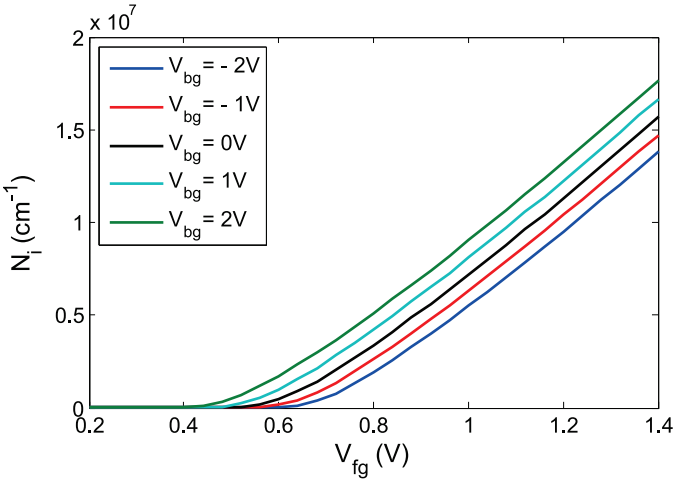

Fig. 2. N_i vs. V_{fg} in a device with $W_{Si} = H_{Si} = 5$nm, as a function of V_{bg} (ranging from -2V to 2V).

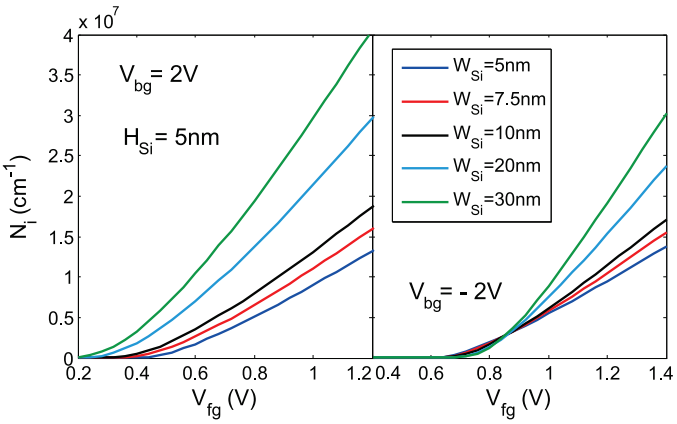

Fig. 3. N_i vs. V_{fg} in a device with $H_{Si} = 5$nm and variable silicon width: $V_{bg} = 2$V (left), $V_{bg} = -2$V (right).

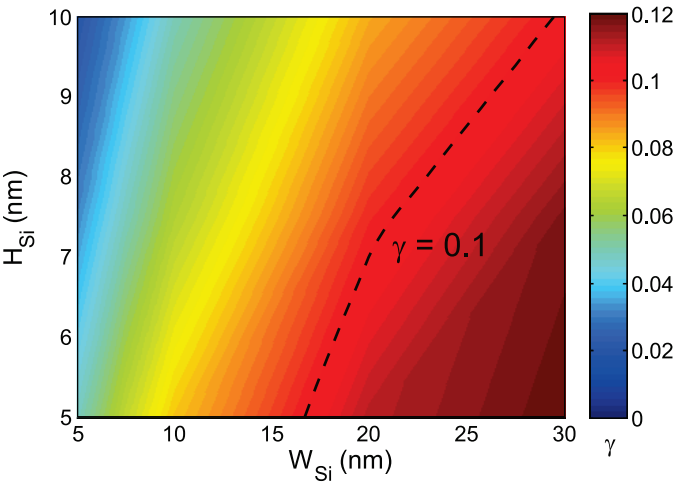

Fig. 4. Body factor (γ) as a function of W_{Si} and H_{Si}. The dashed line indicates the $\gamma = 0.1$ isoline.

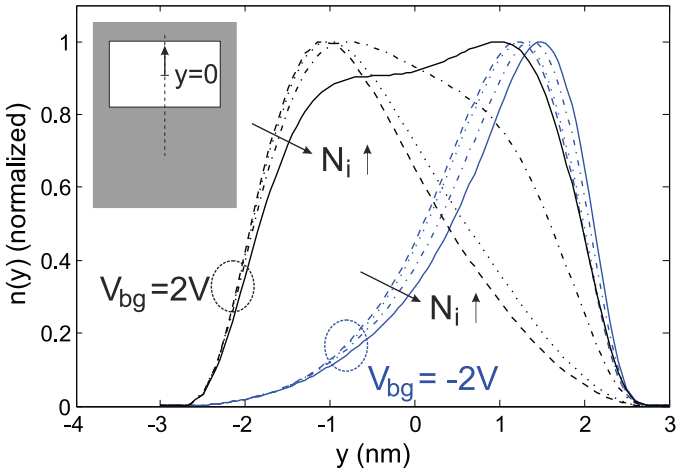

Fig. 5. Electron distribution at different inversion charges (N_i=10^5cm^{-1}, 10^6cm^{-1}, 5×10^6cm^{-1} and 10^7cm^{-1}) in a vertical slice (see inset) of a 10nm $\times$ 5nm trigate, with $V_{bg} = \pm 2$V.

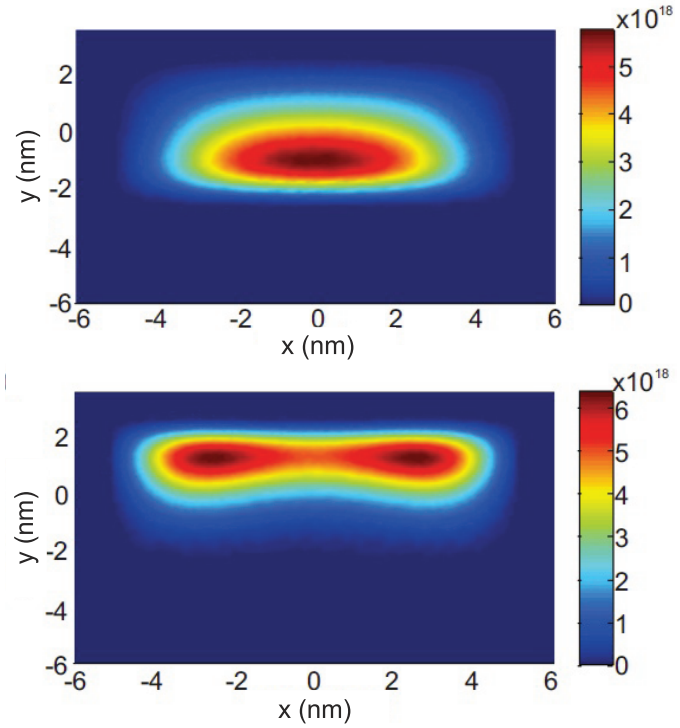

Fig. 6. Electron distribution at N_i=10^6cm^{-1} in a 10nm $\times$ 5nm trigate device, with $V_{bg} = 2$V (top) and $V_{bg} = -2$V (bottom).

Apart from the influence of the back-gate bias on the threshold voltage, the use of V_{bg} also modifies the electron distribution in the channel. Figure 5 represents the normalized charge distribution along a vertical slice of a $W_{Si} \times H_{Si} = 10$nm $\times$ 5nm trigate device for different inversion charges (N_i) at $V_{bg} = \pm 2$V. For positive V_{bg} values, the volume inversion effect is enhanced, being the charge more homogeneously distributed along the channel (even for large values of N_i, close to 10^7cm^{-1}). On the other hand, negative V_{bg} values shift the charge towards the top interface.

The 2D charge distribution is depicted in Fig. 6 at an inversion charge of $N_i = 10^6$cm^{-1}: not only the charge is closer to the top interface in the $V_{bg} = -2$V case, but it is also more confined and closer to the lateral regions of the device. As it will be demonstrated later, this redistribution of the charge has a very important influence on the carrier mobility.

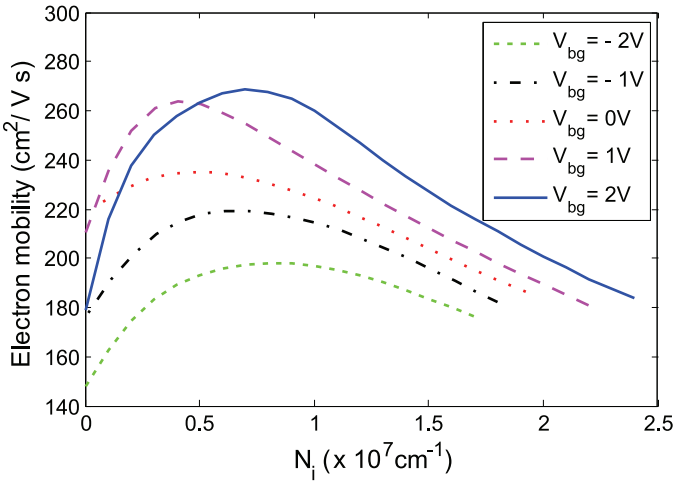

Fig. 7. Electron mobility *vs.* inversion charge as a function of the back-gate bias for a 10nm $\times$ 5nm trigate device.

B. Mobility results

The redistribution of the charge in the semiconductor fin as a function of V_{bg} affects the contribution of the different scattering mechanisms, and therefore it is expected to impact on the electron transport properties. To demonstrate it, we have calculated the electron mobility of a device with $W_{Si} = 10$nm and H_{Si}=5nm, depicted in Fig. 7 as a function of the inversion charge for V_{bg} values ranging from -2V to 2V. As shown, in general, higher V_{bg} values increase the electron mobility (although there is a non-monotonic behavior at low N_i). The resulting curves can be explained by studying, separately, the role of the different scattering mechanisms.

The influence of the CO scattering has been analyzed comparing the total mobility achieved in the absence of interfacial charges (only SR, AP and OP) and that achieved when the interface charge is placed only at the Si/BOX interface or at the Si/OX interfaces. The results, depicted in Fig. 8, prove that the Si/BOX charge has a negligible influence when $V_{bg} = -2$V, as the inversion charge is located close to the top interface (see Fig. 6). On the contrary, for $V_{bg} = 2$V, the charge is close to the bottom interface in the sub-threshold regime and thus, the CO-limited mobility due to $N_{it,bottom}$ is strongly degraded for $N_i < 5 \times 10^6$ cm^{-1}. It should be pointed out that, although the same value for N_{it} has been used for top, lateral and bottom Si/insulator interfaces, these values could be different in actual devices. For example, smaller values can be found in the literature for the Si/BOX interface, close to 10^{11}cm^{-1} [12].

Phonon (μ_{PH}) and surface roughness (μ_{SR}) limited mobilities are depicted in Fig. 9 for $V_{bg} = \pm 2$V. Both of them are higher when $V_{bg} = 2$V, explaining the results presented in Fig. 7. In the case of the phonon-limited mobility (dashed-lines in the figure), the lower mobility attained at $V_{bg} = -2$V is mainly due to the decrease of the contribution of Δ_4 valleys to the

total mobility, caused by their larger confinement close to the top interface and the corners (not shown). This effect increases the overlap integrals and therefore reduce their mobility.

The non-monotonic behavior of μ_{SR} for $V_{bg} = 2$V is related to the charge redistribution that occurs when N_i increases, as shown in Fig. 5. For small N_i, the charge is located close to the Si/BOX interface and the SR scattering due to this surface is not negligible. Thus, the SR mobility for $N_i \longrightarrow 0$ is very similar to that achieved for $V_{bg} = -2$V (which is caused mainly by the top interface). However, as V_{fg} is increased and N_i grows, the charge is shifted from the Si/BOX towards the center of the fin, as shown in Figs. 5 and 6, and therefore the influence of the SR scattering is reduced. As a consequence, the achieved mobility is larger than in the $V_{bg} = -2$V case (almost one order of magnitude for $N_i = 10^7$ cm^{-1}).

IV. Conclusions

We have analyzed the influence of the back-gate bias on the threshold voltage and the electron mobility of multigate silicon devices. It has been confirmed the possibility of achieving body factors higher than γ=0.1 as long as the channel width over height ratio is increased as much as possible. Moreover, a strong impact of the back-gate bias on the electron mobility has been shown. Positive back-gate bias pushes the charge further from the top and lateral Si/insulator interfaces, reducing the influence of SR and Coulomb scattering mechanisms and therefore increasing the carrier mobility. On the contrary, the carrier mobility is degraded for negative back-gate bias.

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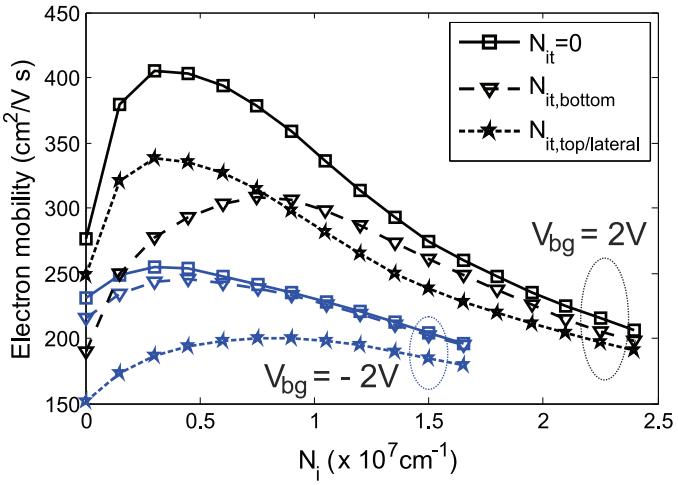

Fig. 8. Influence of the N_{it} on the total mobility ($V_{bg} = \pm 2$V) of a 10nm $\times$ 5nm trigate device: No N_{it} (squares), N_{it} only at the Si/BOX interface (triangles) and N_{it} only at the Si/OX regions (stars) are compared.

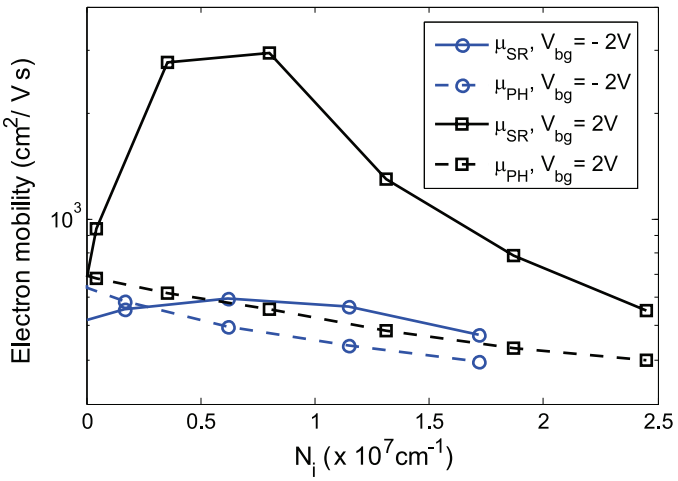

Fig. 9. SR-limited (solid lines) and phonon-limited (dashed-lines) mobility of a 10nm $\times$ 5nm trigate device with $V_{bg} = 2$V (squares) and $V_{bg} = -2$V (circles).

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