Simulation on Endurance Characteristic of Charge Trapping Memory

Zhiyuan Lun, Taihuan Wang, Lang Zeng, Kai Zhao, Xiaoyan Liu, Yi Wang, Jinfeng Kang, Gang Du*
Institute of Microelectronics, Peking University
Beijing 100871, China
* gangdu@pku.edu.cn

***Abstract*—A comprehensive simulation method for endurance reliability issues in charge trapping memory is developed. For this purpose, a practical algorithm is carefully designed to investigate the cycling performance of charge trapping memory. The models that account for the generation of substrate/tunneling oxide interface trapped charge and oxide trapped charge are incorporated into the simulation. The influence of these models on flat-band voltage evolution under programing/erasing cycling is investigated in detail, thus providing insight into the mechanism of the endurance issues in charge trapping memory.**

Keywords—endurance; charge trapping memory; cycling; interface trapped charge; oxide trapped charge

I. INTRODUCTION

Among many memory concepts proposed to replace the conventional floating gate devices, charge trapping based structure is considered to be the most promising candidate due to its immunity to stress-induced leakage current, reduced interference between adjacent cells and process compatibility with CMOS technology [1]. More recently, increasing attention has been paid to the reliability issues of charge trapping memory (CTM). A lot of effort is dedicated to investigate the retention reliability issues caused by formation of vertical charge dipole [2], charge trapping into defects in high-k blocking oxide [3-4] and trapped charge redistribution after erasing [5], whereas much less research is aiming at discovering the performance of charge trapping memory after programming/erasing (P/E) cycling. However, the modeling of trap generation at Si/SiO_2 interface and inside tunneling oxide and their effects is of great importance to understand cycling-related degradation phenomenon of CTM. In this paper, a comprehensive simulation method for endurance reliability issues is presented for CTM. In addition, a practical algorithm is designed to investigate the cycling performance of charge trapping memory. The influence of interface trapped charge and oxide trapped charge on P/E cycling evolution is distinguished by careful modeling.

II. PHYSICAL MODEL AND SIMULATION METHOD

A. Physical Models

Fig.1 illustrates the schematic of the fabricated CTM device studied here, with gate stack composed of SiO_2(5nm)/HfO_2(9nm)/Al_2O_3(17nm). The generation of interface traps at substrate/tunneling oxide interface, upon electrical stress, is considered to be one of the dominate effects on endurance characteristics of charge trapping devices [6], which is shown in Fig.2 (a). By incorporating the extensively-studied dispersive transport model proposed in [7] into our physical-based numerical simulator [8], the influence of interface trapped charge on endurance is effectively considered.

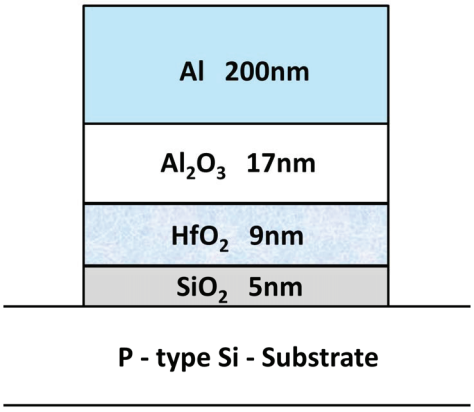

Fig.1. Schematic of the studied charge trapping device in this work.

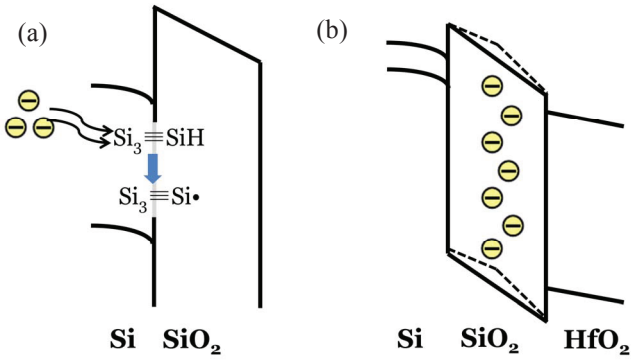

Fig.2. Mechanisms included to investigate (a) generation of Si/SiO_2 interface trapped charge and (b) oxide trapped charge.

The mechanism included in the simulation for the generation of Si/SiO_2 interface defects is modeled as

This work is supported by the National Basic Research Program of China (Grant No. 2010CB934203).

978-1-4673-5736-4/13/$31.00 ©2013 IEEE

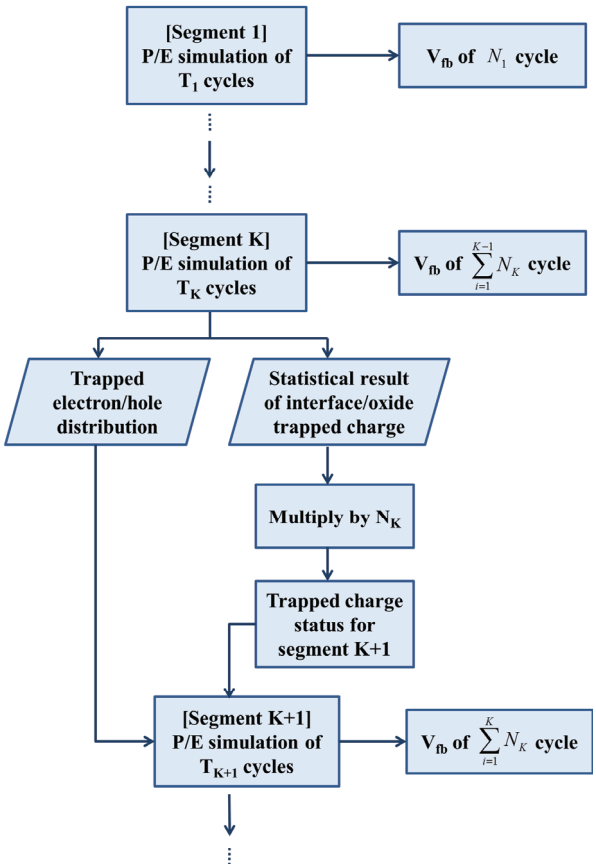

Fig.3. Cycle-weighted algorithm for P/E cycling simulation. N_K is the number of cycles in segment K(K=1…N).

$$[\mathrm{H_{int}}] = [\mathrm{Si_3} \equiv \mathrm{SiH}]\{1 - \exp(-\sigma_{\mathrm{H^+}} N_{\mathrm{inj}})\}, \quad (1)$$

where $[\mathrm{Si_3} \equiv \mathrm{SiH}]$ is the initial concentration of passivated SiH bonds with a typical value of $10^{13}\mathrm{cm}^{-2}$ [9], which yields interface states that can be charged in the following process with liberation cross section

$$\sigma_{H^+} = \sigma_0[(|qV_{ox}| - E_{th}) / E_{th}]^2, \quad (2)$$

and number of injected electrons per unit area

$$N_{\mathrm{inj}} = (1/q)\int J_{tun}(t)dt. \quad (3)$$

In (2), σ_0 is the hydrogen-release cross section and is estimated to be $10^{-19}\mathrm{cm}^{-2}$. E_{th} is the threshold electron energy for the release of hydrogen and equals to 1.4eV [9].

In the meanwhile, P/E cycling also increases the amount of tunneling oxide trapped fixed charge, resulting in shift of flat-band voltage and reshaping of the band diagram in both P/E process which finally affects P/E efficiency, as shown in Fig.2 (b). Tunneling oxide charge generation during cycling is modeled according to [10], which can be applied to a non-constant current stress over a large range of oxide thickness. This process is modeled by

$$N_{ox} = \alpha[\sigma_{ox}\int (J_{ox}/q)dt]^{\beta}, \quad (4)$$

where α is a fitting constant and β is a field-dependent factor and approximates to 1 in typical memory applications [10].

B. Simulation Approach

A cycle-weighted algorithm is introduced to reduce the computing time and memory effort when the endurance simulation is performed with approximately 100K cycles in this work. Fig.3 describes the basic simulation flow of the above algorithm. Firstly, total cycle number is divided into *N* segments. Then, *Ti* (i=1…*N*) cycles of the P/E simulation are performed at the start of each segment. The interface and oxide degradation in each cycle is calculated by the statistical results of the performed *Ti* P/E cycles. We assume that the change of tunneling current $J_{tun}(t)$ is negligible in each segment by choosing *N* and *Ti* appropriately. Thus, the total degradation accumulation of each segment is obtained. In the simulation, the input electrons and holes distribution as well as the potential diagram of next segment are taken from the results of previous segment.

III. Results and Discussion

The physical parameters used in the simulation are listed in Table I. Trap-assisted tunneling (TAT) is considered and modeled in the simulation due to that the generated defects can contribute to the change of TAT current.

By using the above set of physical parameters, the experimental data of P/E and incremental step pulse programing (ISPP) characteristics are well reproduced. The calibration results of these parameters and physical models are shown in Fig. 4.

TABLE I. Main Parameters Used in the Simulation.

Parameter	Value
SiO_2 electron effective mass	$0.30m_0$[11]
SiO_2 hole effective mass	$0.40m_0$[11]
Al_2O_3 electron effective mass	$0.20m_0$[3]
Al_2O_3 hole effective mass	$0.25m_0$[3]
SiO_2 electron trap depth for TAT	1.70eV[13]
SiO_2 hole trap depth for TAT	2.81eV[12]
SiO_2 electron cross section for TAT	$2\times10^{14}\mathrm{cm}^2$[13]
SiO_2 hole cross section for TAT	$2\times10^{14}\mathrm{cm}^2$[13]
SiO_2 trap density for TAT	$5\times10^{16}\mathrm{cm}^{-3}$[13]
HfO_2 electron trap depth	2.0eV[12]
HfO_2 hole trap depth	2.7eV[12]

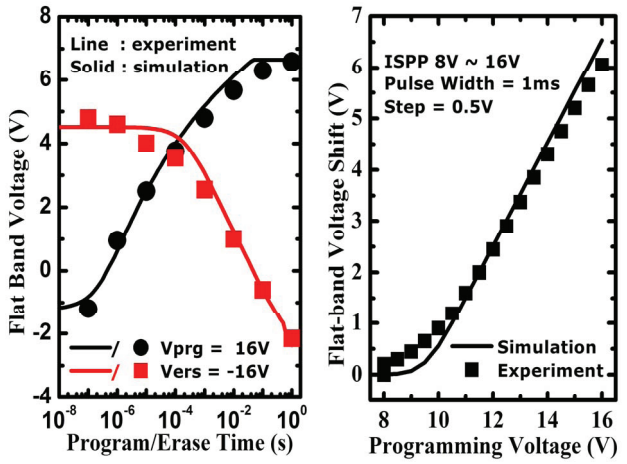

Fig.4. Calibration of the parameters and physical models in the simulation. The symbols are experimental data and the lines are simulation results. Vprg and Vers hereinafter indicate the programming voltage and erasing voltage respectively.

Fig. 5 illustrates the evolution of generated interface states with number of cycles, under different operation configurations. In terms of the device based on P-type substrate, these interface states are positively charged (donor-like) when the P/E cycling is monitored by flat-band voltage.

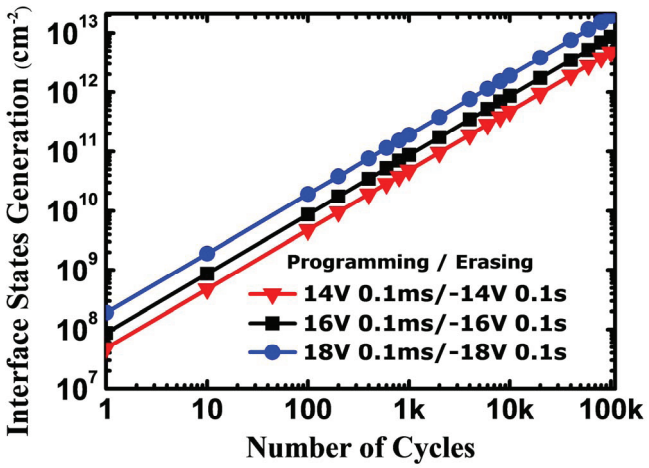

Fig.5. Interface states generation under different cycling operations.

Fig. 6 presents the asymmetric flat-band voltage evolution during P/E cycling due to interface trapped charge. The influence of negative oxide trapped charge on endurance characteristics is simulated by introducing cycle-dependent charge in tunneling oxide. Here we assume that the oxide trapped charge is located at the center of the oxide, which is feasible to cover the effect of distributed localized charge. It can be seen from Fig. 7 that the trapped electron density has a declining tendency with the P/E cycling.

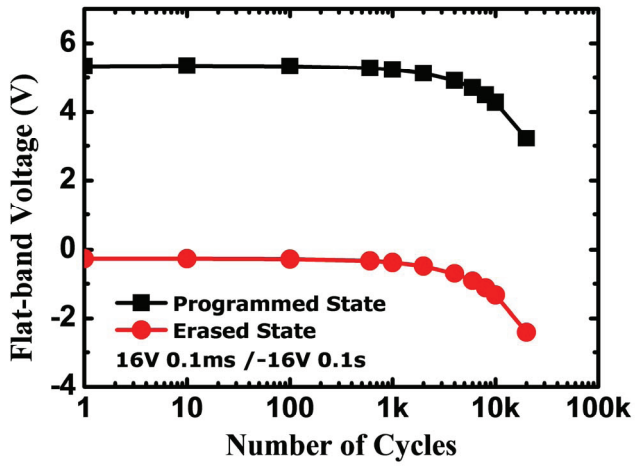

Fig.6. Flat-band voltage evolution due to interface trapped charge.

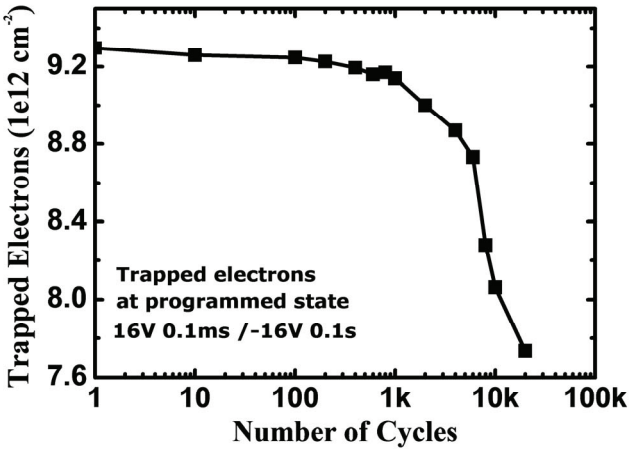

Fig.7. Trapped electrons in HfO_2 layer as a function of cycle number.

Fig. 8 demonstrates the evolution of P/E cycling affected by oxide trapped charge. The influence of flat-band voltage shift and effect of trapped charge on band diagram which leads to reduced programming efficiency are distinguished. It can also be concluded that reduced programming efficiency caused by negative oxide trapped charge is compensated by positive shift of flat-band voltage.

IV. Conclusion

The method to simulate endurance issues of CTM is developed. The generation of interface trapped charge and oxide trapped charge is incorporated into the simulator and a cycle-weighted algorithm for endurance simulation is introduced for endurance simulation. The simulator can be used to understand the detailed mechanisms of endurance issues in charge trapping memory.

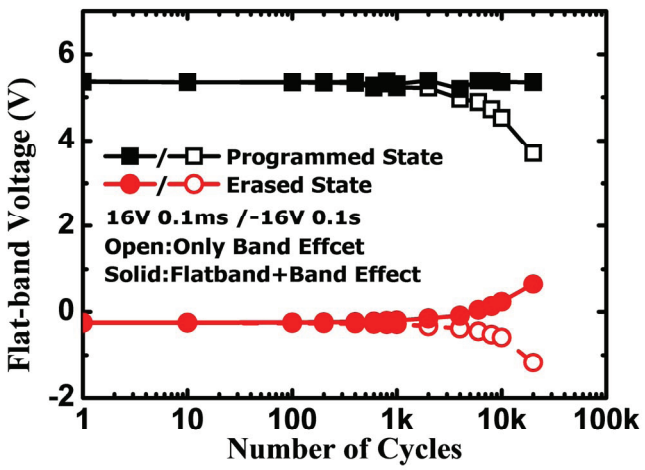

Fig.8. Evolution of P/E cycling affected by oxide trapped charge. Band Effect refers to effect of trapped charge on band diagram. Flatband refers to shift of flat-band voltage.

ACKNOWLEDGMENT

The authors would like to thank Guoxing Chen of Institute of Microelectronics, Chinese Academy of Science for sample testing and many helpful discussions.

REFERENCES

[1] G. Wang and M.H. White, "Characterization of scaled MANOS nonvolatile semiconductor memory (NVSM) devices", Solid-State Electronics, 2008(52), pp. 1491–1497.

[2] A. Padovani, A. Arreghini, L. Vandelli, L. Larcher, G.V. den bosch, J.V. Houdt, "Evidences for vertical charge dipole formation in charge-trapping memories and its impact on reliability", Applied Physics Letters, 2012(101), 053505–053505–4.

[3] A. Padovani, L. Larcher, V. Della Marca, P. Pavan, H. Park, G. Bersuker, "Charge trapping in alumina and its impact on the operation of metal-alumina-nitride-oxide-silicon memories: Experiments and simulations", Journal of Applied Physics, 2011(110), 014505–014505–9.

[4] S.M. Amoroso, A. Mauri, N. Galbiati, C. Scozzari, E. Mascellino, E. Camozzi, et al., "Reliability constraints for TANOS memories due to alumina trapping and leakage", IEEE International Reliability Physics Symposium (IRPS), , 2010, pp. 966–969.

[5] J.K. Park, D.-I. Moon, Y.-K. Choi, S.-H. Lee, K.-H. Lee, S.H. Pyi, et al., "Origin of transient Vth shift after erase and its impact on 2D/3D structure charge trap flash memory cell operations", IEEE International Electron Devices Meeting (IEDM), 2012, pp. 2.4.1–2.4.4.

[6] G. Van den bosch, L. Breuil, A. Cacciato, A. Rothschild, M. Jurczak, J. Van Houdt, "Investigation of Window Instability in Program/Erase Cycling of TANOS NAND Flash Memory", IEEE International Memory Workshop (IMW), 2009, pp. 1–2.

[7] P. Samanta, C.-L. Cheng, Y.-J. Lee, M. Chan, "Electrical stress-induced charge carrier generation/trapping related degradation of HfAlO/SiO2 and HfO2/SiO2 gate dielectric stacks", Journal of Applied Physics, 2009(105), 124507–124507–8.

[8] Y.C. Song, X.Y. Liu, Z.Y. Wang, K. Zhao, G. Du, J.F. Kang, et al., "Evaluating the effects of physical mechanisms on the program, erase and retention in the charge trapping memory", International Conference on Simulation of Semiconductor Processes and Devices, 2008, pp. 41–44.

[9] M. Houssa, V.V. Afanas'ev, A. Stesmans, M.M. Heyns, "Defect generation in Si/SiO2/ZrO2/TiN structures: the possible role of hydrogen", Semicond. Sci. Technol. (2001)16, L93.

[10] J. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, et al., "Flash EPROM endurance simulation using physics-based models", International Electron Devices Meeting Technical Digest, 1994, pp. 295–298.

[11] A. Gehring, S. Selberherr, "Modeling of tunneling current and gate dielectric reliability for nonvolatile memory devices", IEEE Transactions on Device and Materials Reliability. 2004(4), pp.306–319.

[12] L. Vandelli, A. Padovani, L. Larcher, R.G. Southwick, W.B. Knowlton, G. Bersuker, "A Physical Model of the Temperature Dependence of the Current Through SiO2-HfO2 Stacks", IEEE Transactions on Electron Devices, 2011(58), pp. 2878–2887.

[13] A. Padovani, L. Larcher, D. Heh, G. Bersuker, "Modeling TANOS Memory Program Transients to Investigate Charge-Trapping Dynamics", IEEE Electron Device Letters, 2009(30), pp. 882–884.