Impact of Back biasing in Ultra Short Channel UTBB SOI nMOSFETs

Kai Zhao[a], Tiao Lu[b,*], Gang Du[a], Xiao-yan Liu[a] and Xing Zhang[a]
a. Institute of Microelectronics, Peking University, 100871 Beijing, China
b. School of Mathematical Sciences, LMAM and CAPT, Peking University, Beijing 100871, China
*E-mail: tlu@math.pku.edu.cn

***Abstract*—The impact of back biasing on electron transport in extreme short channel Ultra-Thin Body and BOX (UTBB) SOI MOSFETs is investigated by a deterministic multi-subband Boltzmann solver. A 7.5nm channel length UTBB device is simulated, and its transport details are presented in this paper.**

***Index Terms*—UTBB, back biasing, Boltzmann transport equation (BTE), quasi-ballistic transport**

I. Introduction

UTBB SOI device is a promising solution for continued aggressive scaling beyond the 14nm node because of its better short channel effect control, threshold voltage modulation, reduced variability and compatibility with mainstream planar technology [1]. Many experimental works have be done [2], [3] to study nanoscale UTBB SOI devices characteristics recently. However, the carrier transport details inside the devices, which are critical for the compact models in sub 14nm scale, are not clearly known yet. A comprehensive study of electron transport details, with particular focus on the impact of back biasing, is presented in this paper.

II. Simulation method

A transient multi-subband deterministic Boltzmann transport equation (BTE) solver based on the Positive and Flux Conservative (PFC) method [4]–[6] is employed to explore the transport details in a end-of-roadmap UTBB SOI nMOSFET. The channel length is fixed to $7.5nm$ with $10^{14}cm^{-3}$ doping (Fig. 1). The effective oxide thickness (EOT) is $0.9nm$ and the source and drain length are both $7.5nm$ with a doping concentration of $10^{20}cm^{-3}$. The body thickness is $3nm$, and BOX thickness $6nm$. The BTE is 1D in real space (x-direction), and 2D in wavevector space $(\mathbf{k_x}, \mathbf{k_y})$ due to the quantization in z direction. The quantum confinement effect is taken into account by 1D Schrödinger equation (z-direction) and 2D Poisson iterations.

In real space, spacing of $0.3nm$ in x-direction and in z of $0.15nm$ are used (75×66 grid nodes). In the dimensional splitted $\mathbf{k}$ space, the adimensional kinetic energy has 150 grids with spacing of k_BT, and the angular dimension has 6 angles with spacing of $\pi/3$. Only 8 subbands are considered in the simulation due to the strong energy band splitting as a result of the ultra thin Silicon body. Phonon and surface roughness scattering are considered, and the Pauli exclusion principle is included in the BTE solver.

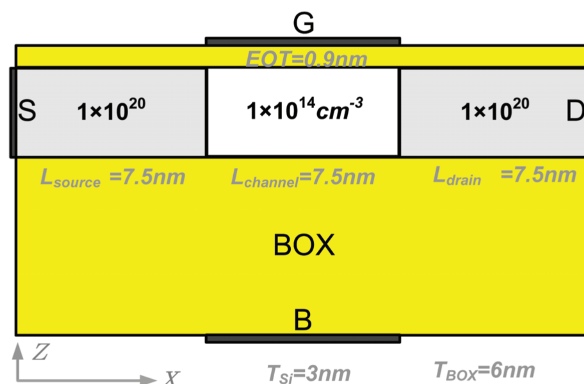

Fig. 1. The device structure of the simulated UTBB SOI nMOSFET and the doping profile. The channel length is $7.5nm$, source and drain length $7.5nm$, EOT $0.9nm$, $T\ _i$ $3nm$ and T_{BOX} $6nm$ respectively.

III. Results and discussion

The ballistic and diffusive output characteristics of the simulated UTBB SOI device at zero back biasing (ZBB) are shown in Fig. 2. Although the channel length is extremely short, scattering still plays an important role, especially for the strong inversion and large drain bias cases. Therefore, all the results below are simulated at diffusive conditions. The output characteristics at different back biases with V_g=0.4V and 0V are shown in Fig. 3. The effect of back-biasing modulation is obvious seen at both $0.4V$ and zero gate voltages. Forward back biasing (FBB) boosts the drain current significantly, and makes the device acting as a double gate MOSFET. The output curves at V_g=0.4V with -1V reverse back biasing (RBB) and V_g=0V with 1V FBB coincide very well, which means that 2V back bias may achieve the similar control ability with 0.4V gate voltage for such a device structure.

Fig. 4 demonstrates the 3D potential profile at V_g=0.4V, V_d=0.4V and V_b=-1.0V. In contrary to typical double gate MOSFETs, the potential distribution in the channel along the quantum confinement direction is asymmetric. The 3D potential profile shows that RBB can reinforce the gate control ability and hence reduce the DIBL effect. Fig. 5 illustrates the cross-section potential profile and electron density distribution along quantum confinement direction at the virtual source (VS) [7] for different back biasing at V_g=0.4V, V_d=0.4V. The back biasing modulation on the electrostatic potential manly

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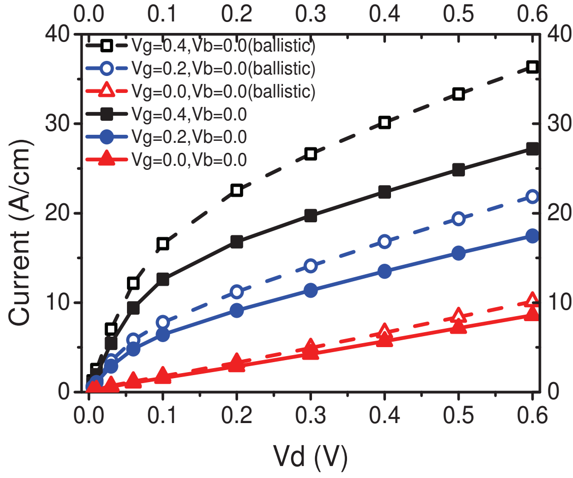

Fig. 2. Comparison of ballistic and diffusive output characteristic at zero back bias and different gate voltages. All the results below are simulated with the presence of phonon and surface roughness scattering.

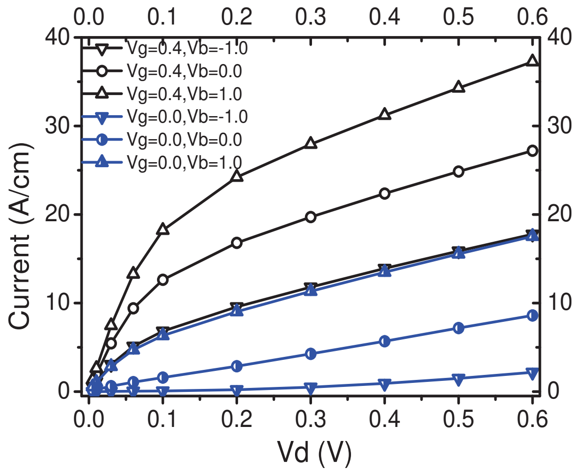

Fig. 3. Output characteristic at different back biases with V_g=0.4V and 0V.

appears in the bottom half of the silicon layer. The ultra thin silicon layer results in strong quantum confinement in the channel, and drives electrons away from the surfaces. Therefore, the range of the density peak shift in thin silicon layers is not as obvious as that in larger devices.

The back biasing tuning effect on the lowest subband is shown in Fig. 6. FBB lowers the barrier height significantly, especially for the small gate bias cases. Therefore, in order to turn off ultra short channel devices and minimize the off-state current, RBB is necessary. It is worth noticing that there are subband energy drops at the channel-end of the source when imposing FBB at V_g=0.4V and V_d=0.4V. The contribution to the sheet density of the two-folded lowest subbands at the VS is shown in Fig. 7. The two-folded lowest subbands contribute up to 97.5% of the total electrons at V_b=-1.5V and V_g=0V, and down to 71.4% at V_b=1.5V and V_g=0.4V. The reason is that back biasing induced barrier lowering (BBIBL) and gate

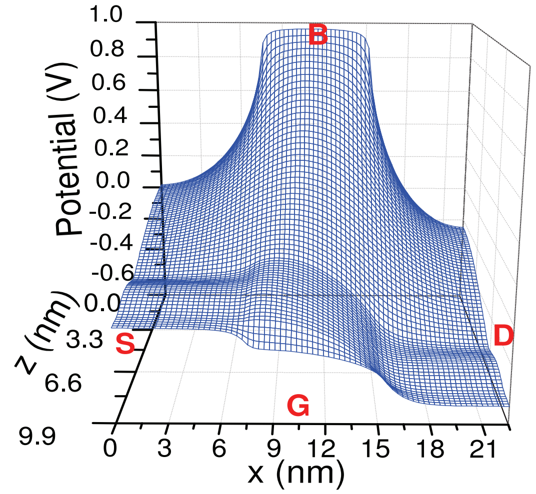

Fig. 4. The three dimensional potential profile of the simulated device with V_g=0.4V, V_d=0.4V and V_b=-1.0V.

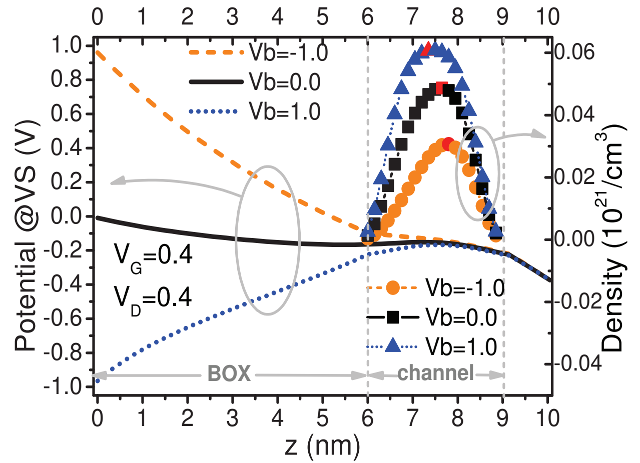

Fig. 5. The cross-section potential profile and electron density distribution along the quantum confinement direction on the VS. The back bias varies from -1V to 1V. V_g and V_d are set to 0.4V.

induced barrier lowering (GIBL) (Fig. 6) insure higher energy injections at the VS.

Fig. 8 shows the barrier height with respect to the source contact as a function of back biases at different gate and drain voltages. According to the virtual source model [7], electron density and group velocity at the VS are merely determined by the barrier height. Fig. 8 clearly shows that the barrier height has strong dependency on back biasing, especially in the RBB region. This is the main mechanism of the back biasing tuning effect. Fig. 9 shows the electron group velocity at the VS as a function of back biases. The group velocity increases more rapidly in the RBB region when increasing V_b, which is self-consistent with Fig. 8. Usually for deca-nanometer channel length devices, the injection group velocity at the VS is smaller

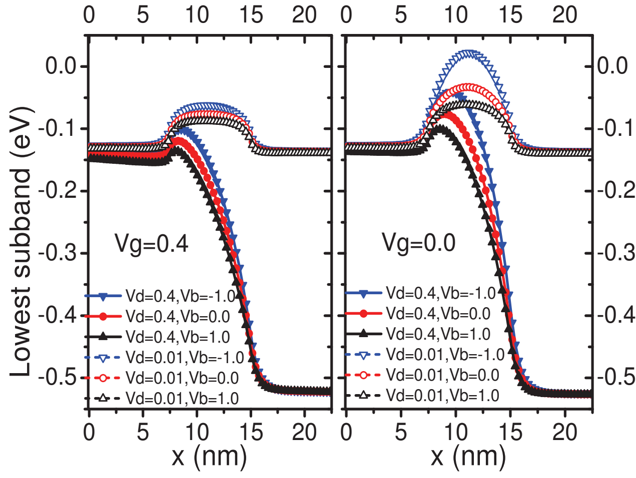

Fig. 6. The lowest subband profile along the transport direction for different back and drain biases with V_g=0.4V (left) and 0V (right), respectively.

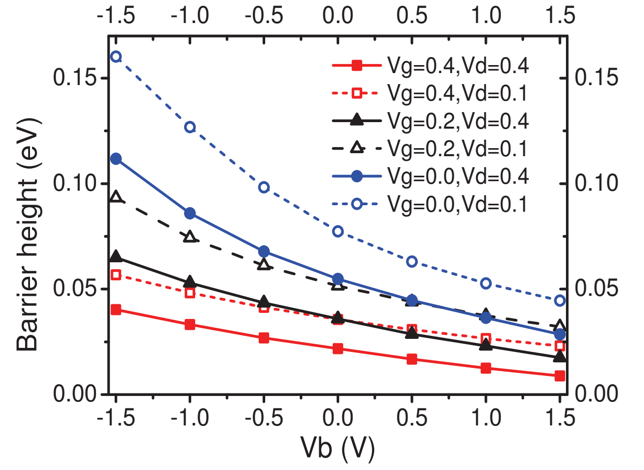

Fig. 8. The barrier height w.r.t. the source contact as a function of back bias at different gate and drain voltages.

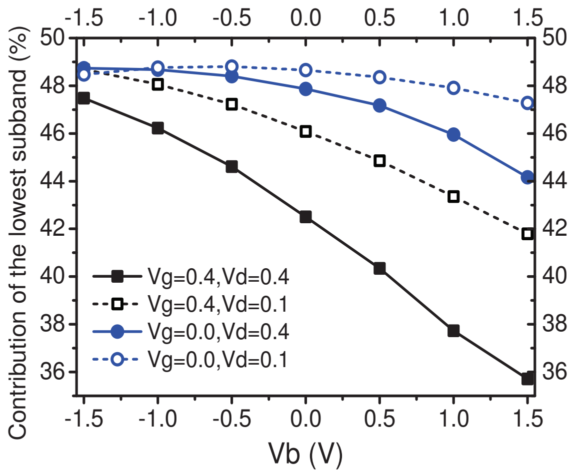

Fig. 7. The contribution to sheet density of the 2-folded lowest subband on the VS at different back biases.

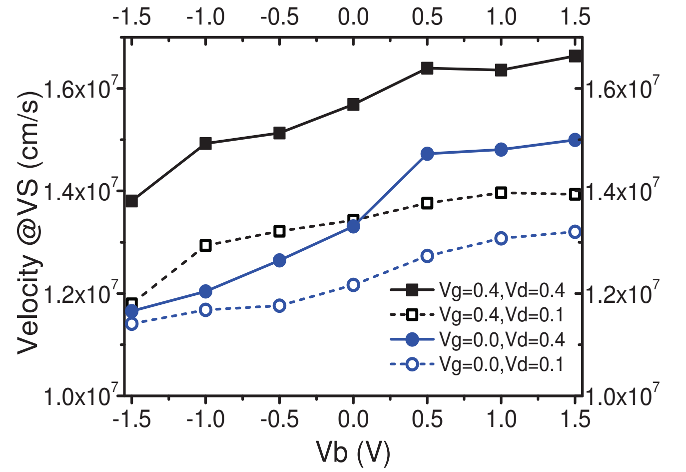

Fig. 9. The group velocity on the VS as a function of back bias at different gate and drain voltages.

than the thermal velocity v_{th} ($10^7 cm/s$) [8], [9]. However, in such a short channel and thin body device, the group velocity at the VS may higher than v_{th}. In the FBB region of the on-state case(e.g. the solid black line), the electron distribution is already far from equilibrium because of the potential drop in the source region(Fig. 3 left). Electrons have already been accelerated before reaching the VS when applying large gate and drain biases. Fig. 10 shows the electron sheet density at the VS as a function of back biases. The sheet density increases almost linearly with the increase of back voltage at on-states. Fig. 11 shows the ratio of backward moving and the forward moving electron density on the VS with $0.4V$ gate voltage at different back and drain biases. The backward moving electrons increase exponentially in the FBB region attributing to the barrier lowering w.r.t. the drain contact.

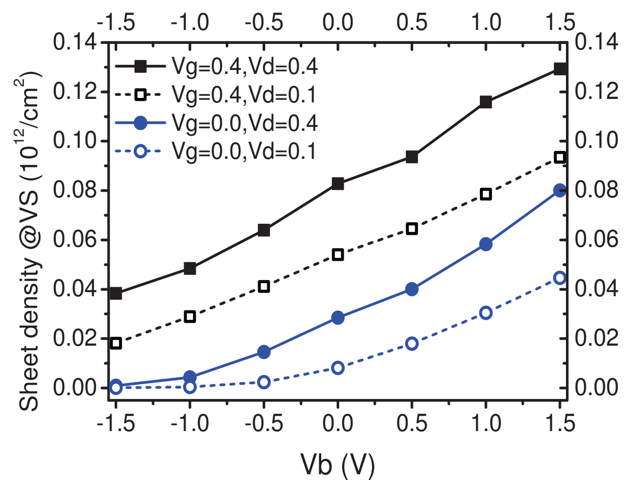

Fig. 10. The electron sheet density on the VS at different back biases with V_g=0.4V and 0.0V.

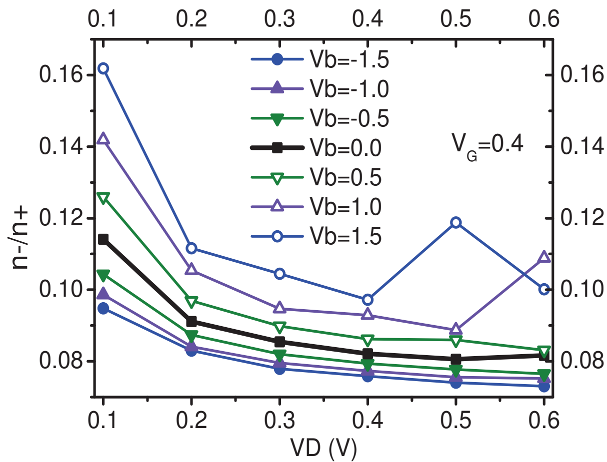

Fig. 11. The ratio of n- and n+ on the VS at different back and drain biases with V_g=0.4V.

IV. Conclusion

In this paper, we explored detailed electron transport characteristics in a $7.5nm$ channel length UTBB SOI nMOSFET. The back biasing dependence of electrostatic potential, barrier height, electron velocity and density on the VS, which are critical to end-of-roadmap device modeling, were calculated by a physically based multi-subbband BTE solver. The barrier height modulation induced by back biasing plays a very important role in nano-scale UTBB SOI devices.

Acknowledgment

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References

[1] F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J.-P. Noel, C. Fenouillet-Beranger, J.-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand *et al.*, "Low leakage and low variability ultra-thin body and buried oxide (ut2b) soi technology for 20nm low power cmos and beyond," in *VLSI Tech. Dig*, 2010, pp. 57–58.

[2] Q. Liu, F. Monsieur, A. Kumar, T. Yamamoto, A. Yagishita, P. Kulkarni, S. Ponoth, N. Loubet, K. Cheng, A. Khakifirooz *et al.*, "Impact of back bias on ultra-thin body and box (utbb) devices," in *VLSI Tech. Dig*, 2011, pp. 160–161.

[3] N. Xu, F. Andrieu, B. Ho, B.-Y. Nguyen, O. Weber, C. Mazuré, O. Faynot, T. Poiroux, and T.-J. K. Liu, "Impact of back biasing on carrier transport in ultra-thin-body and box (utbb) fully depleted soi mosfets," in *VLSI Tech. Dig*, 2012, pp. 113–114.

[4] F. Filbet and G. Russo, "High order numerical methods for the space non-homogeneous boltzmann equation," *J. Compu. Phys.*, vol. 186, no. 2, pp. 457–480, 2003.

[5] T. Lu, G. Du, X. Liu, and P. Zhang, "A finite volume method for the multi subband boltzmann equation with realistic 2d scattering in double gate mosfets," *Commun. Comput. Phys.*, vol. 10, no. 2, p. 305, 2011.

[6] G. Liu, G. Du, T. Lu, X. Liu, P. Zhang, and X. Zhang, "Simulation study of quasi-ballistic transport in asymmetric dg-mosfet by directly solving boltzmann transport equation," *IEEE Trans. on Nanotechnology*, vol. 12, no. 2, pp. 168–173, 2013.

[7] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Trans. Electr. Dev.*, vol. 49, no. 1, pp. 133–141, 2002.

[8] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.*, vol. 76, no. 8, pp. 4879–4890, 1994.

[9] P. Palestri, D. Esseni, S. Eminente, C. Fiegna, E. Sangiorgi, and L. Selmi, "Understanding quasi-ballistic transport in nano-MOSFETs: Part I-scattering in the channel and in the drain," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2727–2735, 2005.