Compact Modeling of SOI MOSFETs with Ultra Thin Silicon and BOX Layers for Ultra Low Power Applications

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Abstract— A compact model for SOI-MOSFET with ultra-thin both SOI and BOX layers has been developed based on the potential distribution within the device. The potential distribution is calculated by solving the Poisson equation together with additional analytical equations derived under approximations. All equations are solved simultaneously by the Newton iteration method. It is demonstrated that the model can not only reproduce measured specific device characteristics but can even predict change of device characteristics caused by device parameter change.

Keywords—thin-film transistor, SOI-MOSFET, compact model, potential-based model, Poisson equation

I. INTRODUCTION

Ultra thin-film transistors are getting more attention due to superior short-channel control as well as reduced variability of device performances [1,2]. The SOI-MOSFET with ultra-thin SOI and BOX layers (SOTB-MOSFET) is one of such transistor structures developed for ultra-low power applications, which controls threshold voltage through an ultra thin BOX by adjusting the back-gate voltage [3]. To exploit such new device functions in circuit design an accurate compact model is inevitable. However, compact model development of such ultra-thin film devices is very tough, because the potential distribution must be considered from the surface to the bottom of the substrate explicitly to describe all induced charged accurately.

Conventional compact models for SOI-MOSFETs are developed based on the threshold voltage description, and the floating potential value at back-surface potential is often analytically described [4]. We have developed the SOI-MOSFET model HiSIM-SOI for devices with any SOI-layer thickness, dynamically varying channel condition between fully and partially depletion, by solving the Poisson equation explicitly [5, 6]. Here we extend the model for SOTB-MOSFET, where inversion as well as accumulation charges at the both side of BOX are explicitly considered. Different from the double-gate MOSFET, the influence of the impurity concentration of the substrate must be explicitly considered.

Thus the main tasks for the development of the SOTB generation are:

1. Device performances must be formulated with physical device parameters such as the impurity concentration, and thus the model can be applicable even for device optimization.

2. The model is applicable for wide variety of applied bias variations from positive to negative values with correct description of the strong coupling effect between the front- and the back-gate control.

II. FEATURE OF SOTB-MOSFET

Fig. 1a shows the schematic of the SOTB-MOSFET structure. The studied device parameters are depicted together. Three surface potentials (\(\phi_s\), \(\phi_b\), \(\phi_{bulk}\)) plus that within the SOI-layer (\(\phi_b'\)) describe the potential distribution along the vertical direction of the device as can be seen in Fig. 1b. The back-gate bias \(V_{bg}\) is utilized to control the threshold voltage \(V_{th}\), which is varied largely from positive to negative. As can be seen in Fig. 1a, many varieties of structural variations are possible for SOTB-MOSFET. The impurity concentration in the SOI layer \(N_{SOI}\) is optimized to meet the requested \(V_{th}\). Usually the impurity concentration in the substrate \(N_{SUBB}\) is adjusted to optimize the \(V_{bg}\) dependence of \(V_{th}\). The lower value of \(N_{SUBB}\) results in reduced \(V_{bg}\) dependence (see Fig. 2b). This is due to the depletion width extension within the substrate and the voltage \(V_{bg}\) applied is largely absorbed within the substrate. In Fig. 2, not only the \(V_{bg}\) dependence change but also the change in \(V_{th}\) shift is also observed by the \(N_{SUBB}\) variation. To optimize the device parameters to meet device requirements, thus, all device parameters must be explicitly considered in modeling without treating them as fitting parameters. Though the studied device has the same impurity-concentration type in \(N_{SUBB}\) as that in the SOI layer, it is also possible to have the different type. This changes not only the built-in potential between \(N_{SOI}\) and \(N_{SUBB}\), but also sign of charges induced at BOX.
III. BASIC EQUATIONS

Since $V_{gs}$ as well as $V_{bg}$ varied are widely from negative to positive, charges induced within the device are varied after the bias conditions. Typical charge distributions are summarized in Fig. 3. These charges are a function of potential values depicted together in Fig. 3. Fig. 4a shows 2D-device simulation results of the inversion charge within the SOI layer for the case (b) with $V_{bg}=1$V and the case (c) with $V_{bg}=-1$V in Fig. 3. Circles and triangles are 2D-device simulation results, and lines are calculated charges with simulated solutions of potential values at surfaces $\phi_s$ and $\phi_b$. Dashed lines are calculated charges induced only at the front surface $Q_i$ and solid lines are sum of two charges $Q_i$ and $Q_b$. It is seen that the total inversion charge consists of two parts for the case (b). For the charge calculation the charge sheet approximation is assumed. Deviations between circle and lines becomes more obvious with positively increased $V_{bg}$. However, it can be concluded that the charge-sheet approximation is still valid for the studied device even for very thin SOI layer thickness of 10nm (see Fig. 1a). The main cause of the subthreshold slope degradation for $V_{bg}$>0 is thus the additional carrier contribution induced in the SOI layer at BOX. This phenomenon is quite similar to the double-gate MOSFET but a big difference is that the amount of the charge induced at the BOX is influenced not only by $V_{bg}$ but also strongly by $N_{subb}$.
The Poisson equation for SOTB-MOSFET together with the Gauss law is written as

\[ V_{gs} - V_{th} - f_c = (Q_i + Q_{sdep} + Q_b + Q_{bulk}) V_{C_{FOX}} \]  

(1)

where \( Q_i, Q_{sdep}, Q_b \) and \( Q_{bulk} \) are the inversion and depletion charges at the front surface and back-gate surface, respectively. The bulk charge induced at the BOX surface of the back-gate side is denoted by \( Q_{bulk} \) (see Fig. 3). All these charges are function of potential values. Thus to describe the device feature for various different bias conditions accurately the main task for model development is to calculated accurate potential values along the depth direction. To solve four potential values, three additional equations are required. These equations are derived differently for different bias conditions.

1. Case (c): Front-surface potential control \( (V_{bg} \leq 0) \)

Smooth potential change along the device depth direction without potential peak \( \phi_i = \phi_b \)

\[ \phi_i - \phi_b = (Q_{FD} + 2Q_{bulk}) / 2C_{SOI} \]  

(2)

derived by solving the Poisson equation analytically under the approximation that the inversion charge, assuming the charge-sheet approximation, can be ignored for calculating the potential distribution within the SOI layer. The charge \( Q_{FD} \) is the depletion charge and \( C_{SOI} \) is the capacitance in the SOI layer.

2. Case (b): Both surface and back-surface potential controls

Peak in the SOI layer occurs and thus both equations from Case (a) and Case (b) must be solved together.

3. Case (a): Back-surface potential control \( (V_{bg} > 0) \)

Smooth potential change along the device depth direction without potential peak \( \phi_b = \phi_b \)

\[ \phi_b - \phi_i = (Q_{FD} + 2Q_{bulk}) / 2C_{SOI} \]  

(3)

derived in the same way as the case (c) but from the back-gate side.

All cases required one more equation

\[ \phi_{bulk} = \phi_b + V_{bi} + Q_{bulk} / C_{BOX} \]  

(4)

derived by the Gauss law at BOX.

It is seen that the above additional analytical equations are mostly derived under the charge-sheet approximation. However, the major difficulty preventing from deriving precise analytical equations is the thin body thickness. The layer is so thin that no charge neutrality is preserved either at the front-gate insulator or at BOX independently. The neutrality is preserved only totally within the whole device. Thus the most important equation preserving the correct physics of such ultra thin devices is the Poisson equation.

The Poisson equation can be solved only iteratively together with additional equations. Thus all equations are solved simultaneously with the Newton method. Though it is believed that the iterative solution requires more simulation time, the CPU increase due to the iteration is not serious in circuit simulation. The reason is that the time step for the circuit simulation is well controlled by simulator so that no drastic potential change does not occur and thus the previous solution of the potential values can be used as initial values. In compact modeling, charges on nodes must be calculated by integrating the charge distribution along the channel. Once the potential values at the source side and the drain side are calculated, charges at the both sides are calculated, which are integrated along the channel. Derivatives of the charges determine capacitances, and integration of the inversion charge with the carrier mobility gives the current as schematically shown in Fig. 5.

![Fig. 5. Surface-potential-based modeling approach for consistancy of different device characteristics like currents and capacitances.](image)

IV. MODEL VERIFICATIONS

The developed model is verified with measured I-V characteristics as demonstrated in Fig. 6. For reproducing all device characteristics the device parameters extracted with extra measurements are adopted without any modifications. Reliability of the extracted model parameter values is confirmed by verifying that one set of model parameter values is valid for any device sizes. As can be seen the important device characteristics for the \( V_{bg} \) variation is well reproduced without any fitting parameters (see Fig. 6a). The transconductance characteristics are depicted in Fig. 6b, and \( I_{ds}-V_{bg} \) characteristics are shown in Fig. 6c. The channel conductance is compared in Fig. 6d. In Fig. 6 simulation results only for a long-channel case is depicted, but the same accuracy is achieved for any device sizes.

Calculated charges are compared among three different \( V_{bg} \) values as a function of \( V_{gs} \) in Fig. 7. For \( V_{bg} \leq 0 \), the bulk charge \( Q_{bulk} \) is always negative, and it becomes positive for \( V_{bg} > 0 \) as schematically depicted in Fig. 3. However, it becomes even negative because of the strong front-gate control by increasing \( V_{gs} \). The front-surface inversion charge \( Q_i \) increases drastically by increasing \( V_{gs} \). The back-surface inversion becomes obvious only for \( V_{bg} > 0 \). In the HiSIM-SOTB calculation, the back-surface inversion charge is reduced to zero with increased \( V_{gs} \) values, which is different from the 2D-device simulation results shown in Fig. 4b. The reason is that HiSIM-SOTB attributes all inversion charge to \( Q_i \) after the front-gate control dominates.

V. DISCUSSIONS

Fig. 2 compares 2D-device simulation results with different \( N_{SUBB} \) values. Calculation results with HiSIM-SOTB are depicted together by solid lines. For the simulation the model parameter values are extracted with the I-V characteristics shown in Fig. 2a, and the \( N_{SUBB} \) value is changed to the used value for the I-V simulation shown in Fig. 2b. Additionally the Coulomb scattering parameter was slightly adjusted. Fig. 8 shows another measured I-V characteristics with 10 times lower impurity concentration of the substrate \( N_{SUB} \). Fig. 8a shows calculated results with the extracted model parameter values shown in Fig. 6. Clear
deviation is observed. Fig. 8b shows calculated results obtained only by reducing the $N_{SUBB}$ value by a factor of 10. Agreement to the measurements is quite good. This confirms the accuracy of the extracted model parameter set.

VI. CONCLUSION

An advanced SOI technology aims at ultra low-power applications realized by controlling $V_{th}$ with the back-gate bias $V_{bg}$. The compact model HiSIM-SOTB has been developed for the device valid even for the device optimization. The model is based on the complete potential-based description solving the Poisson equation iteratively together with additional equations derived. It is demonstrated that the model can reproduce not only measured $I-V$ characteristics but also the device parameter dependence accurately.

REFERENCES


