Bridging Design to Manufacturability by Layout Enhanced Analyses Process Simulations (LEAPS)

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***Abstract*— This work describes a novel approach (LEAPS) that combines process simulations with layout analyses for identifying manufacturing hotspots. The LEAPS workflow for integration within the foundry's manufacturing environment is also presented. One advantage of the LEAP methodology is the multi-dimensional consideration of simulation and process sensitivity to narrow down to actual manufacturing hotspots.**

Keywords*— *Design, Manufacturability, Process Simulations, Layout Analysis, LEAPS, Workflow.

I. Introduction

Design for manufacturing (DFM) methodologies can help to address the challenges in the deep-submicron regime of integrated circuits manufacturing today [1]. Despite fulfilling standard design rules, layout weakpoints with process marginalities continue to exist that can severely impact yield. As the foundry moves towards streamlining process offerings to cater for different customers, there is an increasing need to understand the relationship between design layout and process variations, and how this impacts yield.

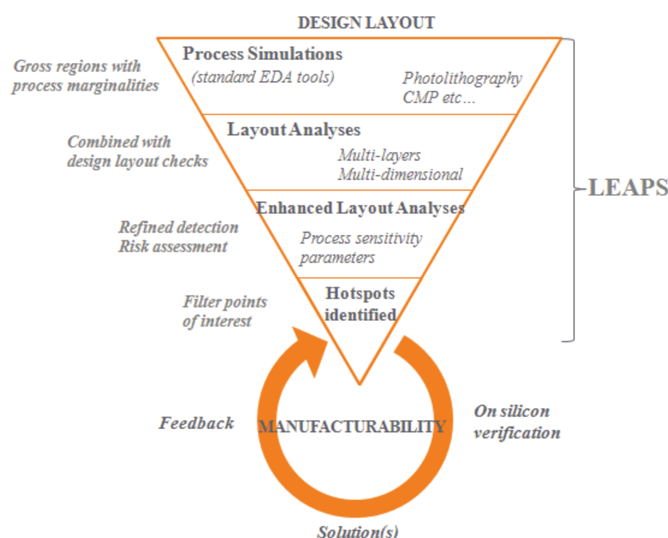

Fig. 1. Schematic illustrating the implementation of LEAPS in the foundry. The manufacturing hotspots are verified on silicon and then feedback into the LEAPS model.

II. LEAPS Workflow And Implementation

In this work, we describe a novel approach (LEAPS) that combines process simulations with layout analyses for identifying process hotspots during manufacturing. The advantage of LEAPS is that the results from our multi-dimensional analyses can help to further filter and refine real process hotspots from noise. Fig. 1 illustrates the workflow for implementing LEAPS in the foundry and dovetailing this with on-silicon verification and feedback in manufacturing.

Both simulation and layout-based process sensitive structures are considered in LEAPS. The manufacturing hotspots density is broadly governed by (1):

$$\text{Hotspot Density} = \sum_{i=1}^{M} k_i \text{ Density}_{\text{simulation parameter }(i)} + \sum_{j=1}^{N} k_j \text{ Density}_{\text{process sensitive structure }(j)} \quad (1)$$

Multiple process simulations (M), and multiple layers (N) such as the interaction of multiple metal layers during BEOL integration, are also considered in the LEAPS model. Furthermore, we observed from our experience that some process marginalities are layout pattern specific. Silicon-verified hotspots can be incorporated into our LEAPS model with a higher weighting factor ($k_i > 1$, $k_j > 1$).

Standard process simulations in the foundry include optical/photolithography, etch, chemical mechanical polishing (CMP) [2]. Optical simulation parameters include mask error enhancement factor, normalized intensity log slope and intensity-based thresholding [3] *etc*. Fig. 2 shows an example of simulated optical curves ($I_{maximum}$ and $I_{minimum}$ values) generated by standard photolithography simulator.

Suppose the exposure dose (intensity threshold) is varied, in Fig. 2A and 2B, the minimum $I_{maximum}$ corresponds to the via that is most likely to be underexposed. Conversely, in Fig. 2C and 2D, the maximum $I_{minimum}$ points correspond to the spaces between the vias most likely to be bridged due to overexposure. While simulations can identify many potential hotspots initially, filtering down to specific process-sensitive structures may be achieved by factoring in layout analyses and actual feedback from the manufacturing line [4].

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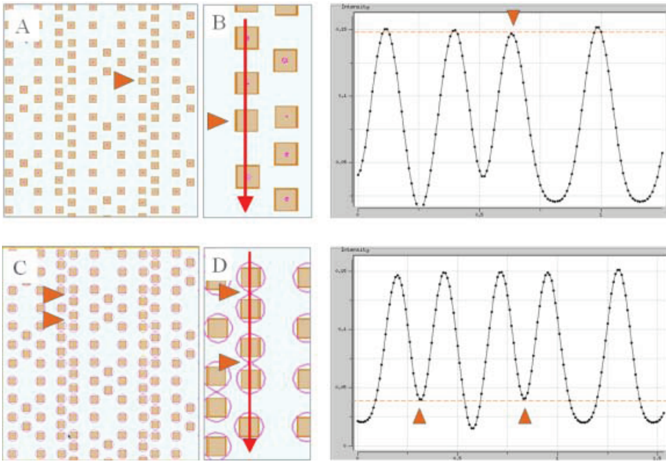

Fig. 2. Example of an optical simulation parameter utilizing intensity-based thresholding. Although the vias are designed with the same dimensions, their actual printed dimensions on silicon are affected by their local environment. The arrows indicate the via process hotspots. A) Via most likely to be underexposed; B) Cross-section intensity vs. distance across 4 via locations: the curve shows that the third via is falling below intensity threshold (dotted line); C) Spaces between vias that are most likely to bridge due to overexposure; D) Cross-section intensity vs. distance across 5 via locations: the curve shows that the space between first and second vias, and between the third and fourth vias, are above intensity threshold (dotted line).

III. Application Of LEAPS To Identify Manufacturing Hotspots

A. *Multi-Dimensional Layout Analyses Identify Via-Related Manufacturing Hotspots*

Picture this scenario: given thousands of vias in a typical design layout, how does one go about identifying the "weakest" via? As discussed earlier, process simulation is on e of the approaches to identify such problematic vias. Multi-dimensional layout analyses can also be a useful tool to determine the process sensitive structures.

Fig. 3 is an example of a typical process-sensitive via-related hotspot (so called "isolated gradient via") that is prone to failure during manufacturing. The multiple criteria for our layout analyses search include: i) isolated via without any neighbor vias within the distance >3x via width; ii) isolated via that is in the net connection path with no redundancy, *i.e.* if this sole via fails, then the net connection will be broken; and iii) via ("gradient via") in an area A that is adjacent to an area B with high via density.

The rationale for these selection criteria stem from a combination of yield considerations and manufacturing process feedback. As illustrated in Fig. 2, the ability to expose and print a feature by photolithography on silicon depends on the local environment of the feature. An isolated via without any neighbors behaves very differently from an optical point of view from a via inside an environment of dense vias.

Furthermore, from a yield point of view, singly-connected isolated vias are more critical compared to isolated vias with redundancy. Therefore, isolated non-redundant vias are assigned a higher weighting k_j, and the density distribution of such vias (red) are shown in Fig 3A.

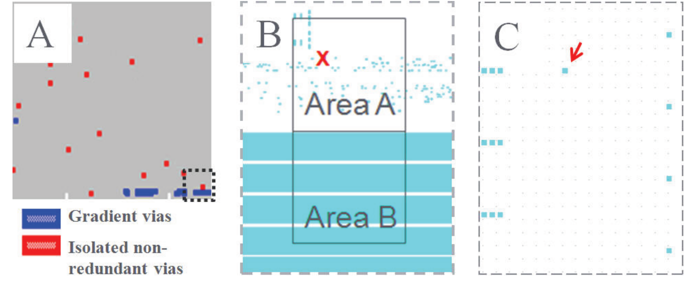

Fig. 3. Multi-dimensional layout analyses of vias filter out the most process sensitive via features on silicon. A) Map showing the distributions of isolated vias with no net connection redundancy and no neighboring vias in close proximity (red) and regions with a high gradient of via densities (blue); B) Area A shows isolated vias, Area B shows highly dense vias, forming a high gradient region; C) The critical via hotspot is the isolated via (red arrow) that lies in this high gradient region.

Applying process etch considerations, isolated vias with a high density gradient, *i.e.* isolated vias (low vias density, Fig. 3B Area A) adjacent to regions with high via density (Fig. 3B, Area B), are more prone to punchthrough during etch. This is has been commonly observed due to the difference in etch rates between the iso- and dense-regions [5-6].

Combining these layout analyses, the process sensitive critical via could be narrowed down to the isolated non-redundant via with a high gradient as shown in Figs. 3B and 3C. On-silicon data feedback that such vias identified by our multi-dimensional layout analyses can punchthrough to metal lines two or more levels downwards. Suppose that a via punchthrough causes bridging of two independent net connections, a catastrophic failure may occur. Therefore, including even more criteria for layout analyses, such as the overlap of isolated gradient vias with underlying metal levels, may be a powerful approach to further refine the detected hotspots.

B. *Multi-Dimensional Critical Area Simulations With Layout Analyses Identify Manufacturing Defectivity*

Critical area analyses (CAA) have become increasingly popular tools in yield modeling and yield predictions. Standard CAA simulators perform checks on all metal and interconnect layers to determine areas that are most vulnerable to *random* defects formation. CAA considers two types of scenarios: connection "opens" and connection "shorts" (bridging). For a range of defect sizes, CAA generates areas for each layout layer that are susceptible to "open" and "short".

The combination of CAA with layout analyses can be a useful approach for factoring in both *random* and *systematic* defects. We can first define defect sizes of interest based on historical inline data of specific defect types, to simulate CAA regions. In this case study of copper hillock defects, the density of each metal layer was generated and specifically, wide metal lines that were prone to hillock formation were selected. The width of the metal line was selected based on previous learnings. We then narrowed the hotspot regions in the 1x copper metal region by combining the CAA results with dense wide metal lines to form a density map in Fig. 4A.

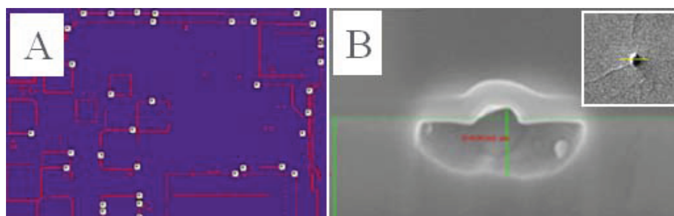

Fig. 4. A) Multi-dimensional considerations combining second-level 1x metal (M2) density and critical area analyses. The final M2 critical area density map overlaps with defectivity observed in the manufacturing line; B) Cross-sectional scanning electron micrograph showing the wide M2 hillock defect. Inset: top-view of the hillock defect.

Inline defect scans revealed the occurrences of defects (white dots in Fig. 4A) that fall within our predicted hotspot regions obtained from our multi-dimensional CAA enhanced layout analyses. Cross-section scanning electron micrography confirmed the defect as a copper hillock.

C. *Combining Multi-Layers Layout Analyses and Process Simulations Narrow Down CMP Hotspots*

Copper CMP and the dual damascene process have become the standard in BEOL planarization. Several process models have been proposed to simulate the uniformity of the metal and dielectric thicknesses after polishing [7-8]. While local pattern density within a single layer can affect CMP performance, we observed that accumulated topography and the interaction between multiple metal layers are also important factors to consider.

In this case study, LEAPS was used to refine and filter regions highlighted by standard CMP simulator. Fig. 5A is an example of a region highlighted by simulation. Multi-layers layout analyses were used to calculate and accumulate a density stack map of the most sensitive metal layers. The density weighting k_j was the same for each metal layer to reflect equal contributions. From this accumulated density map in Fig. 5B, the area of interest was refined further as the parallel wide metal lines (high density>90%, red) with adjacent spaces (low density 10-20%, blue). In Fig. 5C, based on enhanced layout checks for spaces exactly fulfilling minimum design rule with wide metal stacks (N>=2), the hotspots were identified. The hotspot location showing upper dense narrow metal lines (with minimum design rule spaces and widths) landing on dished areas between wide metal line stacks.

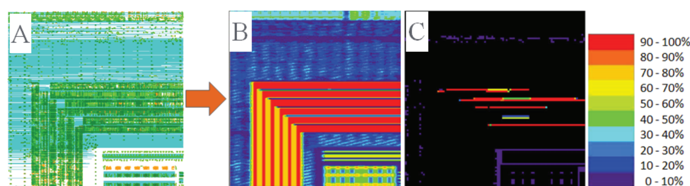

Fig. 5. A) Region highlighted by CMP simulator, B) Refined accumulated metal layers density showing horizontal wide metal lines with greatest density gradient, C) Enhanced layout analyses for minimum design rule spaces were incorporated into the density map, and enabled filtering to specific identified hotspots.

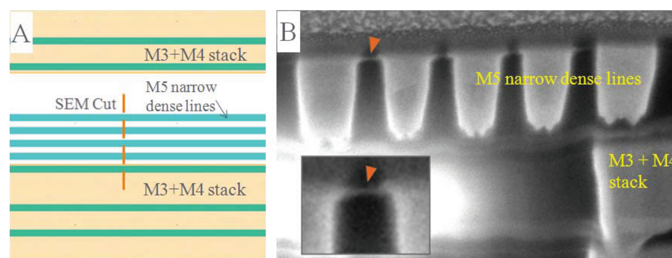

Fig. 6. A) Design layout of the process hotspot identified from Fig. 5C – upper dense narrow M5 metal lines with minimum design rule width and space, flanked by underlying wide M3+M4 metal stack; B) SEM cross-section showing metal bridging (arrows) at the M5 dense lines. Inset: zoomed in view of a bridging location.

The design layout of this process hotspot is shown in Fig. 6A. Although standard design rules were met, based on our manufacturing experience, this type of process hotspot was prone to bridging due to metal under-polishing, as confirmed by the cross-sectional scanning electron micrograph (SEM) in Fig. 6B. Thus, one could assign a higher weighting factor (k_i >1, k_j >1) to the silicon-verified, frequently detected hotspots based on feedback from the manufacturing line.

IV. Conclusions

The results from our work demonstrate the synergy in combining process simulation with layout analyses. By taking multi-dimensional analyses into consideration, LEAPS is a useful toolbox for filtering manufacturing hotspots from noise. LEAPS can also increase layout awareness. In the future, LEAPS may also enable the detection of process hotspots at the design stage and help to refine the foundry's design rules towards manufacturability with greater ease.

Acknowledgments

The authors are grateful to Mingli Yang and Summer Boo for helpful discussions.

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