3-D Modeling of Fringing Gate Capacitance in Gate-all-around Cylindrical Silicon Nanowire MOSFETs

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***Abstract*—In this paper, an analytical model for fringing gate capacitance in gate-all-around cylindrical silicon nanowire MOSFETs (SNWTs) is proposed. The fringing gate capacitances of the SNWT are divided into three parts: sidewall capacitance C_{side}; parallel capacitance C_{gsd}; perpendicular capacitance C_{gex}. Each capacitance is calculated using the following methods: conformal mapping, integral and non-dimensionalization. The proposed model is verified with a three-dimensional field solver, Raphael. Based on the proposed model, the fringing capacitance can be easily predicted in the vertically and horizontally stacked multi-wire SNWTs.**

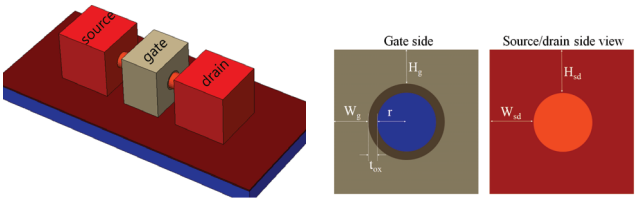
I. Introduction

As the traditional planar MOSFET continues to scale down [1], the control of short-channel effects becomes increasingly difficult in planar-bulk architecture. Recently, the gate-all-around silicon nanowire MOSFET (SNWT) is attractive due to the following: its high immunity to short-channel effects, drain induced barrier lowering, high gate controllability, and reduction of leakage current [2]. The gate capacitance of a transistor is an important factor in determining the circuit performance with respect to the intrinsic delay in digital circuits and the transit frequency of analog circuits. Outer fringing capacitances become significant portion of the total gate capacitance, since the device gate length is reduced to below 90 nm [3]. Former fringing capacitance models in planar structure cannot predict the capacitance of 3-D structure like SNWT. Jibin et al. [4] derives parasitic gate capacitance models using equivalent transformation and inversion of Schwarz-Christoffel mapping. In this paper, we derive analytic outer fringing capacitance models using conformal mapping [5], [6], integral method [7], and non-dimensionalization technique [8] for the SNWT structures. Using non-dimensionalization technique with the dimensionless parameter created from the product of physical variables, we reduce the number of fitting parameters. The accuracy of the developed model is verified with 3-D field solver called Raphael [9].

II. Capacitance Modeling

A. Fringing Capacitance component

A three-dimensional structure of a single-wire SNWT structure is shown in Fig. 1(a). An SNWT structure with source/drain extension regions between an undoped channel and a heavily doped source/drain is considered. Its cross sectional view of the top and side is shown in Fig. 1(b) and



(a) (b)

Fig. 1. (a) Three-dimensional schematic of a SNWT structure. (b) Gate and Source/Drain side view of SNWTs. H_g represents the height of the gate and W_g represents the width of the gate along the horizontal direction.

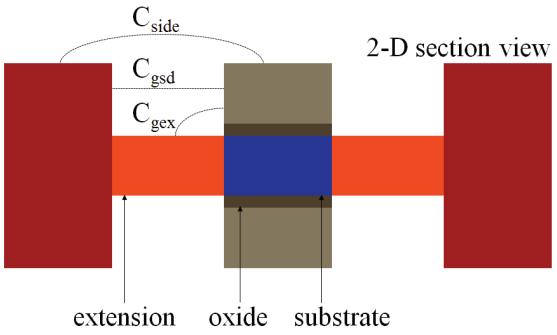


Fig. 2. Two-dimensional sectional view of SNWTs. The outer fringing capacitance (C_{of}) is divided into three part, i.e., C_{side}, C_{gsd}, and C_{gex}. The basic assumption is that source and drain side are equal. We can find the C_{of} by considering one side.

Fig. 2. The fin radius is defined as r. t_{ox} is the thickness of the gate oxide surrounding the fin. H_g represents the vertical gate height, and W_g represents the width of the gate along the horizontal direction. H_{sd} and W_{sd} are source/drain height and width in the gate direction. Length of source/drain, extension and substrate region is L_{sd}, L_{ext}, and L_g. For multi-wire SNWTs, most capacitances can be acquired by the superposition of a single-wire SNWT. Therefore, in this paper, we will mainly study the capacitance modeling of a single-wire SNWT. The total outer fringing capacitance is the sum of C_{side}, C_{gsd}, and C_{gex} (1).

$$C_{of} = C_{side} + C_{gsd} + C_{gex} \tag{1}$$

C_{side} is the sidewall capacitance between the gate and the

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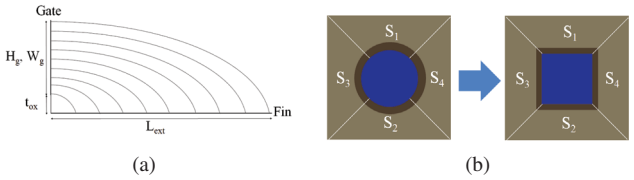


Fig. 3. (a) Electric field lines between the sidewall of the gate and the S/D extension region. Dashed lines present C_{gex}. (b) The gate sidewall is empirically divided into four parts (S_1-S_4). To use conformal mapping method, nanowire fin can be approximated as a rectangular structure.

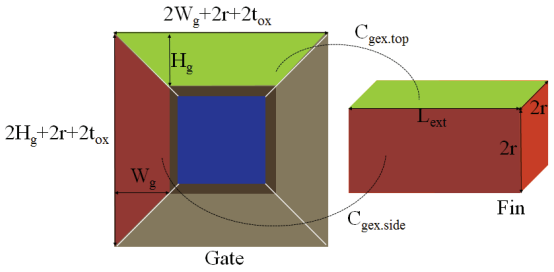


Fig. 4. Schematic of the C_{gex} calculation method. $C_{gex.top}$ contains S_1 and S_2 parts. $C_{gex.side}$ contain S_3 and S_4 parts.

source/drain region; C_{gsd} is the parallel capacitance between the gate and the source/drain region; C_{gex} is the rectangular capacitance between the gate and the extension region.

B. Analytical modeling using conformal mapping

In order to simply define the analytical model of the complex electrostatic system between the gate, source/drain extension region, and source/drain region, it is assumed that the extension region, source/drain, and the sidewalls of source/drain are uncorrelated in deriving the total outer fringing capacitance. Thus, we can divide total outer fringing capacitance into C_{side}, C_{gsd}, and C_{gex}, as mentioned. The sidewall capacitance C_{side} is formed by the top, bottom, and two-side surface along the direction parallel to channel region, so that the C_{side} is derived by multiplying circumference of the gate and C_{side} per unit distance (2).

$$C_{side} = \frac{\epsilon_{di}}{2\pi} \ln(1 + \frac{2L}{L_{ext}}) \times 4(W_g + H_g + 2r + 2t_{ox}) \quad (2)$$

C_{side} per unit distance which consist of two coplanar plates can be calculated using the integral method in two equal plates ($L=L_{sd}=L_g$). The system of two unequal plates can be transformed into the two equal coplanar plates by applying the empirical equation L over L_{ext}. The empirical equation can be defined by the non-dimensionalization method (3).

$$\frac{L}{L_{ext}} = 31.02 \left[\frac{\sqrt{(L_{ext} + L_g)(L_{ext} + L_{sd}) L_g L_{sd}}}{(L_{ext} + L_g + L_{sd}) L_{ext}} \right]^{1.4} \quad (3)$$

The parallel capacitance, C_{gsd}, represents the electric coupling between adjacent sidewalls of the gate and source-drain regions. We can model C_{gsd} as two parallel plates with effective

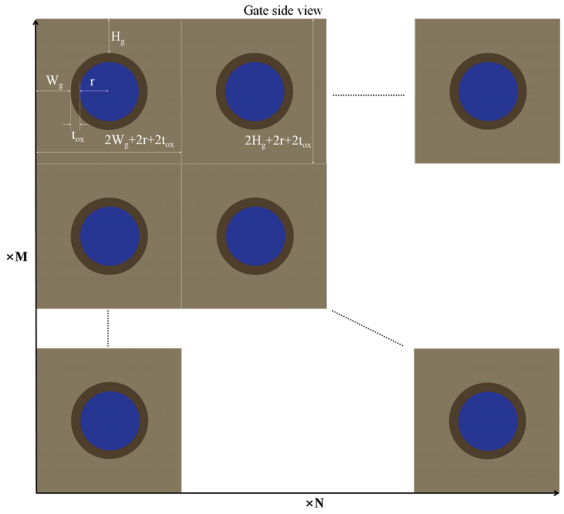


Fig. 5. For multiwire SNWTs, W_g and H_g are the half of the thickness between adjacent wires. Number of stacked wire each side is N and M.

area and distance (4).

$$C_{gsd} = \epsilon_{di} \frac{4(H_g + t_{ox} + r)(W_g + t_{ox} + r) - \pi(r + t_{ox})^2}{L_{ext}} \quad (4)$$

The analytical equation for C_{gex} is derived by transforming the electric field into equivalent quasi-confocal elliptical system, as shown in Fig. 3(a). Fig. 3(b) shows the transformation of fin and oxide. We can approximate the circular fin into quadrangle fin, and empirically divide into four parts (S_1-S_4) to use conformal mapping. C_{gex} is formed by $C_{gex.top}$ which contains S_1 and S_2 and $C_{gex.side}$ which contains S_3 and S_4, as shown in Fig. 4 and in (5).

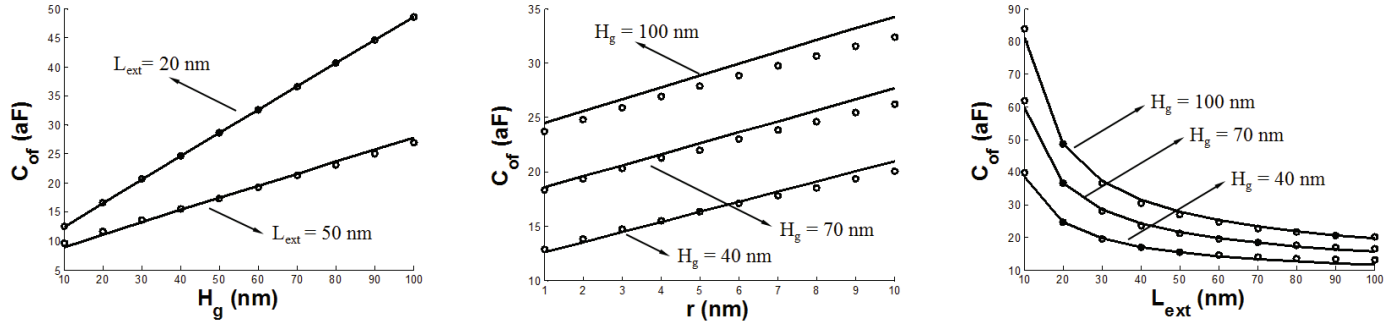
$$C_{gex} = 2(C_{gex.top} + C_{gex.side}) \quad (5)$$

To model the analytical equation C_{gex} precisely, it can be assumed that $C_{gex.top}$ and $C_{gex.side}$ are not related to each other. $C_{gex.top}$ and $C_{gex.side}$ are calculated by conformal mapping and empirical fitting parameter, η and δ (6)-(9). $C_{gex.top}$ and $C_{gex.side}$ per unit distance can be obtained by conformal mapping method between two perpendicular planes in ideal case. H_g, W_g, t_{ox}, and L_{ext} are part of the two ellipses of the same focus without any electrical interference. The empirical parameter η denotes the compensation of the focus offset from the difference from the ideal ellipse. In order to expend the $C_{gex.top}$ and $C_{gex.side}$ which contain the trapezoidal plane as shown in Fig. 4 from $C_{gex.top}$ and $C_{gex.side}$ per unit distance, we can define the equation δ that consists of parameters related thickness: W_g, H_g, r, and t_{ox}.

$$C_{gex.[top,side]} = \frac{2\epsilon_{ox}}{\pi} \delta_{[top,side]} \times \ln \left[\frac{t_{ox} + \eta_{[top,side]}[H_g, W_g] + \tau_{[top,side]}}{t_{ox}} \right] \quad (6)$$

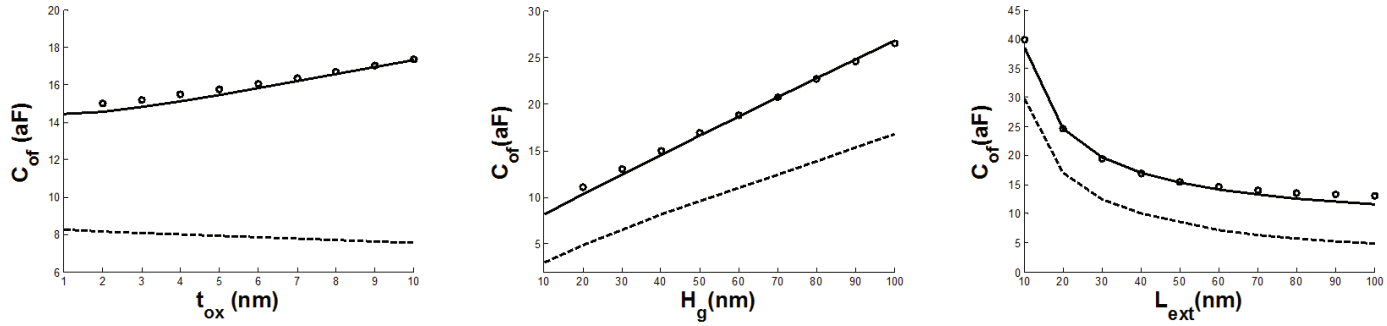
where

$$\delta_{[top,side]} = \frac{[W_g, H_g]}{2\pi} + 2r + \frac{2t_{ox}}{\pi} \quad (7)$$



(a) (b) (c)

Fig. 6. Comparison between the outer fringing capacitandce model (lines) and the 3-D numerical simulation results (symbols) as a function of various device parameters. (a) C_{of} verification at L_{ext} = 20 nm and 50 nm. (b) and (c) C_{of} as a function of r and L_{ext} at H_g = 40 nm, 70 nm, and 100 nm.



(a) (b) (c)

Fig. 7. Comparision with simulation results and a reference model (dash). C_{of} as a function of t_{ox}, H_g, and L_{ext}. H_{sd} and W_{sd} are assumed to be equal to H_g and W_g in fig. 5(a)-(c).

$$\tau_{[top,side]} = \sqrt{(\eta_{[top,side]}[H_g, W_g])^2 + 2\eta_{[top,side]}[H_g, W_g]t_{ox}} \tag{8}$$

$$\eta_{[top,side]} = 3\pi \exp\left[\frac{L_{ext} - \sqrt{[H_g, W_g]^2 + 2[H_g, W_g]t_{ox}}}{L_{ext}}\right] \tag{9}$$

Based on (1)-(9), the expression of outer fringe capacitance can be derived in multi-wire SNWTs, as shown in Fig. 5. The number of the channels connected in parallel along the vertical and horizontal direction is defined as N and M. H_g and W_g represent the half of the gate electrode thickness in between adjacent wires. The total outer fringing capacitance in multi-wire SNWTs $C_{of.m}$ is the sum of the rectangular capacitance, the parallel capacitance, and the sidewall capacitance as same component as a single-wire SNWT (10). The rectangular and parallel capacitances are derived by the multiplying C_{gex} and C_{gsd} by the number of wires. The sidewall capacitance represents the multiplying unit length of C_{side} by the circumference of the gate in multi-wire SNWTs. In case of M and N are 1, $C_{of.m}$ is same as total outer fringing capacitance in a single-wire SNWT.

$$C_{of.m} = (C_{gex} + C_{gsd}) \times MN + C_{side} \times \frac{M(H_g + r + t_{ox}) + N(W_g + r + t_{ox})}{W_g + H_g + 2r + 2t_{ox}} \tag{10}$$

In addition, $C_{of.m}$ over M and N is the outer fringing capacitance per unit number of channel in multi-wire SNWT (11). The rectangular and parallel capacitance per wire is the same as C_{gex} and C_{gsd}. On the other hand, since the fraction multiplied by C_{side} has a value less than 1, the sidewall capacitance per wire is smaller than C_{side}. Thus, multi-wire architecture should be preferred than the single-wire architecture from the perspective of reducing the gate fringing capacitance.

$$C_{of.m}/MN = C_{gex} + C_{gsd} + C_{side} \times \frac{W_g/M + H_g/N + r(\frac{1}{M} + \frac{1}{N}) + t_{ox}(\frac{1}{M} + \frac{1}{N})}{W_g + H_g + 2r + 2t_{ox}} \tag{11}$$

III. Simulation Results

The accuracy of this outer fringing capacitance model is verified over a wide range of geometrical parameters such as H_g, r, L_{ext}, and t_{ox} by 3-D numerical simulations. Excellent agreement is achieved with the proposed model, as shown in Fig. 6. Fig. 7 also shows that the proposed model has better accuracy than the model in the reference paper by Jibin et al. compared to 3-D simulation results. Fig. 8 shows the proposed model validation for multi-wire SNWTs. There is a good agreement between the modeled results and Raphael 3D simulated results for M and N variations. For larger N, the total gate capacitance increases. However, the total gate capacitance per width decresaes due to C_{side} differences, as shown in Fig.

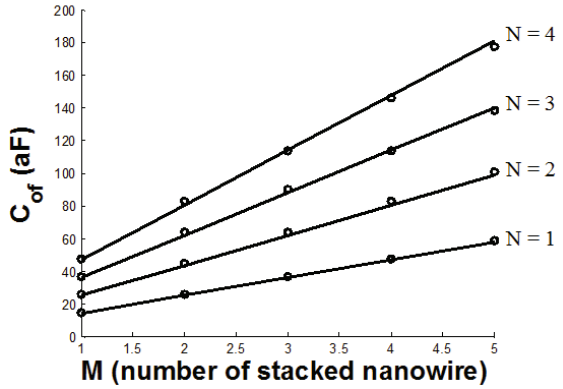


Fig. 8. Comparison between the outer fringing capacitandce model (lines) and the 3-D numerical simulation results (symbols) as a number of stacked nanowire.

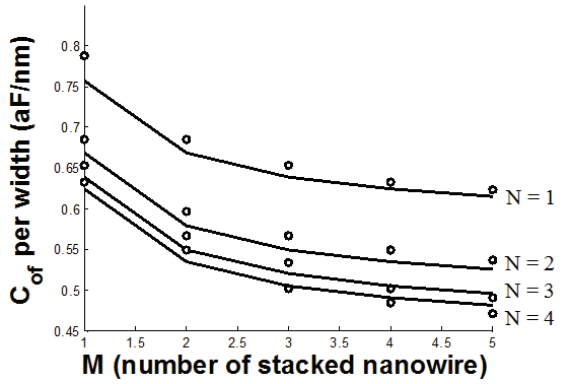


Fig. 9. Comparison between the outer fringing capacitandce model (lines) and the 3-D numerical simulation results (symbols) per wire as a number of stacked nanowire.

9. In addition, Fig. 10 shows the change of $C_{of.m}$ as a function of total gate width over a radius for 3 by 3 multi-wire SNWTs. For radii of 3, 4 and 5, excellent accuracy of $C_{of.m}$ is obtained, and the contribution of fringing capacitance can be reduced by reducing the radius of a single wire when wire pitch are kept constant.

IV. Conclusion

In this paper, a comprehensive model for parasitic outer fringing gate capacitance is proposed for gate-all-around cylindrical SNWTs. The proposed analytical model can be implemented as a compact model for accurate circuit simulations. In the development of fringing capacitance model, a practical SNWT structure was considered with the gate, source/drain, and extension regions. We analyze the effects of geometrical parameter variation on the fringing capacitance of SNWTs. The total 3-D fringing capacitance is decomposed into two-dimensional components each of which is derived with a conformal mapping technique, integral and non-dimensionalization method. The accuracy of the proposed model is verified with the results of three-dimensional field solver, Raphael.

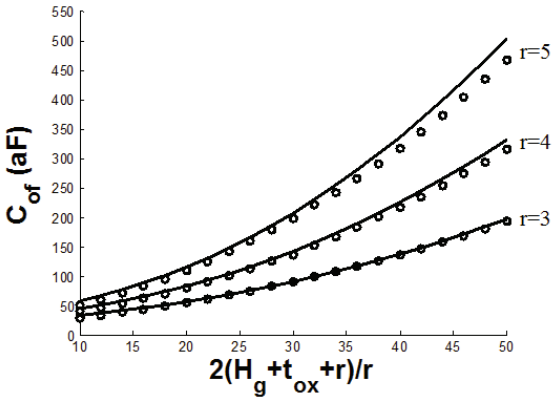


Fig. 10. The outer fringing gate capacitance for 3 by 3 multi-wire SNWTs as a function of total gate width for different radii.

V. Acknowledgement

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