TCAD study of Single Photon Avalanche Diode on 0.35µm High Voltage Technology

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***Abstract* — This paper presents the electrical and optical behavior of Single Photon Avalanche Diode. Key parameters as reverse breakdown voltage, spectral responsivity, photon detection probability, dark count rate and time delay of the diode are extracted from dedicated TCAD simulations.**

Keywords — SPAD; TCAD; Geiger-mode; Breakdown; time delay; DCR; PDP;

I. INTRODUCTION

Sensors detecting low photon counts need devices with a high optical to electrical gain. Geiger mode avalanche photodiodes, also known as SPADs (Single Photon Avalanche Diode), are suitable for these applications with the additional advantage that they can be integrated in standard CMOS high voltage IC technologies. The aim of this article is to study the SPAD timing behavior by TCAD [1].

II. SPAD STRUCTURE AND ELECTRICAL BEHAVIOUR

SPAD devices are used for applications [2] where the signal to be detected consists of few tenths of photons or less. These devices operate in Geiger mode [2] (see Fig. 1) by biasing the junction above its breakdown voltage. At this bias, the electrical field in the space charge region (SCR) can reach up to 500-700kV/cm and a charged pair (generated after the absorption of a photon) injected in the depletion layer may trigger a self-sustaining avalanche, generating a current pulse in the mA range, thus providing infinite gain.

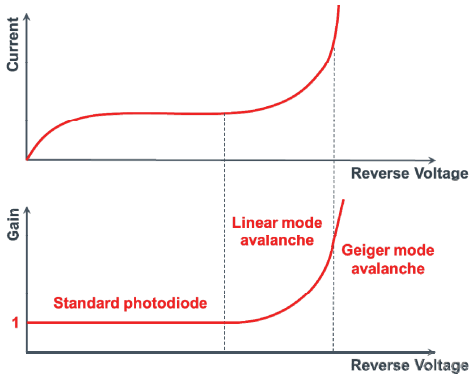

Fig. 1. Photodiode current and gain regions versus applied voltage.

To maximize the area of the avalanche region the field distribution must be as uniform as possible. One viable approach is to use a buried junction built in a 0.35µm high voltage technology in our case. In these diodes, a shallow N type implant is placed close to the surface, suppressing surface leakage current generated by the photons into the depletion region; additionally, a P type implantation is used for counter doping of the N layer and tunes the breakdown value to the desired value of 11V. A deeper and lower doped N type ring is placed surrounding the shallow N layer for preventing premature edge breakdown by lowering the electrical field at the edge of the cathode.

Fig. 2 presents a 2D simulation of the proposed diode operating at breakdown (11V); Fig. 2.a shows the net doping of the diode with a shallow N type implant layer being the cathode of the diode (N+), a Shallow P type counter doping (SP) and an N type lightly doped ring (N-well Guard). Fig. 2.b shows the high and homogeneous electrical field surrounding the junction ensuring the Geiger mode operation in the central part of the diode.

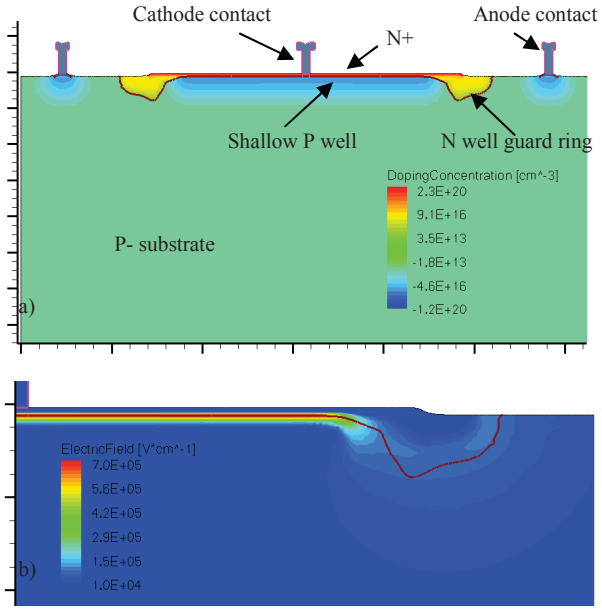

Fig. 2. N+ to substrate buried avalanche diode with Nwell guard ring, a) doping concentration, and b) Electrical field distribution when the diode is operated in breakdown.

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III. Impact of the Light Absorption Location on the Diode Timing

The spectral responsivity of the diode at low bias is shown in Fig. 3. For this type of diode a maximum peak at a wavelength of 720nm can be observed.

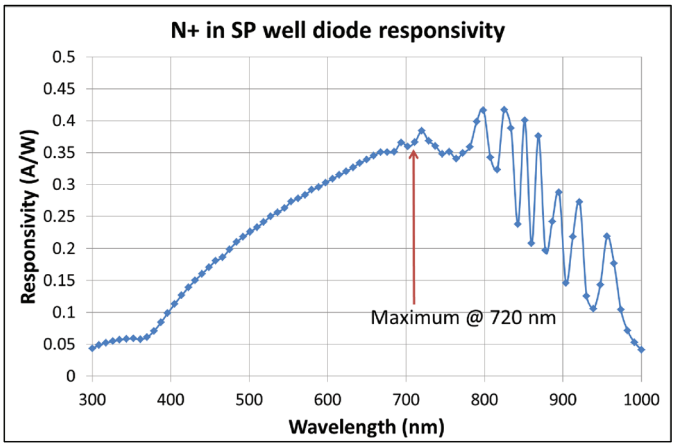

Fig. 3. Spectral responsivity of the diode.

In order to evaluate the possibilities and performance of different junctions prior to fabrication, it is beneficial to calculate critical parameters for the SPADs, such as Dark Count Rate (DCR) and Photon Detection Probability (PDP). In order to do that, ionization factors need to be extracted by analyzing electrical and Shockley-Read-Hall (SRH) recombination profiles from the TCAD simulations. Therefore, to calculate the PDP and the DCR, it is needed first to get the avalanche probabilities. We have implemented a numerical method from [3] in order to calculate the avalanche probabilities based on the ionization factor profiles.

Indeed, the avalanche probabilities depend on the overvoltage through the ionization factors. For the junction shown in Fig. 2, the avalanche probabilities versus the voltage around the breakdown voltage are depicted in Fig. 4.

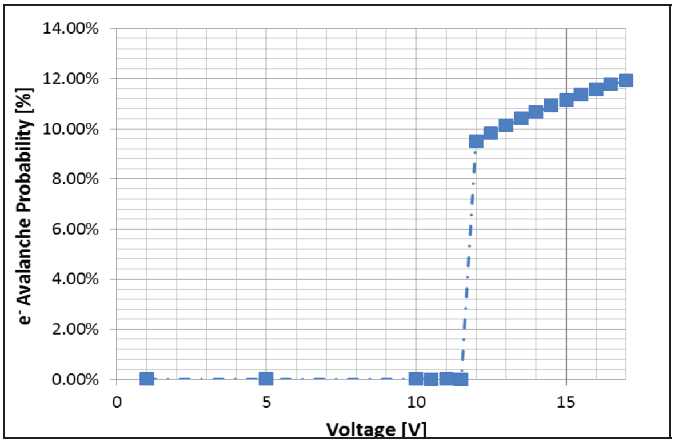

Fig. 4. Electron avalanche probability versus voltage.

The PDP is obtained from the product of the quantum efficiency by the avalanche probability according to the following equation:

$$PDP(\lambda,V) = \eta_l(\lambda) * P_e(V) \quad (1)$$

It is also possible to extract the DCR from the TCAD results. In that case, we use the expression (2) based on [3] and by considering the SRH generation as the main factor determining the DCR.

$$DCR_{SRH} = A \cdot \int_0^W P_e(x) \cdot G_{SRH}(x) \cdot dx \cong A \cdot P_e(x) \cdot \int_0^W G_{SRH}(x) \cdot dx \quad (2)$$

The DCR versus the voltage is represented in Fig. 5. This curve combined with the Quantum Efficiency of the diode and the probability of the electrons of the diode to generate avalanche carriers allows to calculate the PDP curve by using the model described in [3] (see Fig. 6).

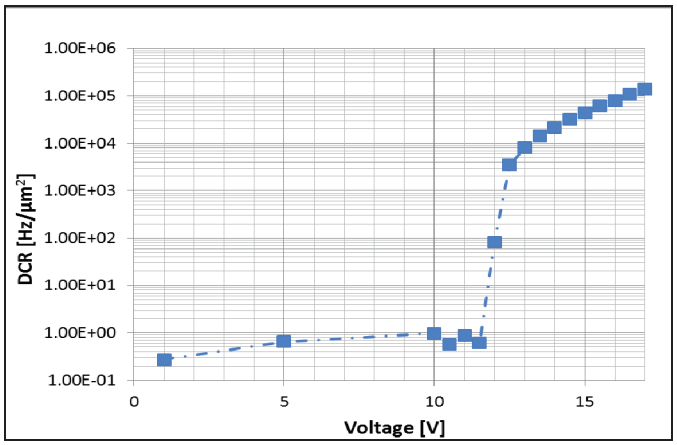

Fig. 5. DCR of the SPAD around the breakdown.

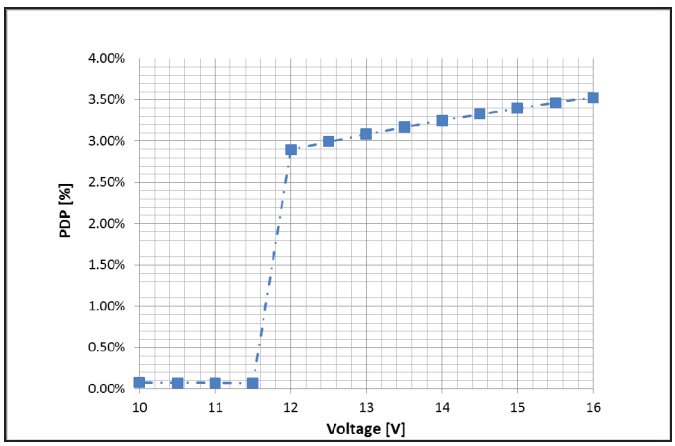

Fig. 6. PDP of the SPAD around the breakdown.

In order to study/evaluate the impact on the diode response time characteristics of the position where the photon is absorbed, a novel procedure for TCAD simulation had been developed by using the commercial TCAD simulation tool sDevice [1].

First, a small box (~400x100nm²) is introduced in the structure and is specified as a light source. Then, several new structures are generated by varying the placement of the box within a range of 100nm below the silicon surface down to 5µm deep into the silicon and laterally up to 30µm away from the center of the diode towards the anode/substrate contact (see Fig. 7).

The CDensityMin parameter of sDevice (controlling the minimum current density for which impact ionization is considered) in the math section of the simulation command file is set accordingly to prevent any avalanche triggering under dark conditions.

The device is connected to a passive quenching circuit, consisting of a high resistance resistor connected to the anode contact. The device is biased and kept at an overvoltage of 2V above its intrinsic breakdown till the end of the transient simulation, ensuring Geiger mode operation.

After initially allowing the diode to settle into its quasi-static state above breakdown, a light pulse (corresponding to a few tenths of photons) is applied in the small box.

The electrical and optical simulation sequence is shown in Fig. 8, where we ensure that before each critical step as the voltage of the diode increases up to the breakdown plus overvoltage and the light pulse is applied, the diode is recovering into its quasi-static state.

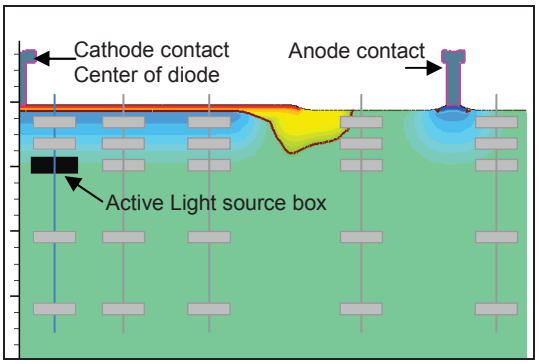

Fig. 7. N+ SPAD device with different box location for light source.

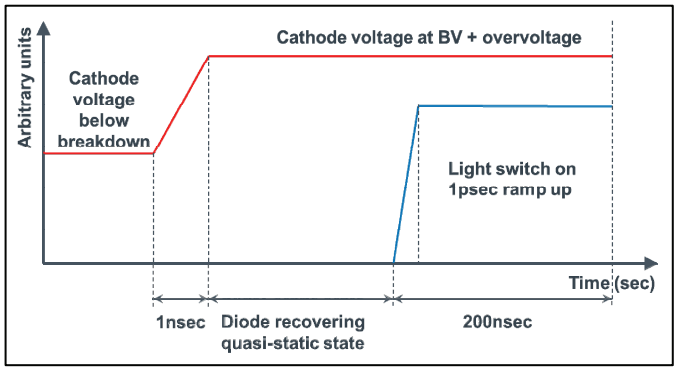

Fig. 8. Electrical and light transient simulation setup.

Fig. 9 shows the evolution of the cathode current of the SPAD diode when the light is switched on at different locations within silicon substrate, either along the surface from the center of the diode to outside the diode close to the substrate contact or at 5µm depth at the center of the diode.

We observe the diode needs some time to react and initiate current in the cathode depending on the placement of light source. The minimum delay (from 10 to 40 picoseconds) is seen when the light source box is placed close to the diode surface or close to the SCR of the diode. Longer delays are seen when the box is placed deeper in silicon or outside the active part of the diode like in the guard ring and in the anode contact area.

A systematic extraction of the time delay of the diode versus the vertical/lateral light box position is presented in Fig. 10. As seen before, the diode starts to react to the photons after 20ps and stays below 40ps till the light source reaches the SCR of the diode (which is 1µm wide). We interpret this as a good approximation for the avalanche initiation time of the element. When the photon absorption takes place below the SCR in the silicon, the delay increases because of the time needed by the carriers to diffuse into the SCR of the diode and initiate avalanche. Longer delay (2 to 3 decades higher) is observed when the absorption is taking place in the guard ring or outside the diode area.

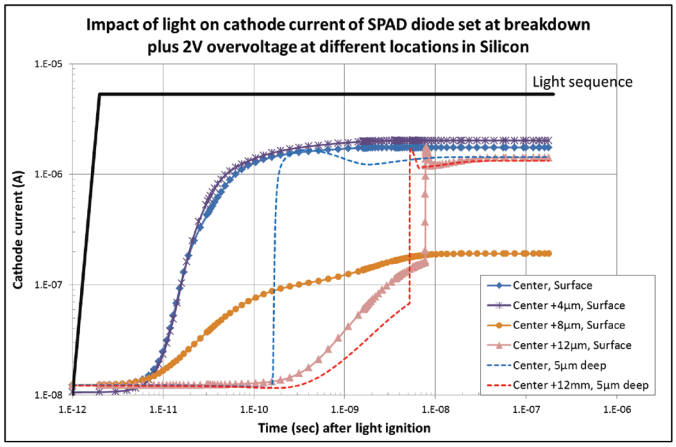

Fig. 9. Cathode current evolution when the SPAD diode is at breakdown plus two volts overvoltage, at different location in silicon.

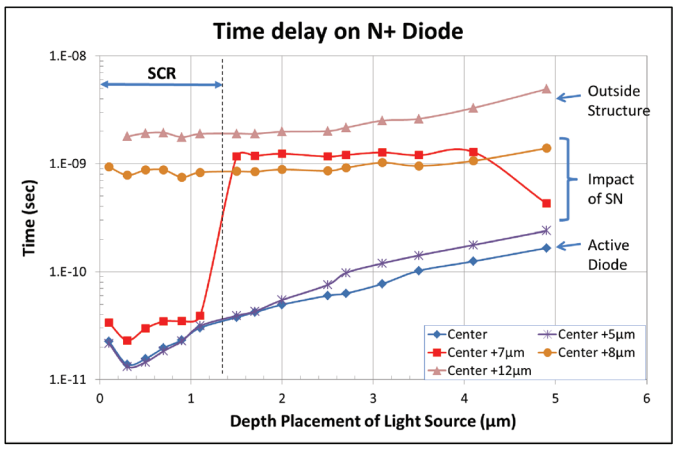

Fig. 10. Time delay response of the SPAD diode.

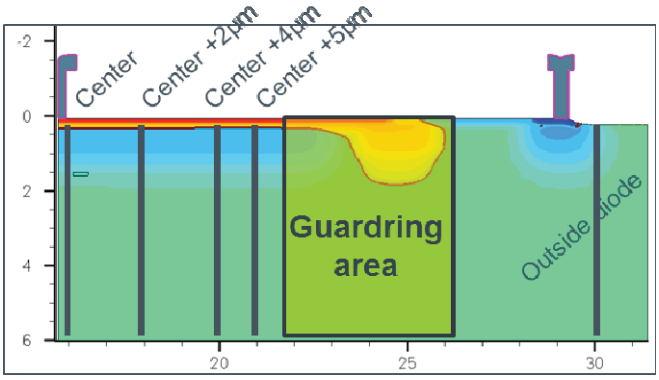

Fig. 11. Visualization of sensitive areas in the structure.

For avoiding such large delays, any light absorption within these areas of the element must be suppressed, by e.g. metal shielding. This helped us in identifying the most sensitive areas visualized in Fig. 11 for further optimization.

IV. Conclusion

This work describes an extension of the available commercial TCAD codes to model discrete effects in SPADs. Key parameters describing the SPAD devices can be simulated with TCAD tools such as standard electrical characteristics of the diode (reverse breakdown and its optimization) but also the interaction of the diode with photons such as spectral responsivity of the diode, photon detection probability around the breakdown and dark count rate. Systematic transient simulation of the impact of light source placement helps to determine the minimum time response of the diode, and to estimate the real time response trend within it.

Optimization of the devices in terms of breakdown, SCR width, their CMOS integration along with their active quenching circuitry and the comparison to experimental data will be part of future work.

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