Fast 3D Electro-Thermal Device/Circuit Simulation Based on Automated Interaction of SDevice and HSpice Simulators

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***Abstract*— Automated interaction of SDevice and HSpice for fast 3D electro-thermal simulation based on the relaxation method is designed. The features and limitations of the method are analyzed and presented. A power vertical super-junction MOSFET under the unclamped inductive switching (UIS) test of device robustness is used to perform validation of the designed electro-thermal simulation.**

Keywords— 3D electro-thermal simulation, SDevice, HSpice, super-junction MOSFET, UIS test.

I. INTRODUCTION

Today's device and circuit simulators are standard tools in the development, characterization and optimization of electronic systems and devices. However, device finite element method (FEM) electro-thermal simulations are very time-consuming and require powerful hardware equipment mainly in the case of complicated 3D structures. Circuit simulations have been limited to electronic functions because the temperature dependences of parameters of simulation models available today are taken into account at the best by changing the static global temperature. In the power-electronic systems in particular, temperature is one of the critical parameters due to the non-negligible self-heating effects and the fact that many properties of power semiconductor devices are strongly temperature dependent [1]. To be able to simulate the inherent heating dynamically, introduction of an equivalent thermal circuit, e.g. *RC*-network and its interactive coupling with the electrical model has to be implemented. However, this direct method usually takes into account 1D heat flow. Assumption of 1D heat flow may be insufficient for power devices and large power loads in which an inhomogeneous temperature distribution caused by 3D heat flow the from semiconductor chip to the package and cooling assemblies can cause an inhomogeneous distribution of the electric properties of the power device along the whole chip. Building up a 3D equivalent thermal mesh is difficult and requires structure simplification [2]. Moreover, in the case of the thermal linear network the nonlinear behaviour of semiconductor materials is not taken into account. Neglecting the nonlinear thermal properties of silicon leads to a significant error in the transistor temperature estimation [3]. The relaxation method for electro-thermal simulation is based on coupling the separately solved thermal and electrical equations. The FEM is used for thermal simulation and a Spice-like program is used for electrical simulation. Only synchronization and data transfer need to be provided [4-5]. The advantage of the method is the speed up of the simulation time for full structure analysis.

In this paper we present automated interaction of SDevice and HSpice for fast 3D electro-thermal simulation based on the relaxation method. The complex system of the device consisting of a silicon chip, lead frame, bonding wires, package and external cooling assemblies is used for 3D thermal simulation in Synopsys TCAD Sentaurus SDevice tool [6]. The electrical properties are simulated at the circuit level in HSpice. The automated interaction is provided by Linux shell script directly supported in Synopsys TCAD Sentaurus. The multipulse UIS test [7] is used for model verification.

II. STRUCTURE AND MODEL DESCRIPTION

The structure under investigation is the power super-junction vertical MOSFET [8-9] in DPAK 2 package (Fig. 1a). The 2D cross section of the structure is shown in Fig. 1b. The trench gate MOSFET is created on top of the n^{++}-type doped substrate and n^{-}-type doped epitaxial layer. The super-junction trench, created by p-type and n-layers around an air gap, provides charge balance and high breakdown voltage for low on-resistance. The whole silicon chip consists of several hundred pillar cells. 3D FEM simulation of such a large number of elements would be very time-consuming. Therefore, only one 2D pillar is used for device simulation. These simulation results have been used for extraction of the electrical properties and analysis of the internal behaviour of the device. Referring to [10] and device simulation (Fig. 1c) the most of heat generated during the avalanche operation of the UIS conditions is located at the bottom of the air gap epitaxial layer. The thermal contacts are placed uniformly on the epitaxial layer and substrate interface by an 8×8 square

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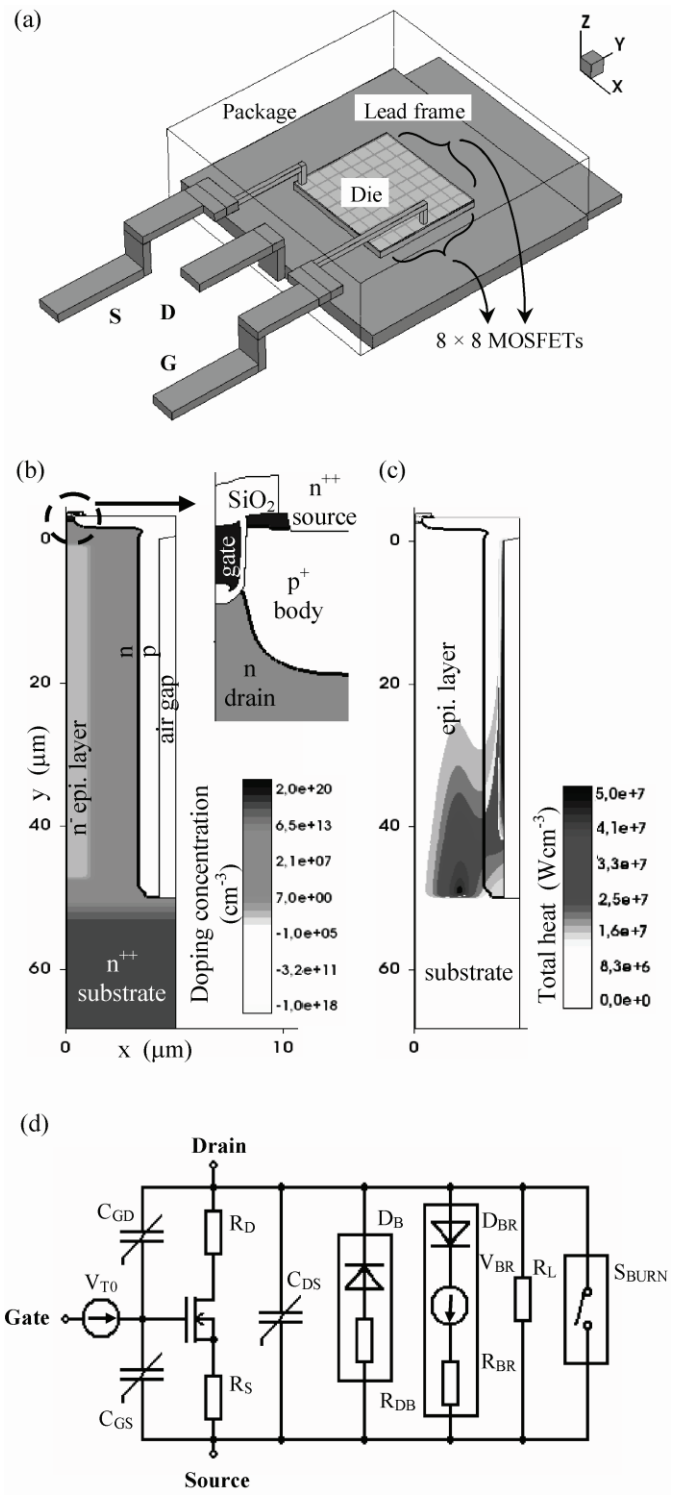

Fig. 1. (a) Thermal model of the MOSFET in DPAK 2 package with 8 × 8 thermal contacts along the silicon die. (b) 2D cross section of the super junction MOSFET. (c) Total heat distribution inside the structure during the UIS breakdown condition. (d) Electrical model of the MOSFET cell with temperature dependent parameters.

mesh. The 3D model of the structure for thermal simulation is created in Sentaurus Device Editor (SDE) [11] based on the physical and geometrical description of the packages of the

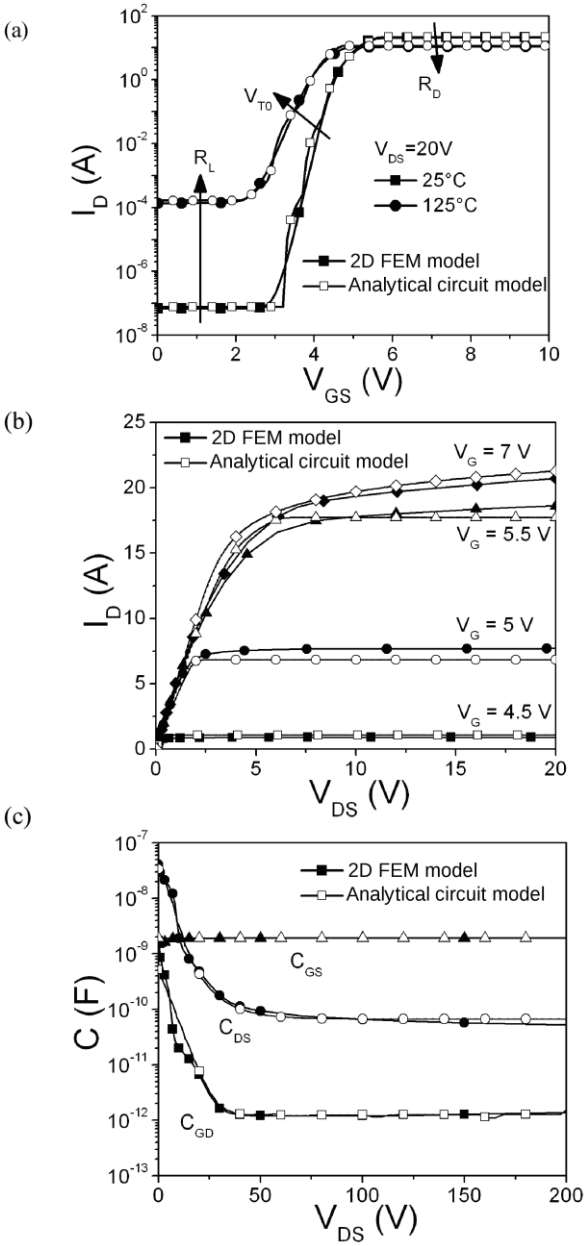

Fig. 2. 2D FEM and analytical circuit model simulation of (a) transfer characteristics at different temperatures, (b) output characteristics and (c) *C-V* characteristics of the analyzed MOSFET.

components. The thermal contacts are generated automatically by a directly supported program cycle in an input command file, which allows an easy use of the defined placement. Each contact corresponds to one MOSFET part and they are together interconnected by data transfer of local temperature and power dissipation. The structure boundary conditions are set to represent a heat sink to the surrounding environment.

The power MOSFET is electrically modelled with a SPICE Level 3 built in Verilog-A [12]. The electrical model is defined considering the temperature dependences of the most relevant parameters extracted from device simulations of the structure at different operating temperatures. The temperature dependence of the threshold voltage V_{T0}, drain resistance R_D, body diode D_B, leakage current through leakage resistance R_L, avalanche

breakdown voltage V_{BR} and over current/temperature destruction S_{BURN} are implemented in the model (Fig. 1d) [13]. Thus the created 64 MOSFETs are electrically connected taking into account parasitic resistances of the polysilicon gate electrode and metal source electrode. Fig. 2 shows 2D FEM simulation compared with analytical circuit simulations of transfer characteristics at different temperatures, output characteristics for different gate biases and *C-V* characteristics of the analyzed MOSFET.

III. Electro-Thermal Simulation

Electro-thermal simulation is based on interaction of SDevice, a FEM thermal engine and HSpice as an electrical circuit simulation program. Simulation uses the relaxation method with separate but synchronized thermal and electrical simulations. Synchronization and data transfer between SDevice and HSpice are provided by a Linux shell script. A great advantage is that the script is directly supported in Synopsys TCAD Sentaurus environment and the simulation can be easily parameterized in Sentaurus Workbench. The flowchart of the method for electro-thermal simulation is shown in Fig. 3. After setting theinitial conditions, HSpice calculates the structure power dissipation during the first time step from the current and voltage distribution for each MOSFET part. The average values of the powers generated during the time period between steps are applied to the thermal contacts and SDevice calculates heat generation and heat transfer inside the structure. The temperatures in the corresponding positions of the structure are taken to drive the temperature dependent electrical parameters of the MOSFET parts. Finally, HSpice calculates the current and voltage distributions at relevant time step for corresponding structure temperature. The whole cycle is repeated with an increment of time until the end of simulation. The time step is user defined and it is set to provide undistorted results for the least time-consuming computation.

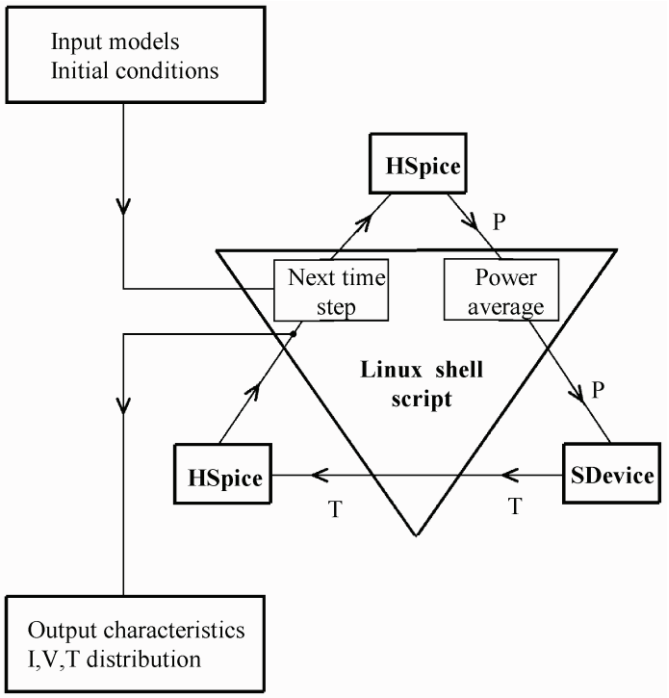

Fig. 3. The flowchart of the electro-thermal simulation. Linux shell script interconnects the SDevice, the thermal simulator of the structure and HSpice as the electrical simulation program.

IV. Experiment

The designed electro-thermal model of the analyzed power MOSFET has been used for simulation of the multipulse UIS test. UIS condition represents a robust test of circuit switching operation for evaluating the ruggedness, which characterizes the device capability to handle high avalanche currents during the applied stress. In case the current flowing through an inductance is quickly turned off, the magnetic field induces a counter electromagnetic force that can build up surprisingly high potentials across the device and the whole built-in energy of the inductor is dissipated directly into the device under test [14].

Fig. 4 shows the results of the multipulse UIS test. There are compared the drain currents and the temperatures of the transistor parts MOS11 and MOS44 which represent the corner and centre of the structure, respectively. The temperature is almost evenly distributed and the currents through the MOS11 and MOS44 transistors are equal during the first pulse. After some period of the power load, the temperature and breakdown

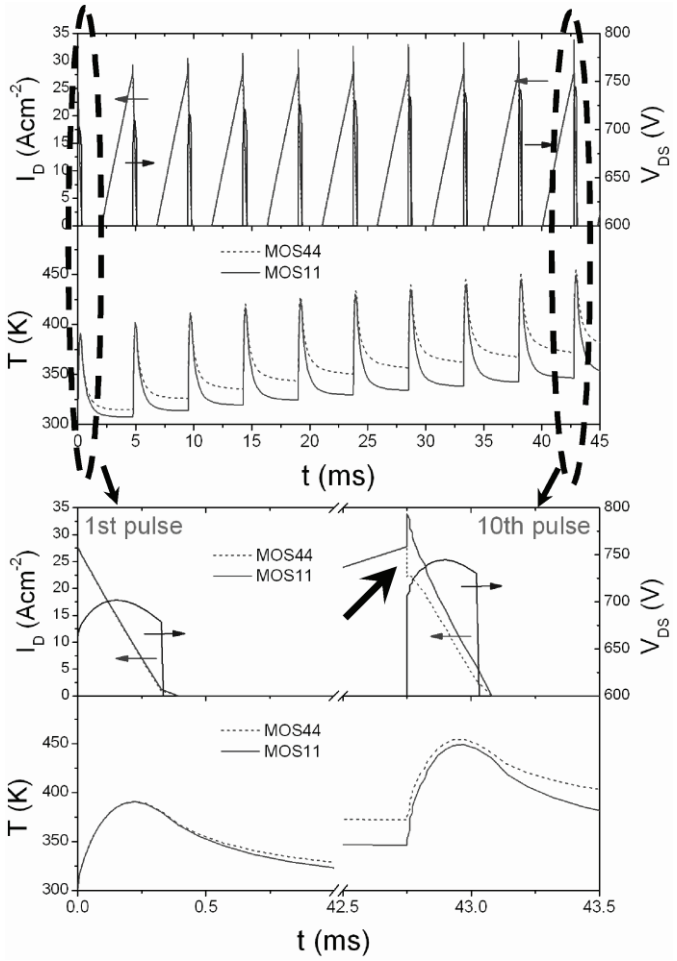

Fig. 4. Comparison of the drain current, drain voltage and temperature of the corner MOS11 and central MOS44 parts during the multipulse UIS test.

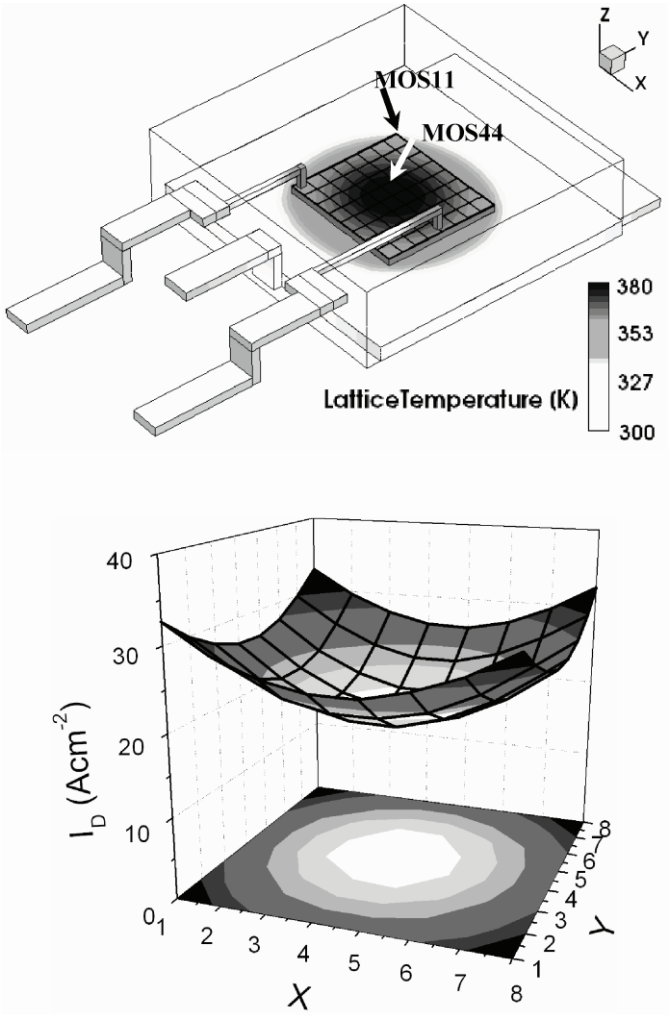

Fig. 5. Temperature (top) and current density (bottom) distributions at the beginning of the tenth UIS pulse inside the structure.

voltage of the central MOS44 transistor cell increase more significantly in comparison with the corner MOS11 transistor cell because the corner cell is cooled more effectively. Therefore, the MOS11 current becomes higher. The inhomogeneous distributions of the temperature and current are clearly seen during the tenth UIS pulse in Fig. 5.

The whole multipulse UIS electro-thermal simulation based on interaction of SDevice and HSpice takes about one hour for the designed full structure model with 75000 mesh elements. The 2D FEM simulation of one pillar cell with about 13000 elements takes about one and half hour. Moreover, the 2D simulation does not take into account the thermal flow and distributed parameters of the structure in the third dimension. The full structure FEM simulation with several hundred pillar cells would be very difficult and the simulation time would be dramatically increased. Relatively less time-consumption using the relaxation method is a great advantage for the full structure analysis.

V. Conclusions

Automated interaction was presented of SDevice and HSpice for fast 3D electro-thermal simulation. The super-junction vertical MOSFET was used for simulation of the multipulse UIS test. The simulation approach helps to assess the device robustness by means of the evaluating both temperature and current distributions in the MOSFET structures operating under critical conditions. The implemented 3D thermal flow and distributed parameters of the MOSFET provide more realistic simulation results. The advantages of the method are the relative simplicity of implementation, the speed up of the simulation time and the capability of full structure analysis.

Acknowledgment

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