Circuit-level modeling of FinFet sub-threshold slope and DIBL mismatch beyond 22nm

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***Abstract*—We propose a way of modeling device variability in sub-threshold slope and DIBL at circuit-level using dependent voltage sources. The usual way of modeling variability using threshold voltage shift and drain current amplification is becoming inaccurate as new sources of variability appear in sub-22nm devices. Benchmark experiments on circuit level, using a set of 1000 TCAD-based 10nm-FinFet device models with mismatch as a reference, show systematic accuracy improvements on mean and standard deviation of 6T-SRAM cell stability metrics of up to 30 and 10 percentage scores, respectively.**

I. Introduction

With the reduction of device sizes on future CMOS technologies the mismatch of device parameters is expected to increase and turn to play a major role. SRAMs, that occupy large areas of modern-day system on chip, are particularly sensitive to these variations. Local mismatch appears more frequently, significantly reducing the reliability of SRAMs if not considered during design.

The variability in devices is a consequence of intrinsic physical parameter mismatch. It can be fully modeled by changing the parameters in the model card of the transistor. The two-injector model [1], that uses two external power sources to modify the threshold voltage and the drain source current of the transistor, has shown reasonable accuracy for planar transistors down to the 45nm node, but with the decreasing size of the devices new mismatch sources become relevant. It has been shown in [2] that as the length of FinFet transistors drops below a critical value, the spread in the sub-threshold slope ramps up (see Figure 1) and thus has to be considered as another parameter to be modeled. The effect of DIBL (Drain Induced Barrier Lowering) in mismatched devices is already considered through the nominal device if there is no DIBL variability, but as the gate length is reduced, the DIBL mismatch becomes comparable to the threshold voltage mismatch and thus also needs to be modeled separately.

Even if less accurate, the injectors method is still useful in several cases:

1) When the statistical model card is not available (future devices) or accessible (encrypted).
2) If variability information is provided as several model cards but not properly as a statistical model, to model the devices in the tails of the distributions.
3) Injectors can also be used to modify the nominal device, linking transistor characteristics to circuit performance in order to set targets for incoming devices.

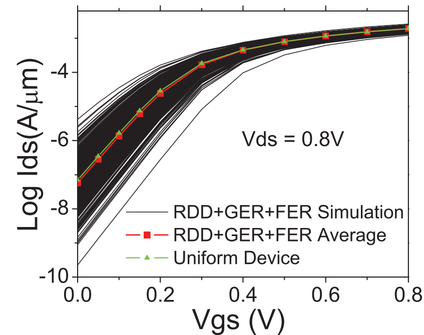

Fig. 1. I-V characteristics at Vdd=0.8V for the nMOS FinFET on logarithmic scales. The curves for the 1000 simulated devices are shown, along with the nominal uniform characteristics.

4) On top of that the parameters used for injectors correspond to electrical parameters that are directly measurable from silicon, bypassing a full statistical device compact modeling step.

In the next section we review the previous injector approach and introduce the two new injectors that we propose to use, we also explain the mismatched models that we use as a reference. The following section collects the results that we obtain with our proposal, first at low level I-V response of the transistor, and how it translates to the stability metrics of an SRAM cell and finally in the yield of a full memory. In the end some conclusions are drawn.

II. Proposal

A. Previous Approaches

When a statistical model is not available, transistor variability is usually modeled using injectors. A threshold voltage injector is the most common, completed if so by a drain current amplification injector. Threshold voltage and drain current gain injectors were first proposed in [1] and have been widely used since [3], [4].

The threshold voltage of the transistor is usually modeled by adding a constant voltage source in series at the gate of the transistor. The voltage value is equal to the difference between the threshold voltages of the nominal device and the one we want to match.

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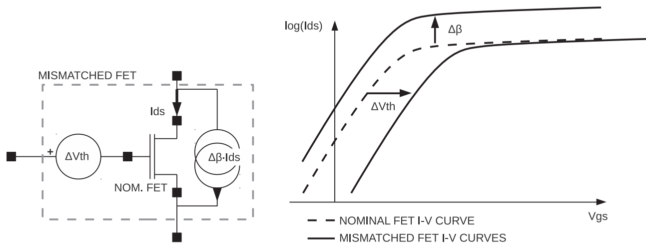

Fig. 2. Injectors ΔV_{th} and $\Delta\beta$ used to model threshold voltage shifts and drain current gain respectively, and the resulting transformations of the I-V curves.

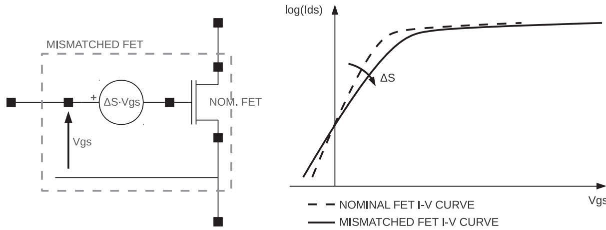

Fig. 3. Injector ΔS used to model sub-threshold slope shift, and the resulting transformation of the I-V curve.

The drain current of the transistor is usually modeled by adding a dependent current source in parallel to the drain and source of the transistor. The value of the current is a factor $\Delta\beta$ of the actual I_{ds} current that the nominal device drives. As a result the equivalent transistor that we model has a drain current $I'_{ds} = (1 + \Delta\beta) \cdot I_{ds}$. Figure 2 shows how threshold voltage and drain current injectors are added to the nominal transistor circuit, creating an equivalent mismatched transistor. Those two injectors have the effect of moving the I-V curves in the V_{gs} and $log(I_{ds})$ directions respectively, also shown in the figure.

B. New Injectors

In this work we propose to model the sub-threshold slope and the DIBL variability at circuit-level using injectors.

The sub-threshold slope can be modeled by scaling the voltage that drives the gate of the transistor by a factor $1-\Delta S$ using a voltage source dependent on the gate voltage at the input of the transistor we want to model as shown in Figure 3. A negative value of ΔS has the effect of shrinking the I-V curve and as a consequence decreasing the sub-threshold slope —a smaller S value means actually a sharper slope— a positive value would stretch the curve increasing the slope. The effect of the injector on the I-V curve is also shown in Figure 3. Instead of a $V_{gs} \cdot (1 - \Delta S)$ voltage generator placed between the gate and the source of the nominal device, a $V_{gs} \cdot \Delta S$ voltage generator in series with the gate is preferred, while the voltages involved remain the same, with the latter method even if the gate capacitance at the input of the transistor can be affected, it is not totally hidden as in the first method.

The DIBL variability can be modeled in a similar way as the threshold voltage variability. Another voltage generator is added in series at the input, as shown in Figure 4, now the voltage is proportional to the drain source voltage: $\Delta V_{th,DIBL} = \Delta DIBL \cdot (V_{dd} - V_{ds})$. $\Delta V_{th,DIBL}$ is the value

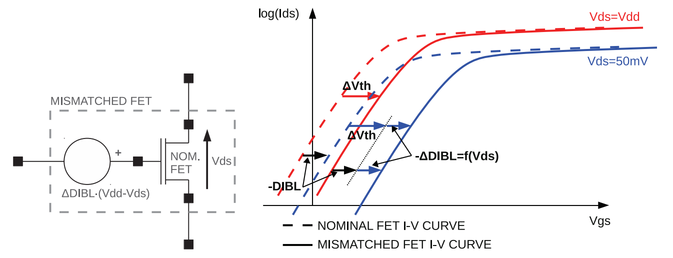

Fig. 4. Injector $\Delta DIBL$ used to model DIBL mismatch, and the resulting transformation of the I-V curve.

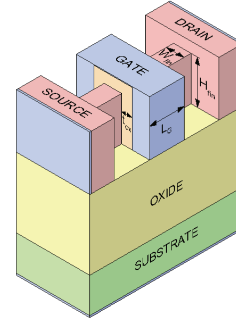

Fig. 5. Schematic of the 3D FinFET structure.

of the voltage generator, $\Delta DIBL$ is the difference between the DIBL of the mismatched transistor and the nominal one and V_{dd} is the supply voltage taken as a reference to measure the threshold voltage mismatch. As for the threshold voltage, it results on a shifting of the I-V curve in the gate voltage direction, horizontally in Figure 4. Now the magnitude of the shift increases as the V_{ds} voltage moves away from V_{dd}.

C. Reference Model

In order to check the accuracy improvement related to modeling the sub-threshold slope and DIBL mismatches in addition to only modeling threshold voltage and drain current mismatches, we have had access of 1000 n-FinFets and other 1000 p-FinFets models provided by [5].

The device design follows the ITRS guideline for HP multi-gate technology at 11nm technology node. Figure 5 shows a schematic picture of the FinFET structure, demonstrating the intrinsic 3D nature of the device. The devices feature a high-k dielectric stack with 0.585nm EOT and metal gates. Dual metal, gate-last process is assumed, in order to eliminate metal gate granularity and the associated work function variability. The device design has been implemented directly in the Glasgow atomistic simulator Garand [6].

The basic geometrical and electrical parameters of nFinFET are summarized in Table I in comparison with those specified in the ITRS for this technology.

In this work, the sources of variability considered are random discrete dopants (RDD), gate edge roughness (GER) and fin edge roughness (FER). The 3σ of the line edge roughness for both GER and FER are 2nm, and the correlation lengths are 30nm. An ensemble of 1000 microscopically different devices

TABLE I. STRUCTURAL AND ELECTRICAL PARAMETERS FOR THE NFINFET DEVICE.

	ITRS	TCAD
LG [nm]	9.7	10
EOT [nm]	0.57	0.585
Hfin [nm]	-	12.5
Wfin [nm]	4.8	5
IDSAT [A/m]	2.0	1.9
IOFF [nA/μm]	100	71
SS [mV/dec]	-	71
DIBL [mV/V]	-	53

is simulated and Figure 1 presents the ID-VG characteristics of the 10nm gate length nMOS FinFET device under the influence of combined statistical variability sources of RDD, GER and FER. Due to the FER induced quantum confinement variation, FinFET devices suffer from relatively large sub-threshold slope variation, as demonstrated in Figure 1. The combined effects of FER and GER also introduce large variation at device DIBL performance.

Compact models are the interface between technology and design. A two-stage statistical compact model parameter extraction strategy is implemented in [5]. During the first stage, a local optimization is employed to extract the complete nominal set of BSIM-MG parameters. During the second stage, key BSIM-MG parameters have been chosen to represent the effect of statistical variability sources, and their values are re-extracted based on the statistical simulation results of device I-V characteristics.

D. Benchmarking

We have calibrated our models to reflect the same device mismatch as the reference models using either two injectors — threshold voltage and drain-source current— or three injectors —including the sub-threshold slope or the DIBL— or four injectors —including both sub-threshold and DIBL.

The models including mismatch information and the nominal model modified by the different sets of injectors have been used to build an SRAM cell that has gone through hSpice simulations to report stability and performance metrics. The results obtained by each of the sets of injectors are compared to the ones obtained by the original transistor models.

III. RESULTS

A. I-V curves comparison

How accurately the new injectors reflect transistor characteristics is shown in Figure 6, transistors modeled using four injectors match the sub-threshold slope and DIBL of the model reference, while using two injectors only matches threshold voltage and Ion current, throwing constant values for the other parameters.

B. SRAM Stability Analysis

With each set of injectors as well as with the statistical model, 1000 6T-SRAM cells with one fin per transistor have been simulated, reporting read and write static noise margins [7], write trip point [8], read current and leakage current.

The percentage difference of the results obtained with each set of injectors compared to the results using the statistical

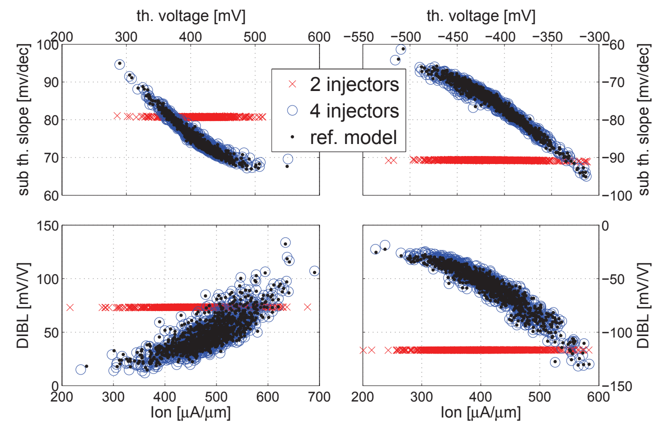

Fig. 6. Sub-threshold slope vs threshold voltage (top) and DIBL vs Ion current (bottom) for n-transistors (left) and p-transistors (right).

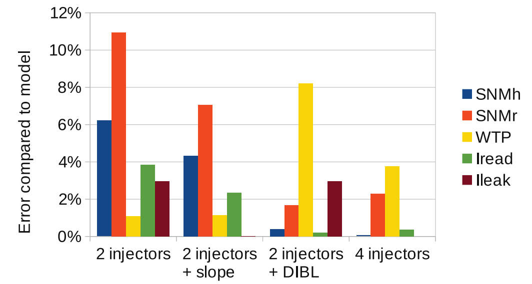

Fig. 7. Percent error compared to model using either 2 to 4 injectors when simulating the average of the key figures of an SRAM cell.

model for the mean values of the metrics are shown in Figure 7. The same values but for the standard deviations of those same metrics are shown in Figure 8

The results show that when using only two injectors the error on the averages of the metrics is high but still stays below 10%, however for the standard deviations of the metrics the error becomes unacceptable, at least 10% in all the metrics and more than 30% for the main stability metrics. Adding either a sub-threshold slope or a DIBL injector improves the accuracy in all the metrics. The slope injector presents better results for leakage and read currents while the DIBL injector improve the accuracy on SNM and WTP. The best results

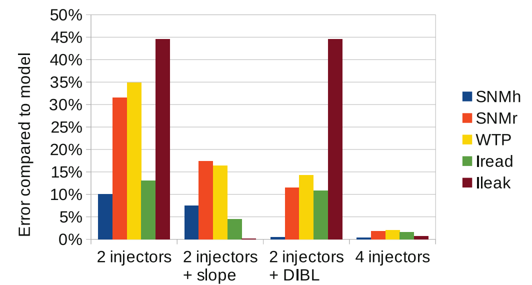

Fig. 8. Percent error compared to model using either 2 to 4 injectors when simulating the standard deviation of the key figures of an SRAM cell.

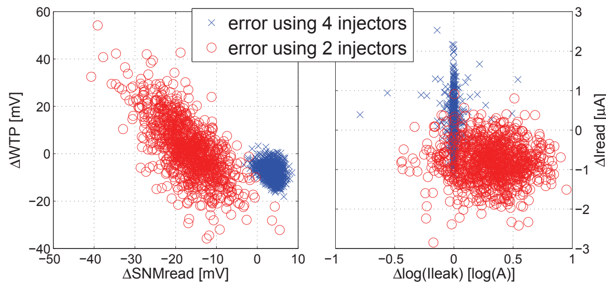

Fig. 9. Errors with 2 and 4 injectors with respect to model in the write trip point vs read static noise margin (left) and in the logarithm of leakage vs read current (right).

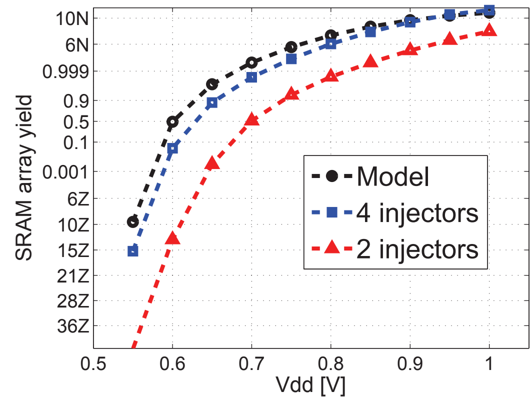

Fig. 10. Yield as the supply voltage is lowered, comparing 2 and 4 injectors to the statistical model. ($iN = 1{-}10^{-i}$ and $iZ = 10^{-i}$)

are obtained when using both DIBL and sub-threshold slope injectors, reducing the errors as low as to 2% in the worst case for standard deviations.

Figure 9 shows a one to one comparison on the performance metrics obtained with 2 or 4 injectors. On the right side, the difference between the logarithm of the leakage current using injectors and the model results are plotted in the x-axis, while the same is done for the read current in the y-axis. Using four injectors —black points— results on both a smaller systematic error and a smaller spread of the errors compared to using two injectors —red points.

The same procedure with similar conclusions are obtained for stability metrics shown on the left side of Figure 9: the read static noise margin presents both a smaller systematic error and smaller spreads, the write trip point systematic error is lower with only two injectors —which can also be seen in Figure 7— but four injectors throw a much lower spread, in the end the absolute value of the errors is lower with four injectors.

C. SRAM Yield

When we know the two main stability metrics, the SRAM yield can be inferred for a particular array size. The array will fail if one or more than one cell fails at either read static noise margin or write trip point. From the failure probability of an SRAM array, the yield is calculated, the usual targeted yield for a memory being 95%, that is no more than 5% of the memories are allowed to present failure in a cell.

Since the yield usually gets worse as the supply voltage is reduced, we can define $V_{dd,min}$ as the minimum supply voltage at which the SRAM presents the expected 95% yield.

We have computed the yield of a 32k-bit memory array, as the supply voltage was reduced, we compared the results using either two or four injectors to what is obtained using the statistical compact model. Those yield curves are shown in Figure 10, where it can be seen that four injectors approach presents a better approximation to the reference curve for the full range of supply voltages considered.

IV. Conclusion

In this work we have proposed two new injectors that model the variability at circuit level. Using dependent voltage sources, we can now recreate DIBL and sub-threshold slope mismatch. This allows a better modeling of the I-V curves of mismatched transistors in the sub-threshold region, for gate voltage below the threshold voltage and also for low drain to source voltages.

The better accuracy achieved on the I-V curves translates on a better accuracy when simulating the main stability and performance metrics of a 6T-SRAM cell, for the standard deviations of those metrics, the relative error can be reduced from 30% to 2% when using four injectors approach, resulting in a much improved yield and $V_{dd,min}$ estimation results.

Acknowledgements

This work was partially funded by the CICYT project TOLERA TEC2012-31292 of the Spanish Ministry of Economy and Competitiveness.

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