TCAD Modeling and Simulation of Non-Resonant Plasmonic THz Detector Based on Asymmetric Silicon MOSFETs

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***Abstract*— We report the experiments of plasmonic terahertz (THz) wave detector based on silicon field-effect transistors (FETs) in the nonresonant sub-THz (0.2 THz) regime. The detector responsivity (R_V) as a function of gate voltage has been successfully controlled by the radiation power in agreement with the plasma wave detection theory. To investigate the effects of the overdamped charge asymmetry on R_V, FET structure with the asymmetric source and drain area under the gate has been proposed. The enhanced R_V according to the increase of asymmetry ratio between source and drain region has been confirmed experimentally.**

Keywords—plasmonic terahertz wave; nonresonant regime; silicon FET detector; responsivity; asymmetry ratio

I. INTRODUCTION

Since terahertz (THz) wave detection mechanism by using oscillations of channel plasma waves based on a field-effect transistor (FET) structure was proposed by Dyakonov and Shur [1, 2], FETs with 2-dimensional electron gas (2DEG) in the channel have been intensively investigated as the promising plasmonic detectors of THz radiations ranging from 0.1 THz to 10 THz for compact and reliable solid-state THz detectors. In FET-based plasma wave detection theory [2], the resonance quality factor is $\omega\tau$ where ω is the angular frequency of the incoming radiation and τ is the plasmon decay time due to scattering in the FET channel, which is related with the carrier mobility $\mu = q\tau/m$ where m is the effective mass of electron, q is the electron elementary charge.

High frequency regime occurs when $\omega\tau >> 1$, which means that channel scattering frequency ($1/\tau$) is much smaller than the incoming THz radiation frequency, and then the channel plasma waves can be developed and the FET can act as a resonant [3, 4] detector in the strong inversion condition if the channel length is shorter than the propagation distance of the plasma wave. On the other hand, low frequency regime occurs when $\omega\tau << 1$, which is the typical situation in silicon (Si) FETs with relatively high scattering frequency ($1/\tau$) and low channel mobility, the FET operates in a nonresonant regime [5-9], but the rectification mechanism is still available in the subthreshold condition and enables broadband THz detection even though the plasma oscillation is overdamped and it cannot reach the drain side in the relatively long channel. FET-based detectors have been demonstrated by using high electron mobility transistors (HEMTs) based on compound materials [3-5] and Si metal-oxide-semiconductor FETs (MOSFETs) [6-8] for resonant mode at low temperature [3] and sub-THz nonresonant mode at room temperature [5-8], respectively.

Both for resonant and nonresonant operation regimes, the photoresponse ΔU appears in the form of dc voltage (V) between source and drain which is proportional to the radiation power P (W). Therefore, responsivity R_V, which can be defined by the ratio $\Delta U / P$ (V/W), is the important performance metric of the plasmonic THz detectors and researches for the enhanced responsivity have a lot of attention recently. In order to induce such a voltage of photoresponse from a given radiation power, some asymmetry between the source and drain is needed and there are typical three methods of asymmetry regime [9], such as the difference in the source and drain boundary conditions by using some external capacitances [8], the asymmetry in feeding the incoming radiation with a special antenna [10], and the asymmetry due to a dc current between source and drain [1, 3]. Related works also have been reported with a double-grating gate FET structure in asymmetric unit cell for strong coupling antenna [11], and asymmetric effects of device parasitics in the circuit aspects of FET rectifiers by integrating patch antenna and a high-gain voltage amplifier [8, 9]. The research of the asymmetry in the internal source and drain capacitances, however, has not been reported yet.

In this work, we report the analytical approach of the enhanced responsivity in silicon (Si) metal-oxide-semiconductor (MOS) FET-based non-resonant plasmonic THz detector with asymmetric source and drain boundary considering the device structural parameters by using TCAD device simulation.

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II. Fabrication and Simulation of Si FET Structure

The devices were fabricated on the 1×10^{15} cm^{-3} p-doped <100> Si wafer. By using the active layer as the first lithography step, the field oxide was removed at the source and drain region by dry etching in CHF_3/CF_4 reactive-ion plasma. At this first lithography step, source/drain region can be formed symmetrically or asymmetrically by varying the width of each source and drain, and the mask gate length (L_g) can be defined with the distance between source and drain region at the same time. After the formation of *n*-type source and drain region by $POCl_3$ diffusion process with the peak concentration of 3×10^{19} cm^{-3} and the junction depth of 700 nm, the 200-nm-thick inter-layer dielectric (ILD) oxide was deposited using plasma-enhanced chemical vapor deposition (PECVD). Subsequently, the gate open layer defines the gate-to-channel coupling region and 50-nm-thick thermal oxide was grown at 900 °C for the gate dielectric. After opening the contact holes at the source and drain regions, aluminum as metal layer was deposited by dc sputter and finally sintered at 450 °C. The metallurgical channel length can be estimated with about 1 μm considering the diffused junction depth from L_g= 2 μm in the non-self-aligned structure. The threshold voltage (V_{th}) extracted from the transfer characteristics at low drain bias was within the range of V_{th}= 0.48 V for all devices. Figure 1(a) presents the micrograph image (top view) of the second gate hole etching step the fabricated Si FET with asymmetric source and drain structure. It is clearly shown that there are 4 mask layers: the first active layer for doping region of source and drain, the second gate open layer for gate-to-channel coupling region overlapped with source and drain, the third contact layer for via hole contact between metal and doped regions, the fourth metal

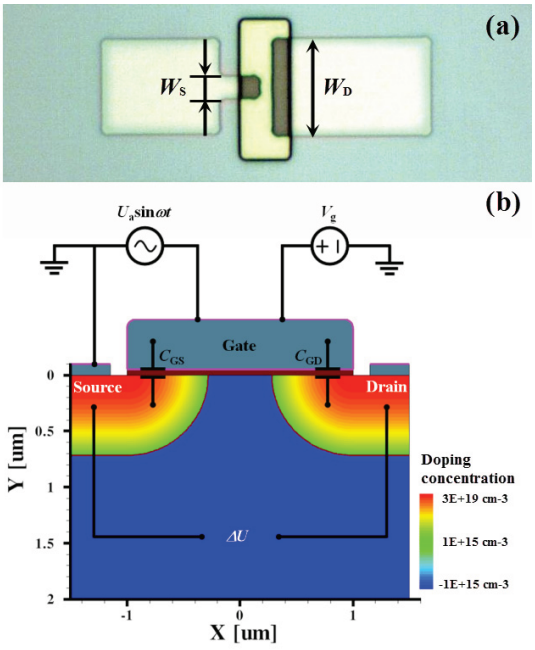

FIG. 1. (a) Micrograph (top view) of the fabricated Si FET with asymmetric source and drain. Drain width W_D and source width W_S with corresponding asymmetry ratio η_a= W_D/W_S is 10 and 1. (b) Schematic of simulation structure based on Si MOSFET. The structure was designed on metal (Al) gate as gate length (L_g) of 2 μm and junction depth (X_j) of 700 nm.

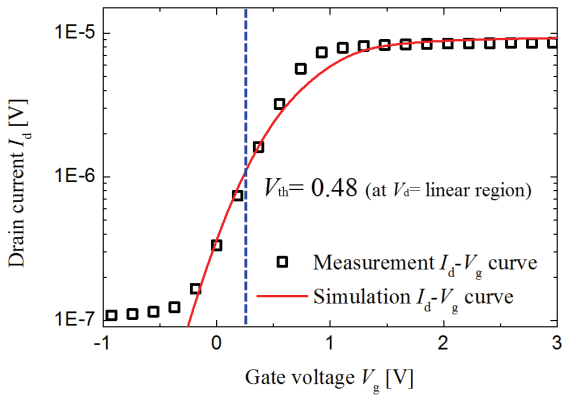

FIG. 2. DC transfer I_d-V_g curves of the fabricated device and simulation results. The threshold voltage V_{th} extracted from DC curves at V_d in linear regime.

layer for metallization of gate, source and drain electrodes, respectively. By using this layer sequence, the asymmetric source and drain doping region, which should be overlapped with gate electrodes, can be easily designed at the first layer step in non-self-aligned structure. Asymmetric structure condition is determined by split of the source width W_S with the fixed drain width W_D. The corresponding asymmetry ratio η_a (= W_D/W_S.) would be 10, and 1. Figure 1(b) shows the device simulation structure based on the fabricated Si MOSFET for the extraction of the DC characteristics and the channel 2DEG propagation distance (l) by THz radiation as modeled with ac voltage source signal ($U_a \sin\omega t$). Si MOSFET structure was designed as gate length (L_g) of 2 μm and channel concentration (N_{ch}) of $1x10^{18}$ cm^{-3}. Device simulation is performed by using Synopsys™ *Sentaurus Device* TCAD simulation with the application of asymmetric boundary condition between gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}). As shown in Fig. 2, the well-matched transfer I_d-V_g characteristics between device simulation and measurement indicate the same subthreshold swing (SSW) and the threshold voltage (V_{th}) have been extracted. While the simulation results show highly suppressed off-current, the fabricated device has subthreshold current owing to junction leakage of the order of 10^{-7}A. Measured DC *I-V* curve, however, has been successfully reproduced by device simulation in the subthreshold region where the 0.2 THz

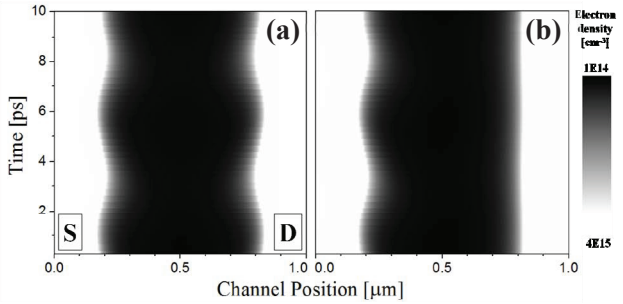

FIG. 3. Contour plot of the channel electron density modulation along with the channel position at each time scale. The channel 2DEG density is modulated near source side due to incoming THz radiation with f= 0.2 THz. (a) symmetry, (b) asymmetry condition of between source and drain.

response occurs with floating drain bias condition for the non-resonant THz wave detection output (ΔU).

III. Results and Discussion

Figure 3 shows that the modulations of the channel 2DEG density at 0.2 THz have been successfully obtained through the transient simulation based on the coupled Drude and continuity equation, which are readily implemented in the TCAD framework. These contour plots of the channel 2DEG density modulation along with the channel position at each time scale depend on the symmetric or asymmetric condition between C_{GS} and C_{GD} as shown in Fig. 3(a) and (b), which indicate the symmetry (C_{GS}=C_{GD}) and asymmetry ($C_{GD} > C_{GS}$), respectively, in source and drain boundary condition given by C_{GS} and C_{GD}. In terms of the asymmetric condition, by adding relatively large external capacitance between gate and drain, the AC signal has been applied only at the source side (x= 0) as $V(0, t)$= 0.05sin(ωt) + V_g (=V_t; 0.42 V) and gate-to-drain voltage can be kept with DC gate voltage as $V(L_g, t)$= V_g= 0.42 V at x= L_g. From these electron density contour plots by TCAD simulation, the plasma-wave propagation distance (l), which is the most important parameter in plasmonic THz detectors, has been extracted as shown in Fig. 3(b). These values of l can be varied by scattering, as plotted in Fig. 4 which illustrates the electron mobility degradation according to the decrease of t_{ox} owing to the surface roughness scattering (SRS) by the enhanced normal electric field. Therefore, it can be expected that the value of l decreases by more degraded electron mobility in thinner gate oxide. From these contour plots by TCAD simulation, the most important parameter l in plasmonic THz detectors has been extracted as 320 nm from the source edge with effective channel length (L_{eff}) of 1μm. At this point, l for symmetry regime can be estimated as 640 nm (2x320 nm) because of the symmetrically same l from the drain side, as shown in Fig. 3(a). By applying the analytical equations from ref. [2], the ideality factors (η) for obtaining l of each symmetry and asymmetry are

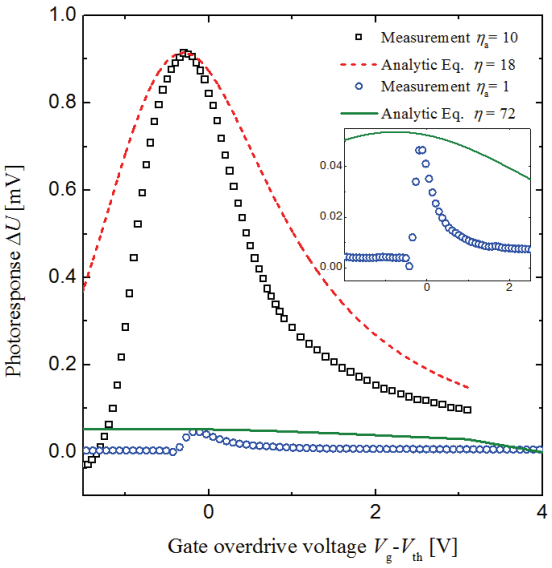

FIG. 4. Measured and analytically calculated photoresponse vs. gate overdrive according to the asymmetry ratio (η_a). Inset shows the symmetry case results in detail.

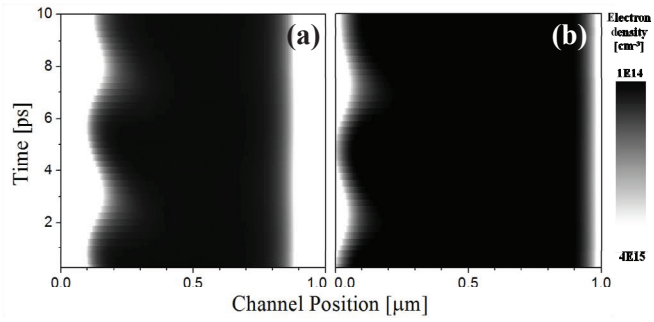

FIG. 5. Contour plots of (a) t_{ox}= 10 nm, and (b) t_{ox}= 1 nm. The propagation length l can be estimated as 300 nm and 150 nm from source side, respectively.

72 and 18, respectively. Based on these extracted and calculated values, as shown in Fig. 4, the key features of the measured photoresponse have been well reproduced with analytical equation for ΔU based on TCAD simulation. In comparison with the symmetrical source and drain structure (asymmetry ratio η_a= W_D/W_S= 1, where W_D and W_S are gate-overlapped drain and source width, respectively) as reference, the photoresponse of the asymmetry structure (asymmetry ratio η_a= W_D/W_S= 10) has been enhanced about 45 times. This difference of photoresponse between symmetry and asymmetry structure indicates that the high photoresponses can be obtained by varying l in an asymmetric structure. As simplified theory of the plasmonic THz detector, the lesser l, the higher photoresponse can be obtained [12]. Figure 5 indicates that l can be changed by the gate oxide thickness (t_{ox}), which is another key structural parameter for the 2DEG density modulation. From our TCAD simulation results, l decreases by reducing t_{ox} due to decrease of the normal field-dependent channel mobility (l= 300 nm with η = 16 for t_{ox}= 10 nm and l= 150 nm with η= 4 for t_{ox}= 1 nm). When t_{ox} decreases from t_{ox}= 50 nm to t_{ox} = 1 nm while L_{eff} is fixed, the enhanced photoresponse can be expected according to the decrease of SSW (Fig. 6).

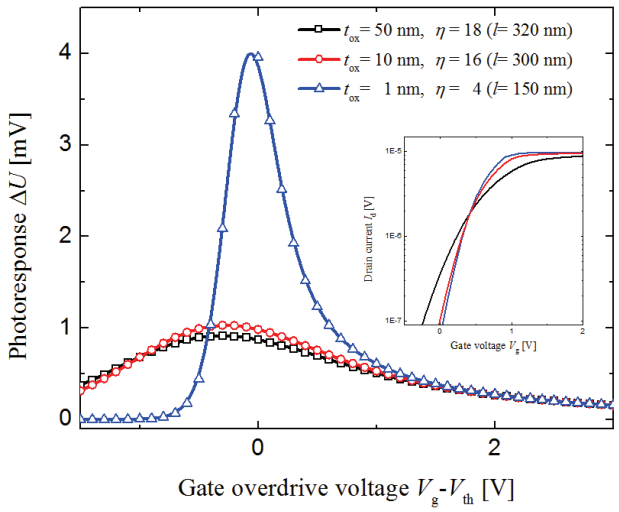

FIG. 6. Calculation results of the photoresponse vs. gate overdrive according to t_{ox} reduction. Inset shows the I_d-V_g curve of the simulated devices. Each curve has been calculated with ideality factor determined by contour plot according to t_{ox} reduction.

IV. Conclusion

We have verified that the plasmonic THz detector based on Si FETs with asymmetric source and drain structures can enhance the responsivity at room temperature by using TCAD simulation. These results can provide the physical simulation platform and the possibility of the plasmonic THz detector performance enhancement focusing on the propagation length by asymmetric design of source and drain structure under the gate in field-effect devices without additional considerations of external antenna and amplifier integration.

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