# 22nm Technology Yield Optimization Using Multivariate 3D Virtual Fabrication

B. Cipriany<sup>\*</sup>, B. Jagannathan, G. Costrini, A. Noemaun,
K. Onishi, S. Narasimha, B. Zhang, C. Sheraw, J. Meiring,
M. Kumar, K. Nummy, N. Zhan, H. Nanjundappa,
J. Norum, S. Furkay, R. Malik, P. Agnello *IBM Semiconductor Research & Development Center Hopewell Junction, NY, US*<sup>\*</sup>brcipria@us.ibm.com

Abstract — We present a technology development methodology that relies on 3D virtual fabrication to rapidly improve yield by increasing tolerance to multilevel process variation. This methodology has been successfully implemented in the development and yield ramp of high-performance 22nm SOI CMOS technology. Based on virtual metrology, dedicated testsite structures were designed and implemented, with electrical results corroborating virtual findings, validating the methodology. This 3D virtual fabrication technique was used to implement a delicate process change, and the same testsite structures validated the improved process window yield.

# *Keywords—CMOS; virtual fabrication; 22nm; testsite; modeling; n-p transition, yield optimization, virtual metrology;*

## I. INTRODUCTION

In advanced CMOS technology nodes, physical yield is often dominated by systematic defects arising from process variation [1-3]. Controlling the interaction of process variations is challenging and often requires a heuristic balance of the multiple failure mechanisms that bound the process Applying mathematical "best-case/worst-case" window. analyses of such complex interrelated variations is impractical. Reactor-scale models exist for studying individual processes or materials, but are not scalable to integrated process flows. Device simulators can incorporate additional process integration information; however, their layout scope and computational requirements are commonly limited to single transistor studies. Virtual fabrication, an entirely physical form of process modeling, uses behavioral abstractions of individual processes to accurately model and predict the structural details of an entire integrated flow. This abstraction enables fast modeling performance over large, multi-device areas, for parallel analysis of design-technology interaction. Since the majority of systematic defect mechanisms are purely physical in nature, virtual fabrication is adept at rapidly exploring the statistical relationships of process variation, and improving yield in the presence of multiple interacting effects.

This 22nm gate-first High-K/Metal-Gate CMOS

D. Fried<sup>†</sup>, K. Greiner, D. Faken, S. Breit *Coventor, Inc. Cambridge, MA, US* <sup>†</sup>david.fried@coventor.com

technology relies on engineering the gate-cap nitride evolution, for the RIE-based removal of this cap prior to salicide module [4]. The conditions for this process require that the cap nitride remain thick enough to protect the gate silicon during the dual-epitaxial source/drain modules, but must also be thin enough to ensure complete top-removal for uniform silicide formation. The most challenging design construct for this particular process window is the gate transition over the interface of nMOS and pMOS regions (n-p transition), where the compounded interaction of several generated-level mask edges creates topography in the nitride cap during spacer and trench etches. To optimize this multilevel interaction, we employ Coventor<sup>TM</sup> SEMulator3D<sup>TM</sup> [5] virtual fabrication platform and its virtual metrology in a parallel analysis to explore both systematic and stochastic process variation.

# II. NOMINAL MODEL CALIBRATION

The nominal case model was assembled by virtual fabrication using a design layout and an initial set of unit process descriptions from an integrated flow. This model demonstrated physically predictive capability that was further refined through both process and structural calibration to physical results at the unit process level. Process calibration was conducted primarily using inline metrology data. Structural calibration involved iterative matching of geometric parameters to corresponding physical measurements, beginning with thickness and shape parameters, and then refining curvature at critical structural features. In this work, the 3D model was matched to inline measurement and metrology data, as well as 2D SEM/TEM cross-section images of the nominal transistor in two orthogonal directions (Fig 1, 2, 3).



Fig. 1: Isometric view of 3D model showing mid-process n-p transition region over STI



Fig. 2: Cross-gate section calibration matching TEM sample

Once calibrated, the virtual fabrication model responds predictively to alternate designs or process variations, and becomes the foundation for exploring design-technology interaction. These interactions are increasingly interrelated and 3D in nature due to state-of-the-art performance-enabling elements. Additionally, different device structures each impose structural limitations, making the yield optimization for an integrated process flow multi-dimensional. In this 22nm gatefirst technology, gate cap thickness can limit yield via incomplete removal prior to silicide along the gate axis (too thick) or via incomplete protection of the nMOS or pMOS gate during epitaxy (too thin), incomplete protection of the differential source/drain stressors (too thin) or potential exposure of the HK/MG stack (too thin). Each of these criteria can also have different limits depending on design construct, differing among logic, memories, analog devices, and process fill-shapes. This level of structural complexity necessitates 3D models to capture the multi-dimensional process boundaries in a design-aware fashion.

#### III. PROCESS VARIATION EVALUATION

While variations in deposition thickness and etch rates contribute slightly to the total variation in the nitride cap at the n-p interface, the dominant sources of variation are the spatial exposure and overlay errors from multiple lithography levels whose edges define that interface. Originally, the intent of processes defining the n-p transition was to maintain a relatively flat nitride cap under nominal conditions (Fig 3) for process simplicity.



Fig. 3: Through-gate section calibration matching SEM sample

Batch execution of the SEMulator3D model was conducted, with forced perturbations in the edge location on each mask level to simulate overlay errors. The individual variations were combined in a root sum square (RSS) method to evaluate the total variation for each set of mask edge placements. Virtual 3D metrology, including a virtual AFM measurement, was used to extract the nitride profile at the n-p interface of the 3D model (Fig 4). The estimated process window boundary conditions predict the onset of defectivity near  $2\sigma$  of total variation (Fig 5).



Fig. 4: Virtual AFM line sample for two cases of  $3\sigma$  root sum square total mask edge placement variation.



Fig. 5: Virtual AFM samples a representative statistical set of edge placement cases, grouped by total process variation. Upper bound at  $2\sigma$  defines process window for final cap RIE.

This virtual profile line-scan data was integrated to create a figure of merit (FOM) for the remaining nitride incoming to the cap removal RIE (Fig 6).



Fig. 6: Integration of virtual fabrication nitride profiles allows a FOM extraction

From this massive multivariate space of mask edge locations, a subset of cases were selected to represent the total possible variation space, and were implemented in testsite characterization structures. The key test structure used for characterization was a long, minimum-width serpentine gate, with repeating n-p interfaces (Fig 7). Incomplete removal of nitride at these n-p interfaces would result in blocked silicide formation and increased serpentine resistance.



Fig. 7: Serpentine gate test structure stressing the continuity across n-p boundaries

Cap nitride removal was varied in a RIE time experiment to illustrate the electrical response from these test structures, which show excellent correlation to the virtual measurement FOM (Fig 8).



Fig. 8: Test structure current is influenced by mask placement variations, plotted vs. nitride FOM. Experiment perturbs silicide uniformity.

While the non-optimized, nominal case shows excellent yield, it only offers process window coverage to  $2\sigma$  of RSS mask edge variation (Fig 9), insufficient for high yield manufacturing.



Fig. 9: Electrical yield of test structures plotted vs. total variation of multiple mask misalignments

#### IV. VIRTUAL DESIGN/PROCESS OPTIMIZATION

Based on the process window evaluation discussed previously, individual components of variation were identified for their influence on multiple yield-limiting mechanisms. This analysis was performed by inspecting 3D models of numerous design constructs (NFETs, PFETs, SRAMs, eDRAM, etc.) to identify boundary constraints in physical variation. In this fashion, the predictive capability of the virtual fabrication was essential to visualize the 3D processcompounded effects at the corners and overlapping regions unique to each construct. The boundary constraints identified and the probable conditions for yield degrade across the device suite established a priority scheme for optimizing the np interface changes. A large set of alternative n-p interface designs was modeled and suggested a new set of nominal mask edge positions. Each set of positions was then analyzed using the method of mask edge perturbation to virtually explore the process window in the presence of yield-limiting constraints, ultimately identifying an optimized set of nominal mask edge positions. Interestingly, this new set of mask edge locations resulted in a nitride profile that is not flat under nominal lithography and process conditions, a non-intuitive process integration solution (Fig 10).



Fig. 10: Through-gate sections illustrating the optimized nitride profile

However, the virtual fabrication model showed that this new process change, implemented across multiple levels, would improve process window tolerance to nearly  $4\sigma$  (Fig 11,12). These optimized edge locations were then evaluated in hardware.



Fig. 11: Virtual AFM line samples for the optimized nitride profile design during intermediate RIE steps. Lower bound at  $4\sigma$  defines onset of process defects.



Fig. 12: Virtual AFM line samples for the optimized nitride profile design, grouped by total process variation. Upper bound at 4σ defines process window for final cap RIE.

### V. VARIATION TOLERANCE IMPROVEMENT

Based on confidence in the virtual fabrication results from the optimized process/design conditions, a complex multimask, multi-module change was executed. The same set of serpentine test structures was included on the updated testsite, and their designs were subjected to the same changes as the remainder of the testsite. Electrical data from the serpentine test structures shows improved yield for the optimized nominal case, despite the non-flat profile. More importantly, the yield on the perturbed layouts of the optimized profile improved dramatically, offering a robust  $5\sigma$  RSS process window to mask edge variation (Fig 13).



#### VI. CONCLUSIONS AND FUTURE WORK

This process yield optimization demonstrates the capability of virtual fabrication to predict complex interrelated effects, study statistical variation, and direct process optimizations for yield improvement. This work relied on the speed, parallelism, and predictive accuracy of virtual fabrication to statistically evaluate a complex set of changes and support rapid technology development. These powerful attributes will enable additional process guidance in future advanced CMOS development.

#### ACKNOWLEDGMENT

We gratefully acknowledge the support of the entire IBM 22nm SOI technology development team, the SEMulator3D development team, and the staff of the IBM 300mm manufacturing facility in Hopewell Junction, NY. This work was guided by management support including Matt Paggi, Neil Peruffo, Gary Patton, and Mike Jamiolkowski.

#### REFERENCES

- Gupta and Papadopoulou, "Yield Analysis and Optimization", Chapter 7.3 in C.J. Alpert, D.P. Mehta, S.S. Sapatnekar editors, "The Handbook of Algorithms for VLSI Physical Design Automation", Taylor & Francis CRC Press, November 2008.
- [2] http://www.itrs.net/Links/2007ITRS/2007\_Chapters/2007\_Yield.pdf
- [3] Stapper, et al., "Integrated Circuit Yield Management and Yield Analysis: Development and Implementation", IEEE TSM Vol 8, No 2, May 1995, pp. 150-159.
- [4] Narasimha, et al. "22nm High-Performance SOI Technology Featuring Dual-Embedded Stressors, Epi-Plate High-K Deep-Trench Embedded DRAM and Self-Aligned Via 15LM BEOL", IEEE IEDM, Dec. 2012 3.3, pp. 52-55.
- [5] http://www.coventor.com/products/semulator3d/