# Strain effects on transport properties of Si nanowire devices

Viet-Hung Nguyen[1], François Triozon[2], and Yann-Michel Niquet[1]
[1]L_Sim, SP2M, UMR-E CEA/UJF-Grenoble 1, INAC, 38054 Grenoble, France
[2]CEA, LETI, MINATEC Campus, 38054 Grenoble, France
Email: viethung.nguyen@cea.fr

***Abstract*—We study the effects of strains on the performances of $\langle 001 \rangle$ and $\langle 110 \rangle$ oriented gate-all-around silicon nanowire (Si NW) transistors within a Non-Equilibrium Green's Functions framework. In agreement with previous works, we show that uniaxial strains can significantly improve the carrier mobility in the channel. However, we find that besides the enhancement of the carrier mobility, the ballistic resistance must be simultaneously optimized to achieve good performances in short channel devices. The response of the ballistic resistance to strains is different in [001] and [110] strained devices. Our study shows that the ballistic resistance is improved more consistently with the mobility in [110] Si NWs, providing the best opportunities for strain engineering in ultimate short channel transistors.**

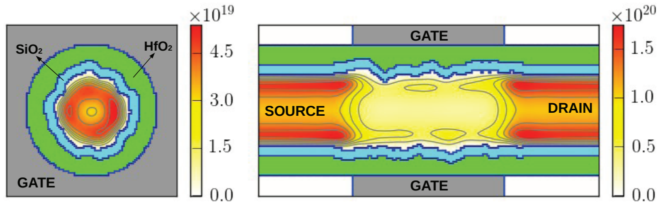


Fig. 1. The simulated devices are cylindrical gate-all-around Si NWFETs with diameter $d$ = 8 nm and gate length $L_g$ = 16 nm. The carrier density in a n-doped, unstrained [110] oriented device is plotted at $V_{gs}$ - $V_{th}$ = 0.5 V and $V_{ds}$ = 25 mV.

## I. Introduction

The development of advanced technologies has raised some challenges such as achieving good electrostatic control and minimal short channel effects [1]. In this context, gate-all-around silicon nanowire (Si NW) transistors appear as promising candidates [2], [3], [4]. However, as the NW diameter decreases, the transport properties of silicon are strongly affected by quantum confinement. The carrier mobility can hence be enhanced or suppressed depending on the limiting mechanism (impurities, phonons, surface roughness...) [5], [6]. Strain engineering techniques, which have been extensively used to improve the electrical properties of semiconductor devices in planar technologies, shall also be very efficient in Si NWs. Indeed, significant performance enhancements have been theoretically predicted [7], [8] and experimentally observed [9], [10].

Understanding the impact of strains in realistic short-channel devices is hence timely and necessary. The non-quilibrium Green's functions (NEGF) technique, which can treat quantum confinement and different scattering effects in a seamless way, is best suited to this objective. In this paper, we present NEGF simulations of uniaxially strained $n-$ and $p-$type Si nanowire field effect transistors (NWFETs) with phonon and surface roughness scatterings. Our model combines the self consistent treatments of scattering and electrostatics with the multibands **k.p** descriptions of electrons and holes in uniaxially strained Si NWs [3], [4]. We show that strains can significantly enhance the carrier mobilities in Si NWs. However, the ballistic resistance must be optimized along with the mobility to achieve the good performance of short channel devices. We give an overview of these results below. Details can be found in [11].

## II. Methodology and simulated device

The simulated devices schematized in Fig. 1 are cylindrical gate-all-around Si NWFETs with diameter $d$ = 8 nm, gate length $L_g$ = 16 nm, and [001] or [110] orientation. The gate stack is made up of a 1-nm thick $SiO_2$ and of a 2-nm thick $HfO_2$ shell. The transport properties of the Si NWs are computed in a NEGF framework [12] based on a two bands **k.p** model for the electrons and a three bands **k.p** model for the holes. The NEGF equations are solved self-consistently in a fully coupled mode space approach [13]. We use the local approximation for the carrier-phonon self-energy [14] and a standard exponential autocorrelation function model for surface roughness [15]. For carrier-phonon scatterings, we borrowed the deformation potentials from [16] for electrons and from [17] for holes. The surface roughness (SR) is characterized by rms radius fluctuations $\Delta$ = 0.25 nm and correlation length $L_c$ = 1.4 nm.

The carrier mobility and ballistic resistance of the nanowires are computed from gate length scaling analyses [11]. At low $V_{ds}$, the total resistance $R_{ch}$ of the channel is written as

$$R_{ch}(L) = R_0(n_{1d}) + \frac{L}{n_{1d}\mu e}. \quad (1)$$

The second term ($\propto L$) is the usual "diffusive" resistance limited by scattering (mobility $\mu$) and $n_{1d}$ is the average 1D-carrier density. The first term ($R_0$) is known as the "ballistic" resistance and is limited by the number of sub-bands available for carrier transport. We now consider fully gated, junctionless Si NWs (no doped access regions) with lengths $L$ ranging from 8 to 32 nm. We apply a small, constant longitudinal electric field $V_{ds} \propto L$ and sweep the gate voltage $V_{gs}$. We monitor the density $n_{1d}$ in the nanowires and their resistance $R(L,n_{1d})$

978-1-4673-5736-4/13/$31.00 ©2013 IEEE

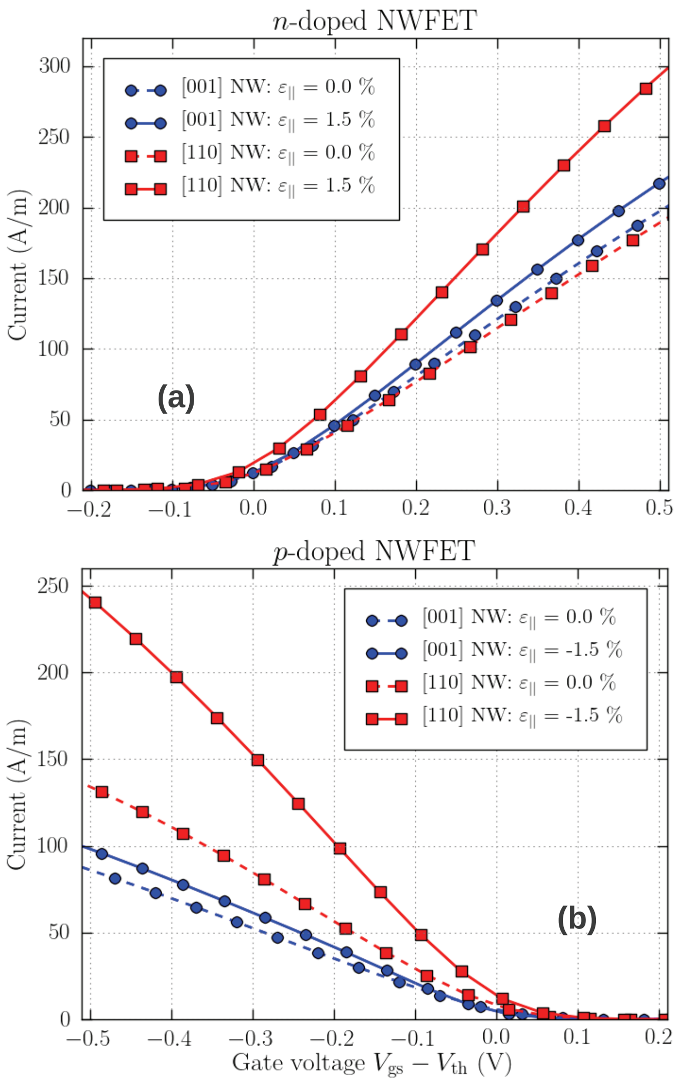


Fig. 2. Room-temperature $I(V_{\rm gs})$ characteristics of free standing and uniaxially strained $n$- and $p$-type Si NWFETs, at low source-drain bias $V_{\rm ds} = 25$ mV. The longitudinal strain is $\varepsilon_{\|} = 1.5\%$ for $n$-type NWFETs, and $\varepsilon_{\|} = -1.5\%$ for $p$-type NWFETs. The current is normalized with respect to the circumference $\pi d = 25.1$ nm of the nanowires.

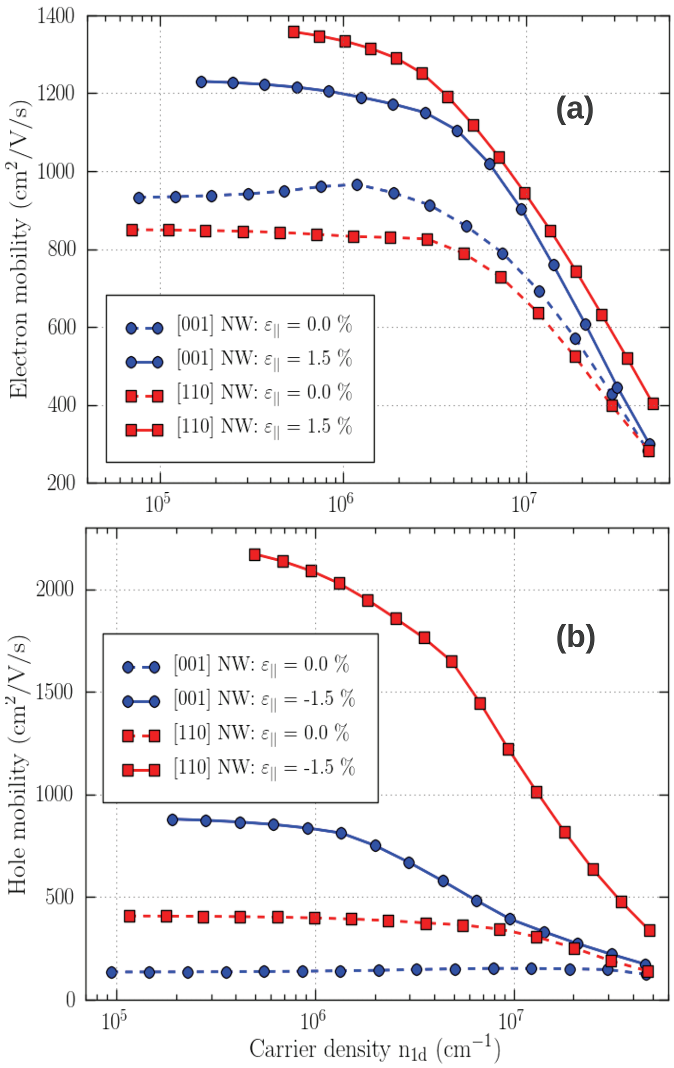


Fig. 3. Room-temperature, phonon+surface roughness limited electron and hole mobilities as a function of carrier density in free standing and uniaxially strained Si NWs with diameter $d = 8$ nm.

= $V_{ds}/I$. Finally, we can extract $\mu(n_{1d})$ and $R_0(n_{1d})$ from a linear regression with (1).

## III. Results and Discussions

The drain current in $n-$ and $p-$type Si NWFETs is plotted as a function of the gate overdrive $V_{gs}$-$V_{th}$ in Fig. 2, at low $V_{ds}$ = 25 mV. First, the performances of these Si NWFETs are very dependent on the nanowire orientation. In free standing Si NWs, while the transconductance is about the same in [001] and [110] $n-$NWFETs, it is $\sim$ 60 % larger in [110] than in [001] $p-$type devices and the current in the saturation regime is about 30 % - 40 % larger in [110] $p-$NWFETs. This is in good agreement with the orientational dependence reported in [6], [8], which is stronger for holes than for electrons. Second, whatever the orientation, the uniaxial tensile strains increase the performances of $n-$NWFETs, while the compressive strains tend to increase the performances of $p-$NWFETs. However, the responses of these Si NWFETs to strains are also very dependent on the nanowire orientation, i.e., the improvement is marginal in [001] oriented devices while it can reach almost 2$\times$ in [110] oriented NWFETs. This is consistent with the experimental results reported in [9], [10]. The same features have been observed on the $I - V_{ds}$ characteristics (see in [11]).

To understand the transport characteristics shown above, we investigate the carrier mobility and ballistic resistance of the nanowires within our NEGF framework. The mobility is plotted as a function of the carrier density in Fig. 3. At low density, where the current is mostly limited by carrier-phonon interactions, the data are consistent with that reported in [6], [8]. The electron mobility is weakly dependent on the nanowire orientation while the hole mobility is about 3$\times$ larger in [110] than in [001] Si NWs. The uniaxial strains enhance

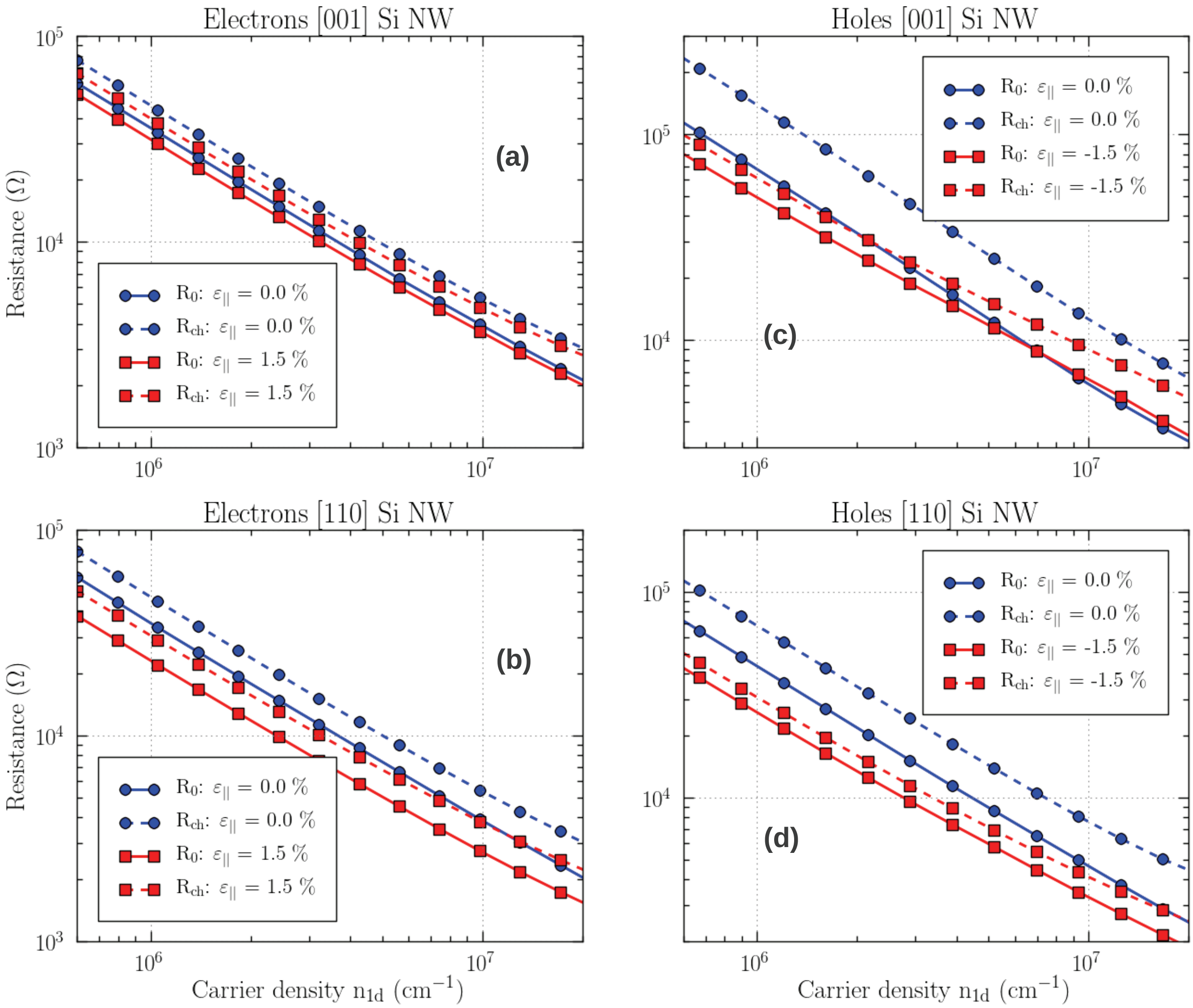


Fig. 4. Ballistic resistance $R_0$ as a function of carrier density in free standing and uniaxially strained Si NWs with diameter $d = 8$ nm. The total (ballistic+diffusive) resistance $R_{ch}$ of a 16 nm long channel is also plotted for comparison.

the carrier mobility whatever the orientation. This is explained in [6], [8], [11] by the fact that the strains empty the heavy $\Delta$ valleys off $\Gamma$ (resp. heavy hole bands) into the light $\Delta$ valleys at $\Gamma$ (resp. light hole bands) for electrons (resp. holes). This picture however changes at large carrier density, where the SR scattering comes into play. On the one hand, the difference between two orientations becomes thinner, especially in free standing nanowires. On the other hand, strains hardly improve the carrier mobility in [001] nanowires while they remain an efficient booster in [110] Si NWs. These trends are reminiscent of the shape of the band structure at high energy (see in [8], [11]).

The devices of Fig. 2 typically operate in the range of $2{\times}10^7$ carriers per cm. It is clear that the orientational and strain dependence of the current does not follow exactly the strends on the mobility shown in Fig. 3. In particular, the increase of current in strained [001] NWs is much lower than expected from the mobility data. The total resistance, as shown in eq. (1), depends not only on the mobility, but also the ballistic resistance. This, as discussed below, can explain the disagreement between the responses of the mobility and current to strains.

In Fig. 4, we plot the ballistic resistance $R_0$ as a function of the carrier density and the total resistance $R_{ch}$ of a 16 nm long channel. To understand the orientational and strain dependence of $R_0$, we can assume Maxwell-Boltzmann statistics and a single transport mass $m^*$ for all sub-bands, and obtain

$$\frac{1}{R_0} = -\frac{2e^2}{h}\int d\varepsilon \left(\frac{\partial f}{\partial \varepsilon}\right) t(\varepsilon) = \frac{n_{1d}e^2}{\sqrt{2\pi m^* kT}}. \qquad (2)$$

Although the assumptions above may not hold in general, this equation nicely explains the main properties of $R_0$. Indeed, in short channels, the ballistic resistance is an important contribution to $R_{ch}$, e.g., it is as large as 75 % of $R_{ch}$ in unstrained [110] $n-$NWFET and about 60 % of $R_{ch}$ in unstrained [110] $p-$NWFET. Fig. 4 clearly shows that the improvement of $R_0$ is significant in strained [110] nanowires but marginal in [001] ones. This, in spite of significant enhancement of carrier mobility, leads to a weak improvement of the total resistance (current) in [001] devices while the effects are stronger in [110] NWFETs.

The response of $R_0$ to strains can be explained as follow. We focus on $n-$NWFETs first. In [001] Si NWs, the $\Delta$ valleys split into light, fourfold degenerate $\Delta_1 \equiv \Delta_{x,y}$ valleys at $\Gamma$ ($m^* \approx 0.19$) and heavier, twofold degenerate $\Delta_2 \equiv \Delta_z$ off $\Gamma$ ($m^* \approx 0.92$) (see Fig. 6 of [11]). Likewise, in [110] Si NWs, the $\Delta$ valleys split into light, twofold degenerate $\Delta_1 \equiv \Delta_z$ valleys at $\Gamma$ ($m^* \approx 0.18$) and heavier, fourfold degenerate $\Delta_2 \equiv \Delta_{x,y}$ off $\Gamma$ ($m^* \approx 0.55$). $R_0$ is hence the ballistic resistance $R_{0,\Delta_1}$ of the $\Delta_1$ valleys in parallel with the the ballistic resistance $R_{0,\Delta_2}$ of the $\Delta_2$ valleys, i.e., $R_0^{-1} = R_{0,\Delta_1}^{-1}(n_1) + R_{0,\Delta_1}^{-1}(n_2)$ with the partial densities $n_1$ and $n_2$. Since $R_0 \propto m*^{1/2}$, the $\Delta_2$ valleys show a much larger ballistic resistance than the $\Delta_1$ valleys for a given density. The decrease of $R_0$ is, however, is much greater in [110] NWFETs because: (i) the population of $\Delta_2$ valleys with fourfold degeneracy is larger in unstrained [110] than in unstrained [001] devices with twofold $\Delta_2$ degeneracy and (ii) the mass of the $\Delta_1$ valleys of [110] NWs decreases from $m^*$ = 0.18 at $\varepsilon_{||} = 0$ down to $m^*$ = 0.13 at $\varepsilon_{||} = 1.5\%$ due to shear strains [8]. The [110] $n-$NWFETs therefore show a 35% decrease in ballistic resistance at $\varepsilon_{||} = 1.5\%$, while it is only about 12% in [001] devices.

In $p-$NWFETs, uniaxial compressive strains push significantly heavy holes down and bring light holes at the top of the valence band in [110] devices (see in [11]). This increases the population of light with respect to heavy holes and strongly reduces the ballistic resistance, e.g., by up to 38% at $\varepsilon_{||} = -1.5\%$. The situation is however more complex in [001] Si NWs. As shown in [8], [11], the holes are very heavy in unstrained nanowires. Even if strains improve the picture, many high-lying valence bands are still little dispersive, which limits the improvement of $R_0$ at large hole densities and hence limits the enhancement of the performances of strained [001] $p-$NWFETs.

## IV. Conclusion

We have simulated the transport characterisrtics of Si NWFETs with the effects of uniaxial strains. We find that the ballistic resistance is an important part of the total resistance of short channel devices and must be optimized along with the mobility to improve their performance. We have shown that uniaxial strains can significantly improve the carrier mobility and decrease the ballistic resistance of nanowires; however, the quantitative trends are different in [001] and [110] oriented devices. In particular, the ballistic resistance is not improved as much as the mobility in strained [001] Si NWs, so that the performances of short channel devices are little enhanced. On the contrary, the improvements of ballistic resistance and mobility are more consistent in [110] Si NWs, which provides much more opportunities for efficient strain engineering in these NW devices.

## Acknowledgment

This work was supported by the French National Research Agency Project Quasanova under Contract ANR-10-NANO-011-02. The calculations were run on the TGCC/Curie machine using allocations from GENCI and PRACE (under projects 2010PA0885 and 2012071219).

## References

[1] *Itrs Roadmap.* (2007) [Online]. Available: http://www.itrs.net/

[2] N. Singh, A. Agarwal , L. Bera , T. Liow , R. Yang , S. Rustagi , C. Tung , R. Kumar , G. Lo , N. Balasubramanian and D.-L. Kwong, "*High-performance fully depleted silicon nanowire (diameter $\leq$ 5 nm) gate-all-around CMOS devices*", IEEE Electron Device Lett. **27**, pp. 383-386 (2006).

[3] M. Casse, K. Tachi, S. Thiele and T. Ernst, "*Spectroscopic charge pumping in Si nanowire transistors with a high-κ/metal gate*", Appl. Phys. Lett. **96**, pp. 123506-1−123506-3 (2010).

[4] S. Barraud, R. Coquand, M. Casse, M. Koyama, J.-M. Hartmann, V. Maffini-Alvaro, C. Comboroure, C. Vizioz, F. Aussenac, O. Faynot and T. Poiroux, "*Performance of omega-shaped-gate silicon nanowire MOSFET with diameter down to 8 nm*", IEEE Electron Device Lett. **33**, pp. 1526-1528 (2012).

[5] N. Neophytou and H. Kosina, "*Atomistic simulations of low-field mobility in Si nanowires: Influence of confinement and orientation*", Phys. Rev. B **84**, pp. 085313-1−085313-15 (2011).

[6] Y.-M. Niquet, C. Delerue, D. Rideau and B. Videau, "*Fully atomistic simulations of phonon-limited mobility of electrons and holes in [001]-, [110]-, and [111]-oriented Si nanowires*", IEEE Trans. Electron Dev. **59**, pp. 1480-1487 (2012).

[7] M. O. Baykan, S. E. Thompson and T. Nishida, "*Strain effects on three-dimensional, two-dimensional, and one-dimensional silicon logic devices: Predicting the future of strained silicon*", J. Appl. Phys. **108**, pp. 093716-1−093716-24 (2010).

[8] Y.-M. Niquet, C. Delerue and C. Krzeminski, "*Effects of strain on the carrier mobility in silicon nanowires*", Nano Lett. **12**, pp. 3545-3550 (2012).

[9] P. Hashemi, L. Gomez and J. Hoyt, "*Gate-All-Around n-MOSFETs With Uniaxial Tensile Strain-Induced Performance Enhancement Scalable to Sub-10-nm Nanowire Diameter*", IEEE Electron Device Lett. **30**, pp. 401-403 (2009).

[10] R. Coquand, M. Casse, S. Barraud, D. Cooper, V. Maffini-Alvaro, M.-P. Samson, S. Monfray, F. Boeuf, G. Ghibaudo, O. Faynot, and T. Poiroux, "*Strain-Induced Performance Enhancement of Trigate and Omega-Gate Nanowire FETs Scaled Down to 10-nm Width*", IEEE Trans. Electron Devices **60**, pp. 727-732 (2013).

[11] V.-H. Nguyen, F. Triozon, F. D. R. Bonnet, Y.-M. Niquet, "*Performances of Strained Nanowire Devices: Ballistic Versus Scattering-Limited Currents*", IEEE Trans. Electron Devices **60**, pp. 1506-1513 (2013).

[12] M. P. Anantram, M. S. Lundstrom and D. E. Nikonov, "*Modeling of Nanoscale Devices*", Proc. IEEE **96**, pp. 1511-1550 (2008).

[13] J. Wang, E. Polizzi and M. Lundstrom, "*A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation*", J. Appl. Phys. **96**, pp. 2192-2203 (2004).

[14] S. Jin, Y. J. Park and H. S. Min, "*A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interactions*", J. Appl. Phys. **99**, 123719-1−123719-10 (2006).

[15] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy and O. L. Krivanek, "*Surface roughness at the Si(100)-SiO2 interface*", Phys. Rev. B **32**, pp. 8171-8186 (1985).

[16] C. Jacoboni and L. Reggiani, "*The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials*", Rev. Modern Phys. **55**, pp. 645-705 (1983).

[17] F. Szmulowicz, "*Calculation of optical- and acoustic-phonon-limited conductivity and Hall mobilities for p-type silicon and germanium*", Phys. Rev. B **28**, pp. 5943-5963 (1983).