Electrostatics and Ballistic Transport Studies in Junctionless Nanowire Transistors

T.-H. Yu, Ethan Hsu, C.-W. Liu, J.-P. Colinge, Y.-M. Sheu, Jeff Wu, and C.H. Diaz TCAD Division, Taiwan Semiconductor Manufacturing Company (TSMC) E-mail: thyub@tsmc.com

Abstract—In this work a drift-diffusion simulator is utilized to study the electrostatics of a cylindrical gate-all-around junctionless nanowire transistor. For carrier transport properties such as carrier scattering and velocity in channel, a full band Monte Carlo is adopted to simulate non-equilibrium and ballistic behaviors. Two major cases: different S/D extension schemes and channel doping effects are examined in this study. It is observed that S/D extension underlap can benefit short-channel control and carrier velocity. In addition, channel doping is found to play an import role to increase carrier injection velocity in the junctionless nanowire transistors.

Keywords—junctionless transistor; nanowire; ballistic transport; injection velocity

L

INTRODUCTION

The junctionless nanowire transistor (JLNT) has become widely recognized as one of the most promising candidates for future nanoscale CMOS technology due to its excellent subthreshold slope (SS), low drain-induced barrier lowering (DIBL) and low leakage current [1-4]. In addition, a recent study in junctionless MOSFETs has revealed higher mobility in accumulation channels than that in bulk due to an impurity scattering screening effect in heavily doped channels [5]. Several researchers have presented studies on JLNTs [2-4]. Refs [2-3] applied a non-equilibrium Green function (NEGF) approach to investigate the channel material impact on performance and the ballisticity of JLNTs. Ref [4] proposed an analytical current-voltage model to study the electrical characteristics of the JLNT. There is, however, no study linking the electrostatics and ballistic transport properties in JLNTs. This paper intends to provide a physical understanding of short-channel effects (SCEs) and carrier velocity properties for different source/drain (S/D) extension schemes and channel doping levels.

From an electrostatics standpoint, it is desirable to use S/D extension underlap to improve SCEs because it increases the effective gate length in the off-state. From a carrier transport point of view, an electric field peak found in the S/D in the source underlap region, helps accelerating electron injection into the channel. Moreover, the ballistic injection velocity, which is related to the channel doping, significantly increases when high channel doping concentrations are used. On the other hand, high channel doping concentration may increase impurity scattering and thus degrade the injection velocity.

II. SIMULATION METHODOLOGY

In general, carrier transport can be divided into three regimes: diffusive transport, ballistic transport, and quantum transport [6]. When the gate length is much greater than the carrier mean free path, the carriers transit within the diffusive transport regime where scattering dominates. Carriers can reach their equilibrium states through sufficient scattering events and thus DD (Drift-Diffusion) model can capture well this equilibrium carrier transport property. When the gate length is shorter than de Broglie wavelength, the carriers transit within the quantum transport regime, where the full quantum transport approach such as NEGF is suitable to simulate strong quantum confinement and significant sourceto-drain tunneling. In the range between these two regimes, the carriers transit from quasi-ballistic to ballistic transport regime. The semi-classical approach Monte Carlo simulator incorporated with full band structure is able to capture the non-equilibrium transport effects.

In this study, a simulation methodology is presented based on a 3D drift-diffusion (DD) simulator [7] including quantum confinement effects to accurately describe electrostatics-related characteristics of JLNTs such as SS and DIBL. An accumulation layer mobility model calibrated using previous work [5] is adopted in this work. Furthermore, a full-band Monte Carlo simulator [8] is utilized to investigate the ballistic and scattering transport properties in JLNTs amending DD's inability to capture nonequilibrium velocity overshoot effects in channels shorter than the carrier mean free path. Scattering mechanisms including ionized impurity, phonon, and surface roughness are considered for non-ballistic transport simulations.

In addition, the Bohr radius is used to determine the range of spatial dimension in which quantum confinement can be observed [9]. For example, if the nanowire diameter is smaller than the Bohr radius, the spatial quantum confinement becomes significant and band splitting becomes significant, accompanied by a bandgap energy and an effective mass increase [9,10]. Therefore, a gate-all-around (GAA) cylindrical geometry with a 6nm diameter, larger than silicon Bohr radius 4.5nm [9], is chosen for this work. The transverse direction size quantization and electrostatic confinement are not strong enough and the top of bulk band structure can be approximately used within reasonable accuracy [11].



Fig. 1 Simulation structure of a cylindrical gate-allaround junctionless nanowire transistor with 10nm gate length and 6nm diameter.



Fig.2 Simulated conduction band edge (dashed lines) and electron density (solid lines) across channel body for different gate bias conditions at (a) off state, Vg=0 (b) threshold voltage, Vg=Vt (c) flatband voltage, Vg=Vfb (d) accumulation conditions, Vg>Vfb.

-3-2-10123

-3-2-10123



Fig.3 Subthreshold slope comparison between this work and literature [2] with a square crosssection junctionless nanowire transistor (5x5nm).



Fig.4 Electron density distributions in saturation across the channel body for two different source/drain extension schemes (a) with 5nm S/D extension underlapping (5,5) (b) Zero S/D extension (zero over/underlapping) (0,0).

The gate length of the simulated JLNTs is 10nm, which is comparable to the de Broglie wavelength [12] but long enough to avoid direct S-D tunneling. As a result transport justifies the use of the Monte Carlo method.

III. ELECTROSTATICS

Fig.1 illustrates the simulation structure of an unstrained ntype silicon JLNT with <110> channel direction. When the gate bias is below threshold, the channel is fully depleted with peak carrier concentration at the center of the cylindrical channel as shown in Fig.2 (a). In Fig.2 (b), as the gate bias increases to threshold voltage, the JLNT is partially depleted and a conducting channel is formed. When the gate bias is equal to flatband voltage in Fig.2(c), current can flow through the entire channel. As can be seen in Fig.2(d), when gate bias is greater than flatband voltage, an accumulation layer forms near the channel surface. To validate the electrostatics simulation, a comparison of SS and DIBL with literature [2] is made. The simulated DIBL/SS 20mV/66.2mV/dec are in good agreement with the literature result of 17mV/61.5mV/dec. Good agreement of SS is observed in Fig.3. In Fig.4, two different S/D extension cases, (a) 5nm gate underlap and (b) zero over/underlap, are examined. Simulations indicate that using



Fig.5 Distribution profiles of (a) electric field (b) electron velocity (c) electron density of two different simulation structures in fig.4 from Monte Carlo ballistic and scattering simulations. $V_{GS}=V_{DS}=0.8V$.

underlap yields better DIBL and SS due to a longer effective channel length in the off and subthreshold states. In saturation the channel pinch-off position is located in the drain underlap region as shown in Fig.4.

IV. BALLISTIC TRANSPORT

The electric field distribution, average electron velocity, and electron density along the channel direction are shown in

Fig.5. There are two electric field peaks in the S/D extension underlapping case as shown in Fig.5 (a). The first electric field peak near the source side arises from the potential drop due to the change from a neutral to an accumulation layer where the source connects to the channel. This electric field peak induces a velocity peak in the underlap region, which accelerates electrons entering the channel. In addition, the second electric field peak is located in the drain underlap region which shields the channel from the drain electric field lines, resulting in a smaller DIBL than in a device without underlap. Fig.6 indicates that in ballistic regime, carrier velocity is almost independent of channel doping. Therefore, the electron density dominates the drive current. In the presence of scattering, the peak velocity value is reduced to about a half of its ballistic limit value. As can be seen in Fig.7, the channel is nondegenerate for low channel doping and the ballistic injection velocity at the top of the barrier is independent of the channel doping. This is because Fermi energy is a weak function of carrier concentration in non-degenerate statistics [13]. Since carriers are injected from thermal equilibrium source side, carriers approach a constant thermal velocity. In heavily doped channel, the doping concentration becomes comparable with effective density of states and the junctionless nanowire transistor becomes degenerate. In degenerate case, only the electrons near the Fermi surface contribute to net transport [14]. Therefore, Fermi energy will be increased as channel



Fig.6 (a) Electron density and (b) velocity distributions for zero over/under-lapping (0,0) with three different channel doping concentrations 10^{19} , 10^{18} , and 10^{15} cm⁻³. $V_{GS}=V_{DS}=0.8V$.

doping increases to allow more available states for electrons to occupy. Hence electrons begin their flight through the device at relatively high energy resulting in higher injection velocity as shown in fig. 7. Therefore, as the channel becomes degenerate the injection velocity significantly increases. However, heavily doped channels have more impurity scattering, which can cause substantial reduction of the injection velocity in scattered transport. The calculated ballistic ratio is 0.5 with channel doping of 10¹⁹ cm⁻³, similar to the NEGF simulation results of Ref. [3].

V. CONCLUSIONS

In this article drift-diffusion and Monte Carlo approaches are used to study JLNT electrostatics and ballistic transport properties, respectively. S/D extension underlapping yields better SCE behavior. Higher channel doping leads to a higher injection velocity. Impurity scattering degrades injection velocity in heavily doped channel.



Fig.7 Injection velocity from source side at top of the barrier for three transport simulations: ballistic, scattering, and scattering independent on channel doping.

REFERENCES

- J. P. Colinge, C-W Lee, A. Afzalian, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A-M Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," Nature Nanotechnology 2010
- [2] P. Razavi, G. Fagas, I. Ferain, R. Yu. S. Das, and J. P. Colinge, "Influence of channel material properties on performance of nanowire transistors," J. Appl. Phys. 111, 2012
- [3] N. Dehdashti Akhavan, I. Ferain, P. Razavi, R. Yu, and J. P. Colinge, "Improvement of carrier ballisticity in junctionless nanowire transistors," Appl. Phys. Lett. 98, 2011
- [4] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Theory of the junctionless nanowire FET," IEEE Electron Devices, vol. 58, 2011
- [5] K.-I. Goto, T.-H. Yu, J. Wu, C. H. Diaz, and J. P. Colinge, "Mobility and screening effect in heavily doped accumulation-mode metal-oxidesemiconductor field-effect transistors," Appl. Phys. Lett. 101, 2012
- [6] D. Vasileska, S.M. Goodnick, and G. Klimeck, Computational electronics semiclassical and quantum device modeling and simulation, CRC press 2010
- [7] Synopsys, Sentaurus Device User's Guide, 2012
- [8] Synopsys, Device Monte Carlo User's Guide, 2012
- [9] E. G. Barbagiovanni, D. J. Lockwood, P. J. Simpson, and L. V. Goncharova, "Quantum confinement in Si and Ge nanostructures," J. Appl. Phys. 111, 2012
- [10] K. Nehari, N. Cavassilas, J. L. Autran, M. Bescond, D. Munteanu, M. Lannoo, "Influence of band structure on electron ballistic transport in silicon nanowire MOSFET's: An atomic study," Solid-State Electronics, 50, 2006
- [11] R. Ravishankar, G. Kathawala, and U. Ravaioli, S. Hasan, and M. Lundstrom, "Comparison of Monte Carlo and NEGF simulations of double gate MOSFETs," J. Computational Electronics 2005
- [12] H. H. Lau, I. H. Hii, Aaron C. E. Lee, M. Taghi Ahmadi, R. Ismail, and V. K. Arora, "The high-field drift velocity in degenerately-silicon nanowires," Proc, INEC 2008
- [13] V. K. Arora, "Ballistic quantum transport in nano devices and circuits," Proc, INEC 2008
- [14] J. H. Davies, The physics of low-dimensional semiconductors, Cambridge university press, 1998