Impact of Intermetallic Compound on Solder Bump Electromigration Reliability

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***Abstract*—Solder bumps are important interconnect components for 3D integration. Their mechanical and electrical properties influence the overall reliability of 3D ICs. A characteristic of solder bumps is that during technology processing and usage their material composition changes. This compositional transformation influences the operation of 3D ICs and, in connection with electromigration, may cause failures in ICs. In this paper we present a model for describing the growth of intermetallic compound inside a solder bump under the influence of electromigration. Simulation results based on the new model are discussed in conjunction with corresponding experimental findings.**

I. Introduction

For the realization of modern 3D ICs new interconnect structures such as through-silicon-vias (TSVs) and solder bumps, together with complex multi-level 3D interconnect structures are gaining importance. The application of new structures and materials inevitably introduces new reliability issues. The interconnect reliability is affected by degradation processes induced by thermal gradients, electromigration (EM), and stressmigration. Solder bumps are important components for 3D integration, because they enable vertical stacking of wafers (c.f. Fig. 1). Pure Sn has been identified as the best Pb-free solder for ultra fine pitch solder bumps for advanced 3D interconnect applications due to its baseline advantages of being electrodeposited and exhibiting a low melting temperature.

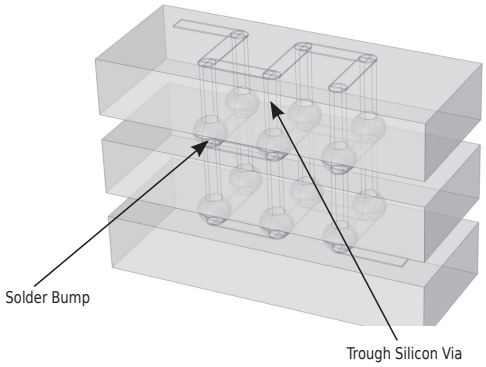

Fig. 1. Schematic representation of wafer stacking by using TSVs and solder bumps.

Failure analyses have shown that failures in Sn bumps occur by EM induced voiding at the interface between the intermetallic compound (IMC) and the solder (c.f. Fig. 2). EM in Sn-based solder bumps is much more complicated than EM in copper due to the presence of impurities.

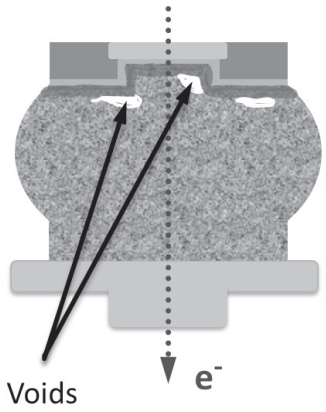

Fig. 2. EM failure is caused by voids which are formed between Ni under bump metalization (UBM) and Sn solder bump.

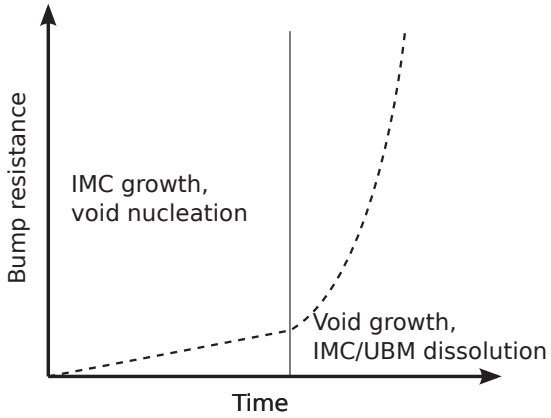

Fig. 3. Resistance change due to IMC growth and voiding with two different slopes.

The development of a failure in a copper interconnect takes place in two distinctive phases: a void nucleation phase and a void evolution phase. During the first phase practically no resistance increase can be measured. The situation is quite different in the case of EM failure development in a Sn bump, where an IMC-layer is also present [1]. From the beginning of EM-stressing a continuous growth of the bump resistance (c.f. Fig. 3) is observed. After a certain period of EM stressing [1], the bump resistance starts to rise with a significantly steeper slope. Chen *et al.* [1] assume that the two slopes of the resistance growth may represent two different stages of failure development: void nucleation combined with IMC growth

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and void propagation with IMC dissolution. Investigation of physical mechanisms behind such a failure behavior is the main subject of this work.

II. Physics of Intermetallic Compound Growth

The solder bump itself is usually designed and realized as an alloy, for example as SnAg, SAC405 (Sn-4% Ag-0.5% Cu), and other Sn, Ag, and Cu combinations [2]. Important for the layouts attached to the solder bumps is an under bump metallization (UBM), which separates the Sn bump from the surrounding metallization. The solder bump with UBM has a lower maximum current density and peak temperature in the solder, which contributes to longer EM lifetimes. A solder bump interface to the UBM, which is usually made of Ni, is also a reason for the development of alloys in solder bumps. At this interface an IMC is formed, which is a thin layer consisting of alloys with Sn as the principal component. Until now several works have been published attempting to model EM induced IMC development [3], [4], however, none of them is applicable for numerical simulation. We describe the growth of the IMC in the Sn solder bump by the following equation system:

$$\frac{\partial C_i}{\partial t} = -\nabla \cdot \vec{J}_i + f_{Sn}(C_i), \tag{1}$$

$$\frac{\partial C_{\text{IMC}_j}}{\partial t} = -\nabla \cdot \vec{J}_{\text{IMC}_j} + \kappa_j(T) C_{Sn} C_i, \tag{2}$$

$$\vec{J}_i = \frac{C_i}{k_B T} \mathbf{D}_i^{Sn} (\nabla \mu_i + |Z_i^*| e \nabla \varphi), \tag{3}$$

$$\vec{J}_{\text{IMC}_j} = \frac{C_{\text{IMC}_j}}{k_B T} \mathbf{D}_{\text{IMC}_j}^{Sn} (\nabla \mu_{\text{IMC}_j} + |Z_{\text{IMC}}^*| e \nabla \varphi). \tag{4}$$

The dynamics of the IMC growth under the influence of EM is determined by an anisotropic EM and diffusion (defined by the tensorial diffusivities $\mathbf{D}_i^{Sn}$ for $i =$ Cu, Ni and $\mathbf{D}_{\text{IMC}_j}^{Sn}$ for $j =$ Cu_6Sn_5, Ni_3Sn_4) and the chemical reaction rates $\kappa_j(T)$ which are thermally activated parameters according to an Arrhenius law. The functions $f_{Sn}(C_i)$ model consummation of Cu and Ni by the chemical reaction in the Sn bump. μ_i and μ_{IMC_j} are the chemical potentials [5].

The model assumes that all transport processes take place in Sn, i.e. Sn is the only transport medium in the model. However, when a thin layer of IMC is formed, impurities migrate through this layer in order to reach the Sn region, where the chemical reaction which produces IMC occurs. Migration through the IMC for both Cu and Ni is characterized by specific diffusion coefficients and effective valences. Since we focus only on a very thin IMC layer, we consider that the model assumption regarding the transport is justified.

A. Model Parameterization and Properties of Sn

The Sn solder bump microstructure plays an important role in interconnect reliability. Compared to Cu, Sn crystallization produces 100-1000 times larger grains. Correspondingly, the role of grain boundaries as fast diffusivity paths is much more pronounced. Sn solder bumps often consist of several large Sn grains, such that most solder bumps exhibit one or at most a few Sn grain orientations [6].

Sn has a bulk tetragonal crystal structure which exhibits highly anisotropic diffusional, electrical, mechanical, thermal, and electrical properties [7].

A clear dependence of the thermo-mechanical response of a Sn solder bump on microstructure and Sn grain orientation was also observed [6]. The coefficient of thermal expansion is higher in the c-axis direction than in the a- or b-axis directions.

The isotropic diffusivity coefficient in Ni is [8]

$$D_{Ni} = 2.9 \exp\Big(-\frac{2.88\,eV}{k_B T}\Big) \frac{\text{cm}^2}{s}. \tag{5}$$

The effective valence for self-EM in Ni is, to the best of our knowledge, not available in the literature. Therefore, we use a simple estimate from the ballistic EM model [9]

$$Z^* = -n_0 l \sigma_{tr}, \tag{6}$$

where n_0 is the electron concentration, l is the electronic mean free path, and σ_{tr} is the transport cross section of the atom evaluated at the Fermi energy. By taking the values for n_0, l, and σ_{tr} from [10] we obtain an estimated $Z_{Ni}^* \approx -10$.

Measurements of self-diffusion in Sn clearly show an anisotropic atomistic transport. From [11] we have

$$D_{c,Sn} = 3.7\,10^{-8} \exp\Big(-\frac{0.25\,eV}{k_B T}\Big) \frac{\text{cm}^2}{s}, \tag{7}$$

$$D_{a,Sn} = D_{b,Sn} = 8.4\,10^{-4} \exp\Big(-\frac{0.45\,eV}{k_B T}\Big) \frac{\text{cm}^2}{s}. \tag{8}$$

The value of self-EM effective valence in Sn is obtained experimentally in [11]: $Z_{Sn}^* \approx -79$.

Diffusion of Ni in Sn is studied in [12] and the following values are obtained:

$$D_{c,Ni(Sn)} = 1.99\,10^{-2} \exp\Big(-\frac{0.19\,eV}{k_B T}\Big) \frac{\text{cm}^2}{s}, \tag{9}$$

$$D_{a,Ni(Sn)} = D_{b,Ni(Sn)} = 1.87\,10^{-2} \exp\Big(-\frac{0.56\,eV}{k_B T}\Big) \frac{\text{cm}^2}{s}. \tag{10}$$

For effective valence of Ni in Sn we have $Z_{Ni(Sn)}^* \approx -67$ [11].

The diffusivity coefficients (7)-(10) build diffusivity tensors which are used in (3) and (4). The basic structures of the diffusivity tensors are given by

$$\bar{\bar{D}}_{Sn} = \begin{bmatrix} D_{Sn}^a & & \\ & D_{Sn}^b & \\ & & D_{Sn}^c \end{bmatrix}, \tag{11}$$

$$\bar{\bar{D}}_{Ni(Sn)} = \begin{bmatrix} D_{Ni(Sn)}^a & & \\ & D_{Ni(Sn)}^b & \\ & & D_{Ni(Sn)}^c \end{bmatrix}. \tag{12}$$

From (7)-(10) at $T = 150°\text{C}$ we have

$$\frac{D_{c,Sn}}{D_{a,Sn}} \approx 174, \quad \frac{D_{c,Ni(Sn)}}{D_{a,Ni(Sn)}} \approx 10^4. \tag{13}$$

The anisotropy of Ni diffusion in Sn is much more pronounced than the anisotropy of Sn self-diffusion.

B. Intermetallic Compound Resistivity

The bump resistance increases due to void formation and microstructure changes during EM can be precisely measured with Kelvin bump probes [1]. IMCs such as Cu_6Sn_5 and Ni_3Sn_4 have a higher resistivity than pure Sn. In the case of Cu_6Sn_5, the resistivity is approximately 60% higher and in the case of Ni_3Sn_4 it is even 160% higher than the resistivity of Sn at room temperature (see Table I).

TABLE I. MATERIAL PROPERTIES AT 20 °C

Materials	Resistivity (nΩm)	Thermal conductivity (WK/m)
Cu	16.8	403.0
Ni	69.3	76.0
Sn	110.0	67.0
Cu_6Sn_5	175.0	34.1
Ni_3Sn_4	285.0	19.6

III. SIMULATION RESULTS AND DISCUSSION

Model (1)-(4) has been implemented in an in-house three-dimensional simulation tool. For the EM reliability analysis we use a multilayer interconnect structure, similar to those usually used for wafers' stacking (c.f. Fig. 4). The first step is the determination of a maximal current density which is reached in some particular bump for given operating conditions (voltage, temperature) of the whole interconnect structure. In the second step the EM in a single solder bump is analyzed. In our study we have considered Ni_3Sn_4 as the primary IMC. The bump structure used in our simulation is sketched in Fig. 5.

Since our simulation is fully three-dimensional it also enables a study of the influence of bump geometry variation on IMC growth. An example of an IMC layer corresponding to 400h of simulation time is presented in Fig. 6.

The formation and growth of IMC at the interface between the UBM and the Sin bump is caused by several physical mechanisms. In the initial phase both Cu and Ni penetrate into Sn bump and segregate just below the UBM/bump contact surface. Corresponding to this initial phase of EM stressing, there is an increase of the IMC's resistance as presented in Fig. 7. The first phase is completed, when the IMC concentration reaches a peak after which an equilibrium concentration level follows. As expected the dynamics of IMC growth is enhanced at elevated temperatures. The increase of the Sn bump resistance is determined by the following mechanisms:

- Diffusion and EM of Cu and Ni in Sn
- Chemical reactions which convert Cu, Ni, and Sn into IMC (e.g. Cu_6Sn_5 and Ni_3Sn_4)
- Diffusion and EM of IMC in Sn

All these processes are thermally activated according to Arrhenius law. Simulation allows to observe and study the interplay between the above mechanisms. As we can see in Fig. 7, in the first hours of EM stressing the resistance increase at 100°C is higher than those at 150°C and 200°C. Both, migration and chemical reaction are enhanced at elevated temperature, but it seems obvious that in the early phase, migration keeps the concentration of impurities below the threshold necessary for an IMC production which would cause an observable resistance increase. The delay in IMC formation process can also be observed in Fig. 8. Subsequent to the IMC formation, the degradation process is continued by vacancy EM in Sn and at the Sn/IMC interface, which was a subject of our previous study [13].

EM of vacancies ultimately leads to void formation and failure of the bump (c.f. Fig. 2), a scenario which is most commonly observed in EM experiments [1]. However, simulation also permits to study a situation, where no void nucleation takes place but EM stressing proceeds, until the whole Sn of solder bump is converted into the IMC. As we can see in Fig. 9 the bump resistance rises with a gradually increased slope, until the whole bump consists only of IMC (Ni_3Sn_4). From our simulation, we conclude that a much steeper second slope (c.f. Fig. 3) observed by Chen *et al.* [1], which appears abruptly after approximately 100h of stressing, can only be caused by an emergence of the new phase between the IMC and Sn the layers. We support the findings of Chen *et al.* [1] that this "second phase" is actually a beginning of void evolution.

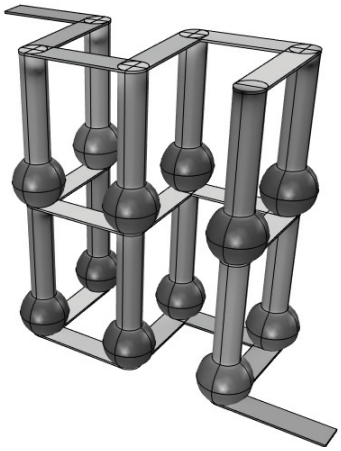

Fig. 4. Multilevel interconnect for 3D integration. Wafers are removed from the picture. Lighter color represents areas with higher current density.

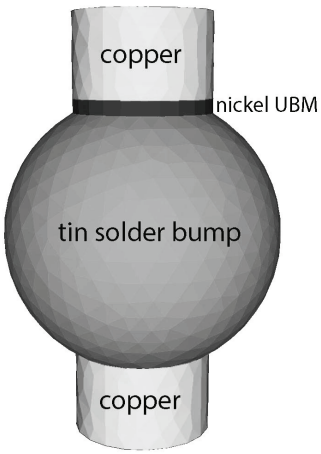

Fig. 5. Structure of the solder bump used for the study. On the top of the Sn bump a Ni UBM is placed.

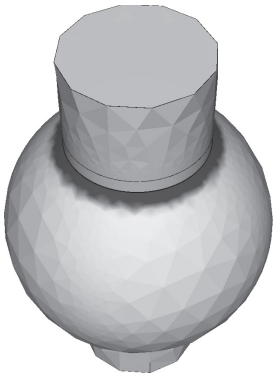

Fig. 6. IMC layer formed at the interface between nickel UBM and Sn solder bump.

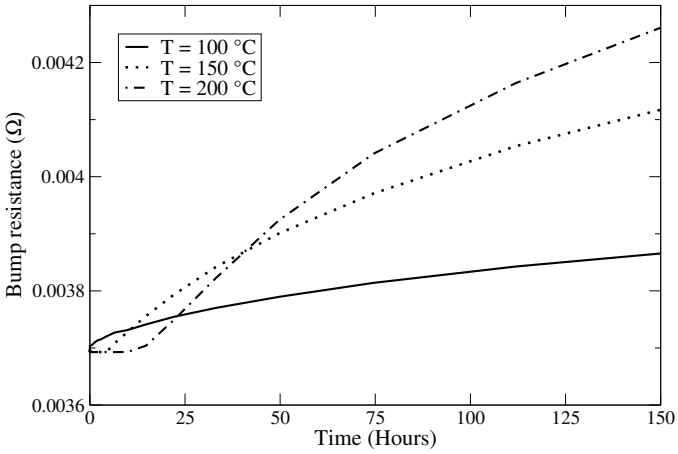

Fig. 7. Initial phase of solder bump resistance growth for three different temperatures.

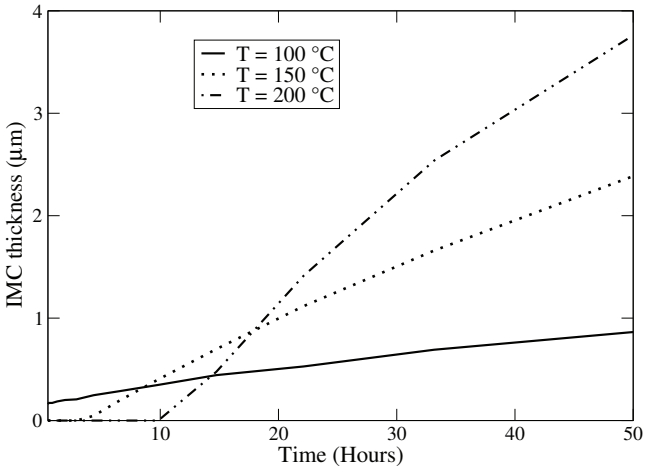

Fig. 8. Growth of IMC thickness in time. Fast migration of Cu and Ni at 150°C and 200°C prevents IMC emergence until 10h of EM stressing.

IV. Conclusion

The development of an IMC phase inside of Sn-based solders bump represents a reliability risk for interconnect structures used for realization of 3D ICs. In this work we have presented a model for IMC growth in Sn solder bumps. The model includes a description of the Cu and Ni migration into the Sn bump and chemical reaction which produces two different types of IMCs. Simulations based on the new model predict three-dimensional profiles of IMC, time-dependent resistance change, and time dependent change of IMC thickness. The obtained results are utilized for explanation and discussion of experimental observations and measurements.

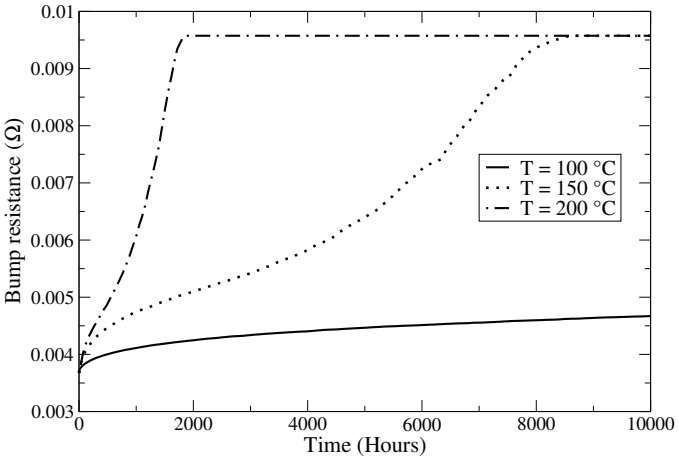

Fig. 9. Late phase of the resistance growth. Resistance of solder bump increases until the whole Sn is converted into IMC.

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