Compact Modeling for Application-Specific High-Sigma Worst Case

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***Abstract*—A high-sigma corner model derived from Monte Carlo simulation with a novel sampling algorithm is presented. Compared with the traditional Monte Carlo simulation approach, the simulation effort and computational resource is greatly reduced. This methodology can be applied to create application-specific corner model for different design spec leading to more competitive designs.**

Keywords—high sigma; compact model; worst case model; Monte Carlo simulation; statistical model; SRAM simulation

I. INTRODUCTION

Device variability has drawn lots of attention in advanced technologies. Accurate and appropriate variation modeling has become one of the critical issues for design enablement [1,2]. The detailed partition for different types of variation sources have been discussed and modeled, including local variation, global variation and variation correlation [3,4]. Traditionally, circuit designers use the corner model to define the worst-case design envelope. However, there are two major shortages for the corner simulation approach. Firstly, although the worst-case of MOSFETs defined at 3 sigma of the saturation current (Idsat) may fulfill the digital applications, it fails to predict the worst-case condition for analog designs, which are more sensitive to transconductance (Gm) and output conductance (Gds), as shown in Fig. 1.

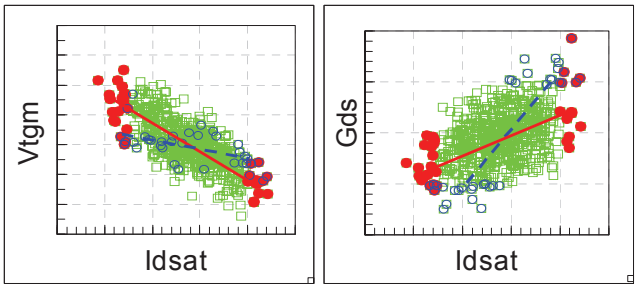

Fig.1 The silicon data show the group of Idsat /Vtgm worst case (the solid dots linked by solid line) is not the worst case of Gds= dId/dVg (the open dots linked by dash line). A universal corner to cover the device variation is not existed. Under this case, the digital corner defined by Idsat/Vtgm underestimated the variation of Gds.

The other issue is the lack of capability for mismatch and local variation cancellation simulation. All of the transistors see the same amount of variation under corner simulation, so users cannot perform local variation simulation for individual transistor correctly. As a result, designers often rely on Monte Carlo simulation to identify the worst case for critical blocks, especially for analog designs.

For a small size of circuits, a full Monte Carlo run is feasible, However, for large-sized memory designs, yield estimation and failure analysis count on reliable statistical data up to 6 sigma's or even higher, which will need at least tens of millions of MC simulations to accurately predict the distribution tail. It is both challenging and time consuming using the conventional MC simulation approach to reach such high-sigma region. This motivated us to seek for a better solution, which can catch the worst-case scenario through an efficient MC simulation. In this work, a novel sampling methodology to reduce the number of MC simulation is presented. This flow can be applied to many applications and extended to define the high-sigma corners. Some examples are presented to illustrate this methodology, including application-specific corner creation, defining the worst-case high-sigma corners for SRAM cell current, static-noise margin and write margin. Compared to the traditional Monte Carlo approach, this new methodology enhanced the simulation efficiency by orders of magnitude.

II. METHODOLOGY

To get a high-sigma distribution effectively, we must reduce the sampling size without sacrificing accuracy. For a pure Gaussian distribution, it's fairly easy to predict the high-sigma distribution by linear extrapolation from a limited data set.

$$N\_sigma\_worst\_case = Median +/- N * sigma \quad (1)$$

In reality, most of the distributions such as the SRAM cell current under low-voltage biasing are not ideal Gaussian distributions [5]. Using linear extrapolation will either overestimates or underestimates the results in the high-sigma region. To resolve this issue, we adopted a power transformation to the target data so that the distribution of the transformed data approaches to a pure Gaussian distribution as shown in Fig.2.

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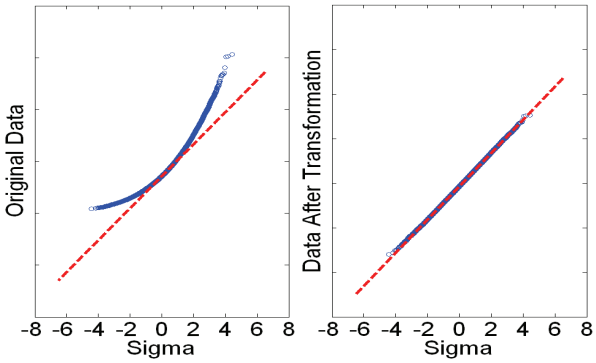

Fig.2 Through the power transformation, the non-Gaussian distribution can be converted in to Gaussian distribution and ready for linear extrapolation.

The high-sigma distribution of the original data can be obtained by linear extrapolation in the transformed domain followed by an inverse transformation. We have compared this high-sigma sampling methodology against direct MC simulations and validated with silicon. Both cases showed that this methodology is an efficient method to predict high-sigma distribution accurately and reliably.

A. Comparison with direct MC simulation

To validate the high-sigma sampling methodology with direct MC simulation, we simulated 10 million MC of SRAM cell currents and used them as the golden data. As expected, the cell current distribution at lower voltage is not a Gaussian as shown in Fig. 3. Directly using low-sigma data for projection would significantly underestimate the SRAM cell current at the high-sigma region. We randomly selected only 100 thousand samples out of these 10 million MC simulations and applied the proposed methodology to project the high-sigma region. As observed in Fig. 3, the result matches that of 10 million direct MC simulations quite well.

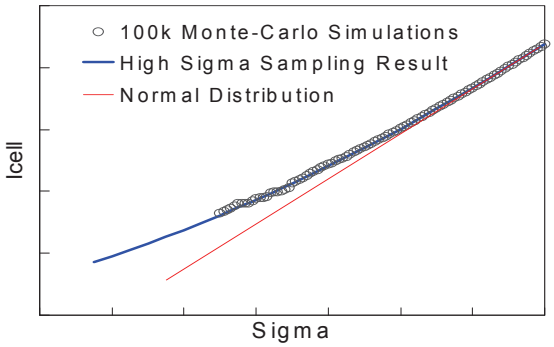

Fig.3 The prediction of high-sigma sampling methodology matches the distribution of direct MC simulations. In the most cases, the liner extrapolation underestimated the Icell level at high sigma regime.

To ensure that this methodology is robust and stable, we repeated this exercise 100 times in randomly selecting 100 thousand data for projection. The results are all stable and consistent as shown in Fig. 4. The max difference is less than 1.5% of Icell among 100 different sampling sets. It demonstrates the repeatability of this methodology.

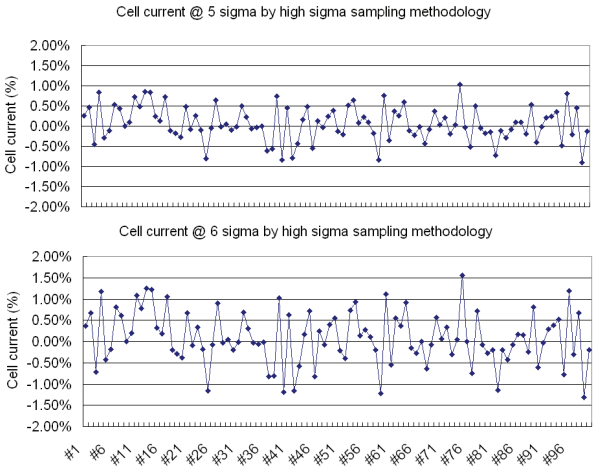

Fig.4 Less than 1.5% Icell difference is observed among 100 sets of exercises. Both 5 and 6 sigma results are extracted from 100 thousand randomly picked samples. It shows the stability of the sampling methodology.

B. Validation with Si statistical data

After validating with direct Monte Carlo simulation, we would like to verify the sampling methodology with measured silicon data. There were 2.8 million 6T SRAM cell currents measured under two bias conditions (0.9V and 0.72V) from a TSMC advanced technology. Firstly, the SPICE model was calibrated for single SRAM device, including PG, PU and PG transistors. The 100 thousand MC runs were then simulated and used as the golden database for high sigma projection. As we expected, the model can match the median and 3-sigma deviation of the cell current well. The proposed high sigma sampling methodology was applied to these MC simulations to validate with 4.9sigma silicon (2.8 million data points equivalent). As shown in Fig. 5, the matching between Monte Carlo projection and silicon is good and the projection up to 6.5-sigma is also on a reasonable trend for both bias conditions. Most importantly, the number obtained from proposed methodology is more competitive than that of the conventional linear approximation. It helps designers to remove the unnecessary guard band for the design sign off.

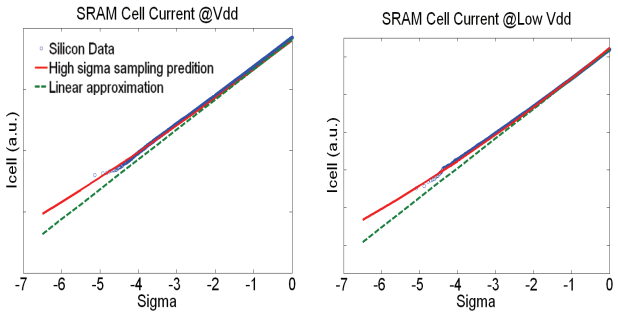

Fig.5 The prediction matches well with the distribution of 2.8Mb SRAM cell current for both 0.9V and 0.72V.

III. EXAMPLE APPLICATIONS

This sampling methodology can be applied to many applications requiring either accuracy in high-sigma regions, or long simulation time needed due to complicated circuit architecture. We will present three real cases, the worst bit corner for SRAM cell current, the worst bit corner for SRAM Static Noise Margin (SNM) and Write Margin (WM) failure analysis and simulation efficiency improvement for analog circuit with multiple types of devices. All three examples follow the flow chart illustrated in Fig. 6, including statistical model building, minimum set of Monte Carlo simulation, power transformation, effective corner building and finally corner simulation.

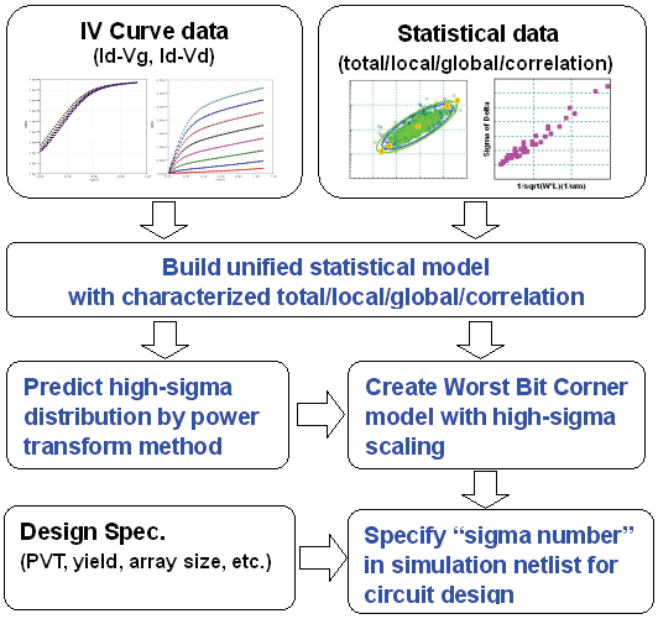

Fig.6 A general flow and usage of high-sigma worst bit corner model.

A. *Worst-bit corner model for SRAM cell current*

Traditional SRAM cell performance simulation is performed based on the 3-sigma corner model for pull-down, pass-gate, and pull-up devices. There are two major issues for the 3-sigma based corner simulation. For the lower sigma region, the cancellation of local variation among these devices are not considered, so the result predicted by the corner model is too conservative even for the lower sigma region. For the higher sigma region, the linear approximation from 3-sigma corner cannot reflect the non-Gaussian distribution, so the gap is getting worse as the number of sigma increases compared with Monte Carlo simulation shown in Fig. 7(a). Although Monte Carlo simulation is one of the solutions to resolve this issue, the long simulation time is still a common concern for Monte Carlo simulation. As a result, we apply the proposed sampling methodology to extend 100K Monte Carlo results and get high sigma distribution at a given global variation corner. The worst bit corner (WBC) model can be constructed with scalable sigma factor to characterize cell current as shown in Fig. 7(b). Designers can obtain the tail of the cell current distribution by sweeping sigma factor in WBC model.

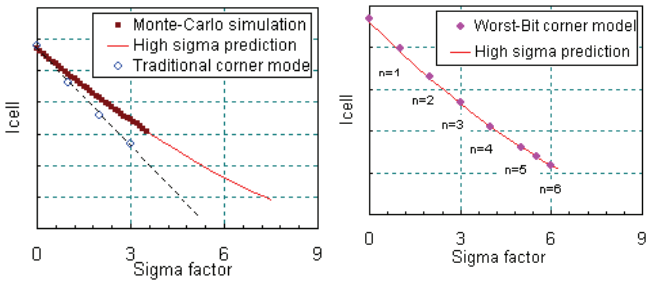

Fig.7 (a) Traditional corner model outputs lower cell current than statistical model, especially at high sigma region (left). (b) Cell current WBC corner with good scaling of sigma factor up to 6s is developed to provide the design reference of cell optimization (right).

To take the most advantage of the Icell vs. sigma factor shown in Fig. 7, we calibrate the sigma factor for different combination of memory size and yield percentage as listed in table 1. The table represents the required sigma to satisfy the specified yield for a given memory size. The yield is evaluated by the all-bit-pass rate of the memory array for two data states expressed as following:

$$Yield = (1 - P_{bit})^{2N} \qquad (2)$$

where N is the cell array size. P_{bit} is the probability of 1-bit failure out of N cells memory while assuming the each bit failure is an independent event [6].

Yield	Memory array size							
	1M	8M	32M	64M	128M	256M	512M	1024M
99.9%	6.12	6.44	6.65	6.75	6.85	6.95	7.05	7.14
95%	5.46	5.81	6.04	6.15	6.26	6.37	6.47	6.58
50%	4.97	5.36	5.61	5.73	5.84	5.96	6.07	6.18

Table.1 The number in this table represents the required sigma to satisfy the specified yield for a given memory size.

The new feature actually allows designers to do yield analysis with the specified sigma number set in the SPICE netlist directly. This is a significant enhancement for memory design simulation in advanced technologies, for which the memory size is usually quite large.

B. *Worst-bit corner model for SRAM Static-Noise Margin (SNM) and Write Margin (WM)*

The simulation of minimum static noise margin (SNM) and write margin (WM) involve both global and local variation, so the traditional corner is inadequate for this purpose. In addition, designers may need a specific model to optimize the read/write assistant circuit, so only a simple SNM/WM number projected from Monte Carlo simulation is not good enough for practical usage. As a result, we applied the proposed high sigma sampling methodology to overcome this challenging. Firstly, the minimum set of Monte Carlo simulation is simulated to reflect SNM/WM distribution at various operating voltages. Followed the methodology discussed in this work, the high sigma behavior can be predicted from golden data set generated by Monte Carlo runs. Finally, the enhanced corner model can be derived from those predicted numbers with a scalable sigma factor (n). The characteristic of static noise

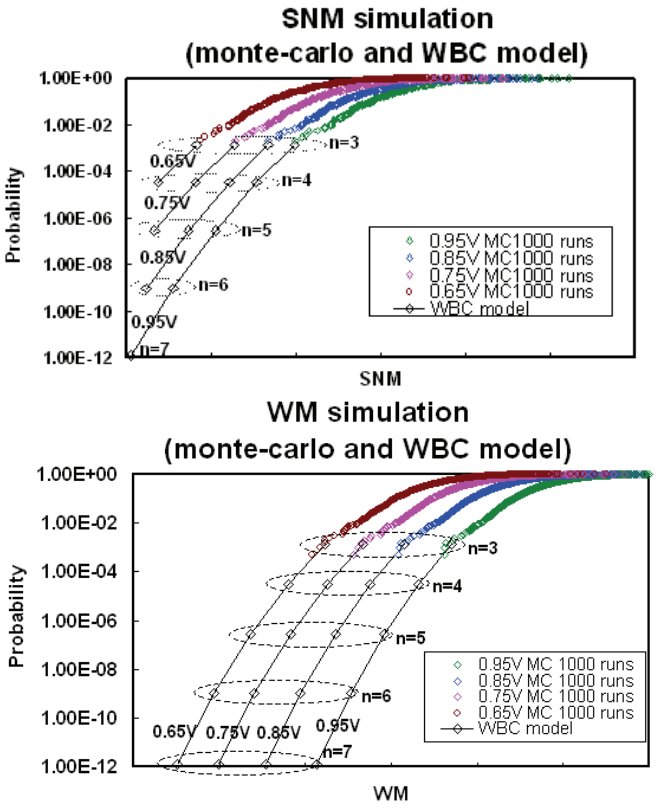

Fig.8 A compact corner model with sigma factor (n) as an instance is developed to reflect the characteristic of static noise margin (top) and write margin (bottom) in SRAM.

margin and write margin versus different Vdd ranges is captured and presented in Fig. 8 (a) and (b). This is the first time the SNM and WM simulation can be done by corner model with high sigma scaling. It indeed provides memory designers a very efficient design reference for cell performance optimization and possible read/write assistance.

C. Analog Circuit Simulation time improvement

Traditionally, the corner model is designed for digital application and implemented for the speed and leakage optimization. Analog performance is usually related to low bias and many analog parameters, like transconductance (Gm) and output conductance (Gds) do not exhibit Gaussian distribution. As a result, the worst case of analog parameters usually cannot share the same worst case as speed and leakage corners. On top of this, analog performance often involves the mismatch of various devices, such as Resistor, BJT and MOSFET. As a result, corner models are not adequate to identify the worst case of analog performance as shown in Fig.9.

Instead, MC simulations are common in the analog designer community to locate the worst-case situations. In this example, we adopt 100 MC simulations with power transformation on the same circuit used in Fig. 8 and extend the result to predict the 3-sigma performance. The prediction matches well with the distribution from 2000 directs MC simulations with more than 20X speed-up in simulation time. This significant simulation time improvement can encourage designers using more MC simulation in design optimization.

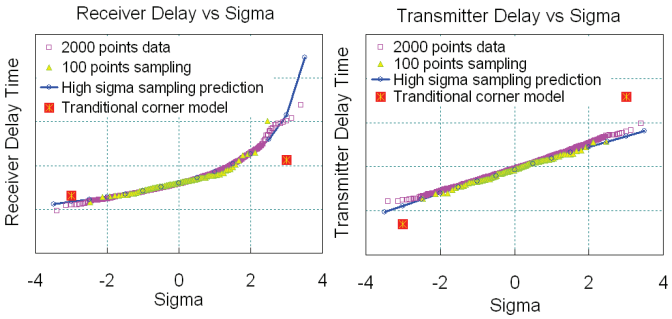

Fig.9 Tradition 3sigma corner model may overestimate or underestimate the variation of circuit simulation. The prediction from 100 data points matches well with 2000 points MC simulation.

IV. CONCLUSION

We have demonstrated a novel sampling methodology to accurately predict the distribution beyond 6-sigma without the need of huge amount of MC simulations. Both direct MC simulations and silicon have validated the accuracy and stability of this methodology. In addition, a general flow to create high-sigma worst-case model is presented. Applications such like SRAM cell current, SNM, and WM worst bit corner model have been developed and implemented in TSMC advanced technologies. The same approach can be extended to create analog-specific corner model and other application-specific worst-case models.

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